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1 Block diagram and pin description

Figure 1. Block diagram

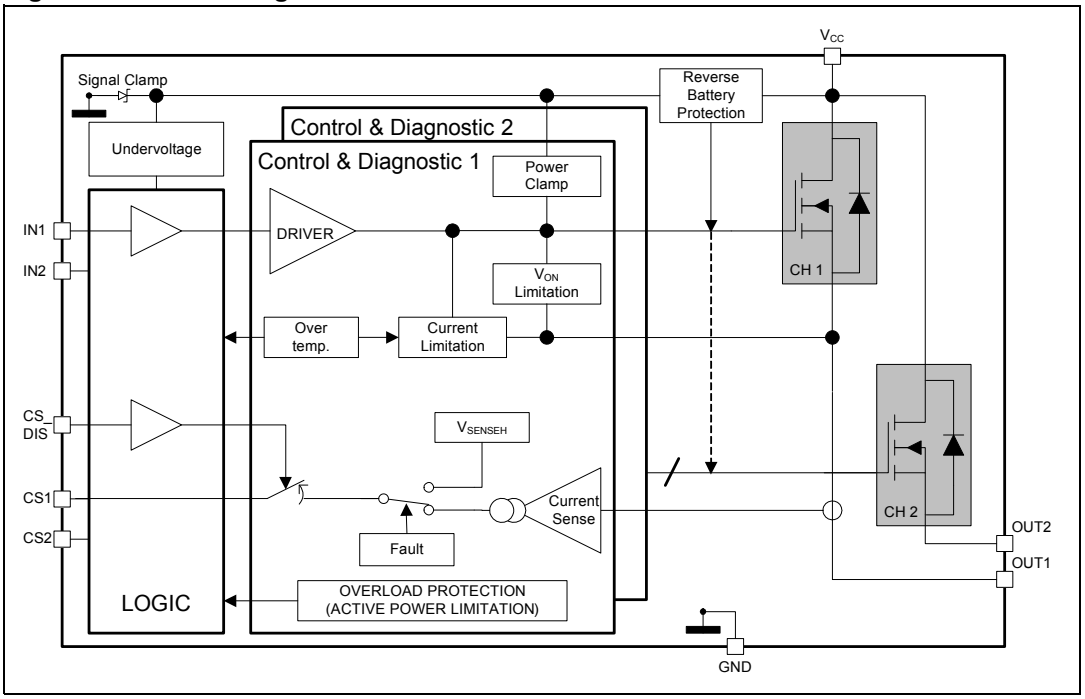


Table 1. Pin function

Name	Function
V_{CC}	Battery connection
$OUT_{1,2}$	Power output
GND	Ground connection
$IN_{1,2}$	Voltage controlled input pins with hysteresis, CMOS compatible. They controls output switch state
$CS_{1,2}$	Analog current sense pins, they deliver a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin

Figure 2. Configuration diagram (top view)

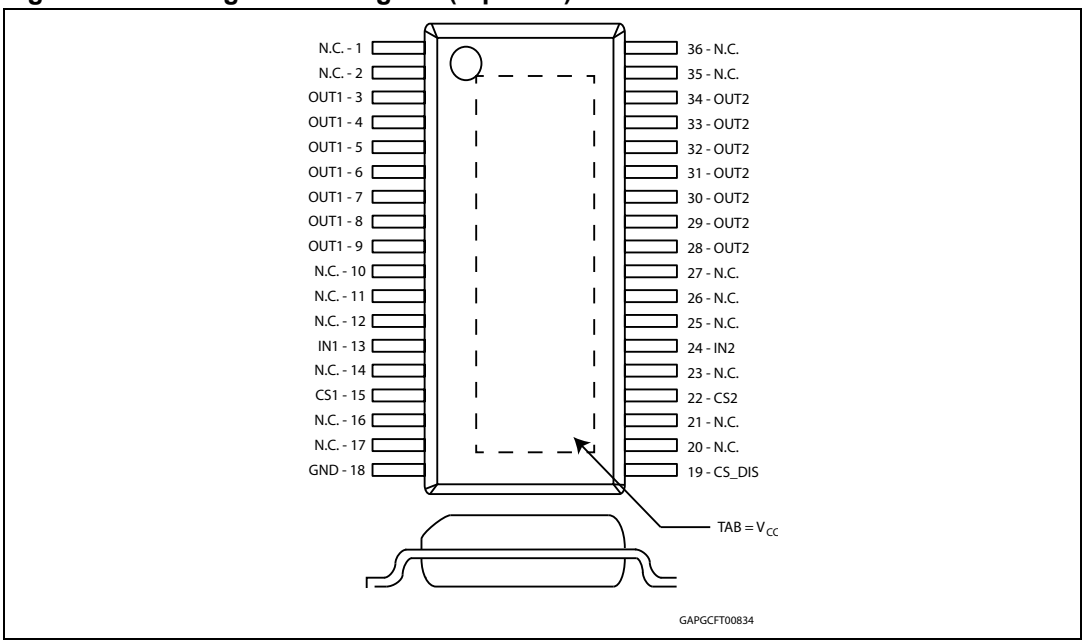


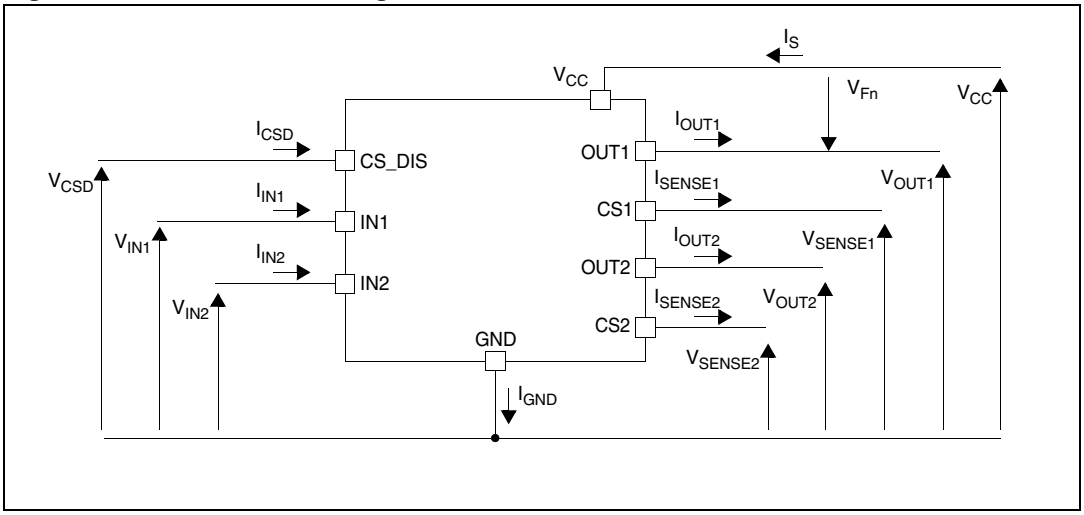
Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	Not allowed	X(1)	X	X	X
To ground	Through 1 KΩ resistor	X	Not allowed	Through 10 KΩ resistor	Through 10 KΩ resistor

1. X: do not care.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	16	V
V_{CC_LSC}	Maximum supply voltage for full protection to short-circuit (AEC-Q100-012)	18	V
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	35	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC} - 41 $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) (L = 0.26 mH; R_L = 0 Ω; V_{BAT} = 13.5 V; T_{jstart} = 150°C; $I_{OUT} = I_{limL}$*(Typ.)*)	29	mJ

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 KΩ; C = 100 pF) – IN – CS – CS_DIS – OUT – V_{CC}	 4000 2000 4000 5000 5000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Maximum value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (with one channel on)	1.4	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (MAX)	See *Figure 35* in the thermal section	°C/W

2.3 Electrical characteristics

Values specified in this section are for 8 V < V_{CC} < 28 V; -40°C < T_j < 150°C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	ON-state resistance	I_{OUT} = 3 A; T_j = 25°C		25		mΩ
		I_{OUT} = 3 A; T_j = 150°C			50	
		I_{OUT} = 3 A; V_{CC} = 5 V; T_j = 25°C		35		
$R_{ON\ REV}$	Reverse battery ON-state resistance	V_{CC} = -13 V; I_{OUT} = -3 A; T_j = 25°C		25		mΩ
V_{clamp}	Clamp voltage	I_S = 20 mA	41	46	52	V
I_S	Supply current	Off-state: V_{CC} = 13 V;T_j = 25°C; V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0 V		2(1)	5(1)	µA
		On-state: V_{CC} = 13 V; V_{IN} = 5 V; I_{OUT} = 0 A		3.5	6.5	mA
$I_{L(off)}$	OFF-state output current (2)	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25°C	0	0.01	3	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125°C	0		5	

1. PowerMOS leakage included.
2. For each channel.

Table 6. Switching (V_{CC} = 13 V; T_j = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 4.3 Ω (see *Figure 6*)	—	20	—	µs
$t_{d(off)}$	Turn-off delay time	R_L = 4.3 Ω (see *Figure 6*)	—	20	—	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L = 4.3 Ω	—	See *Figure 26*	—	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L = 4.3 Ω	—	See *Figure 27*	—	V/µs
W_{ON}	Switching energy losses during t_{won}	R_L = 4.3 Ω (see *Figure 6*)	—	0.25	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 4.3 Ω (see *Figure 6*)	—	0.3	—	mJ

Table 7. Current sense (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.5 A; V_{SENSE} = 0.5 V T_j = -40°C to 150°C	1000	2900	5000	
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 2 A; V_{SENSE} = 0.5 V T_j = -40°C to 150°C T_j = 25°C to 150°C	1900 2240	3000 3000	3810 3520	
dK_1/K_1 (1)	Current sense ratio drift	I_{OUT} = 2 A; V_{SENSE} = 0.5 V; V_{CSD} = 0 V; T_j = -40°C to 150°C	-9		9	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 3 A; V_{SENSE} = 4 V T_j = -40 °C to 150 °C T_j = 25 °C to 150 °C	2230 2460	3000 3000	3550 3350	
dK_2/K_2 (1)	Current sense ratio drift	I_{OUT} = 3 A; V_{SENSE} = 4 V; V_{CSD} = 0 V; T_j = -40°C to 150°C	-6		6	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 10 A; V_{SENSE} = 4 V T_j = -40°C to 150°C T_j = 25°C to 150°C	2710 2780	2900 2900	3150 3080	
dK_3/K_3 (1)	Current sense ratio drift	I_{OUT} = 10 A; V_{SENSE} = 4 V; V_{CSD} = 0 V; T_j = -40°C to 150°C	-3		3	%
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{CSD} = 5 V; V_{IN} = 0 V; T_j = -40°C to 150°C	0		1	µA
		I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{CSD} = 0 V; V_{IN} = 5 V; T_j = -40°C to 150°C	0		2	
		I_{OUT} = 3 A; V_{SENSE} = 0 V; V_{CSD} = V_{IN} = 5 V;	0		1	
V_{SENSE}	Max analog sense output voltage	I_{OUT} = 15 A; V_{CSD} = 0 V	5			V
V_{SENSEH}	Analog sense output voltage in fault condition(2)	V_{CC} = 13 V; R_{SENSE} = 10 KΩ		8		V
I_{SENSEH}	Analog sense output current in fault condition(2)	V_{CC} = 13 V; V_{SENSE} = 5 V		9		mA
$t_{DSENSE1H}$	Delay response time from falling edge of CS_DIS pin	V_{SENSE} < 4 V; 0.5 A < I_{OUT} < 10 A; I_{SENSE} = 90% of $I_{SENSE\ max}$ (see *Figure 4*)		20	100	µs
$t_{DSENSE1L}$	Delay response time from rising edge of CS_DIS pin	V_{SENSE} < 4 V; 0.5 A < I_{OUT} < 10 A; I_{SENSE} = 10 % of $I_{SENSE\ max}$ (see *Figure 4*)		5	20	µs

Table 7. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{DSENSE2H}$	Delay response time from rising edge of IN pin	V_{SENSE} < 4 V; 0.5 A < I_{OUT} < 10 A; I_{SENSE} = 90 % of $I_{SENSE\ max}$ (see *Figure 4*)		70	300	µs
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4V; I_{SENSE} = 90 % of $I_{SENSEMAX}$, I_{OUT} = 90 % of I_{OUTMAX} I_{OUTMAX} = 3 A (see *Figure 7*)			100	µs
$t_{DSENSE2L}$	Delay response time from falling edge of IN pin	V_{SENSE} < 4 V; 0.5 A < I_{OUT} < 10 A; I_{SENSE} = 10 % of $I_{SENSE\ max}$ (see *Figure 4*)		5	50	µs

1. Parameter guaranteed by design; it is not tested.
2. Fault condition includes: power limitation, overtemperature and open-load OFF-state detection.

Table 8. Open-load detection (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Open-load off-state voltage detection threshold	V_{IN} = 0 V; 8 V < V_{CC} < 18 V	2	—	4	V
I_{OL}	Open-load on-state current detection threshold	V_{IN} = 5 V; 8 V < V_{CC} < 18 V; I_{SENSE} = 5 µA		—	45	mA
t_{DSTKON}	Output short circuit to V_{cc} detection delay at turn off	See *Figure 5*	180	—	1200	µs
td_vol	Delay response from output rising edge to V_{SENSE} rising edge in open-load	V_{IN} = 0 V; V_{OUT} = 4 V; V_{SENSE} = 90 % of V_{SENSEH}		—	20	µs
I_{LOFF2}	Off-state output current	V_{OUT} = 4 V	-75	—	0	µA

Table 9. Protections and diagnostics(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short-circuit current	V_{CC} = 13 V	33	47	66	A
		5 V < V_{CC} < 18 V			66	
I_{limL}	Short-circuit current during thermal cycling	V_{CC} = 13 V; T_R < T_j < T_{TSD}		12		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of status		135			°C

Table 9. Protections and diagnostics[1] (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; V_{IN} = 0 V; L = 6 mH; T_j = -40°C	V_{CC} - 39	V_{CC} - 46	V_{CC} - 52	V
		I_{OUT} = 2 A; V_{IN} = 0; L = 6 mH; 25°C < T_j < 150°C	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.1 A; T_j = -40°C to150°C (see *Figure 8*)		25		mV

1. To ensure long term reliability under heavy overload or short-circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level input voltage				0.9	V
I_{IL}	Low-level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	High-level input voltage		2.1			V
I_{IH}	High-level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		
V_{CSDL}	Low-level CS_DIS voltage				0.9	V
I_{CSDL}	Low-level CS_DIS current	V_{CSD} = 0.9 V	1			µA
V_{CSDH}	High-level CS_DIS voltage		2.1			V
I_{CSDH}	High-level CS_DIS current	V_{CSD} = 2.1 V			10	µA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	I_{CSD} = 1 mA	5.5		7	V
		I_{CSD} = -1 mA		-0.7		

Figure 4. Current sense delay characteristics

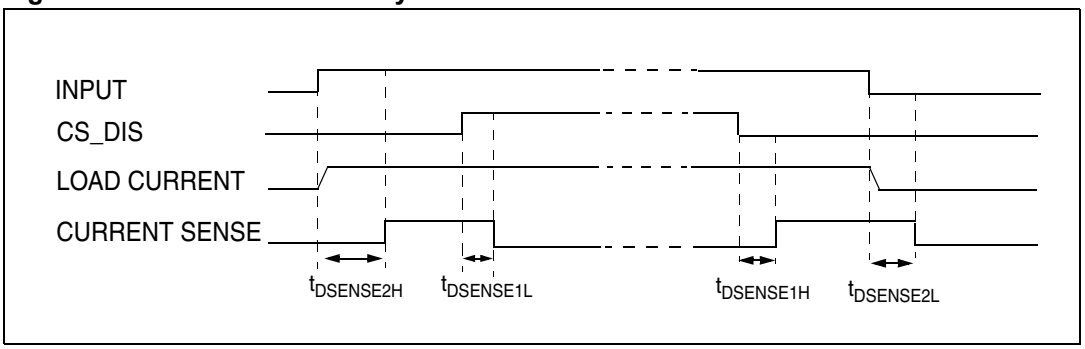


Figure 5. Open-load off-state delay timing

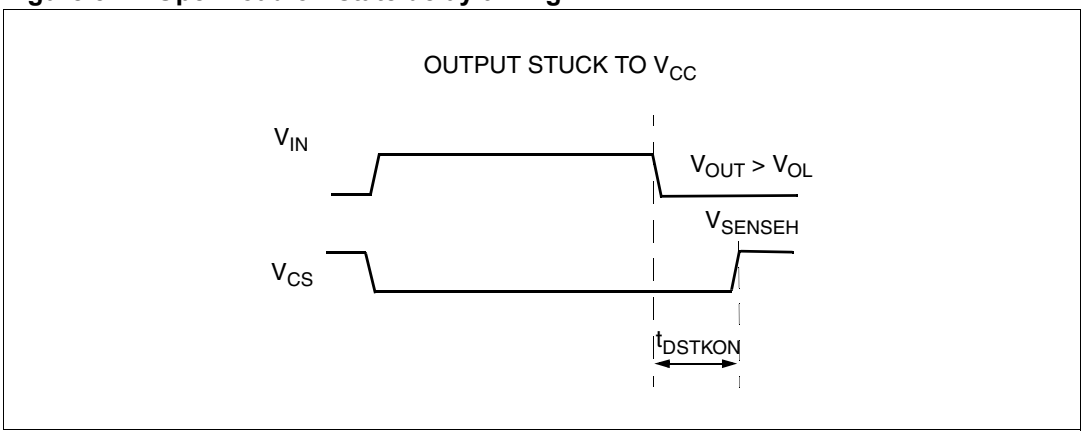


Figure 6. Switching characteristics

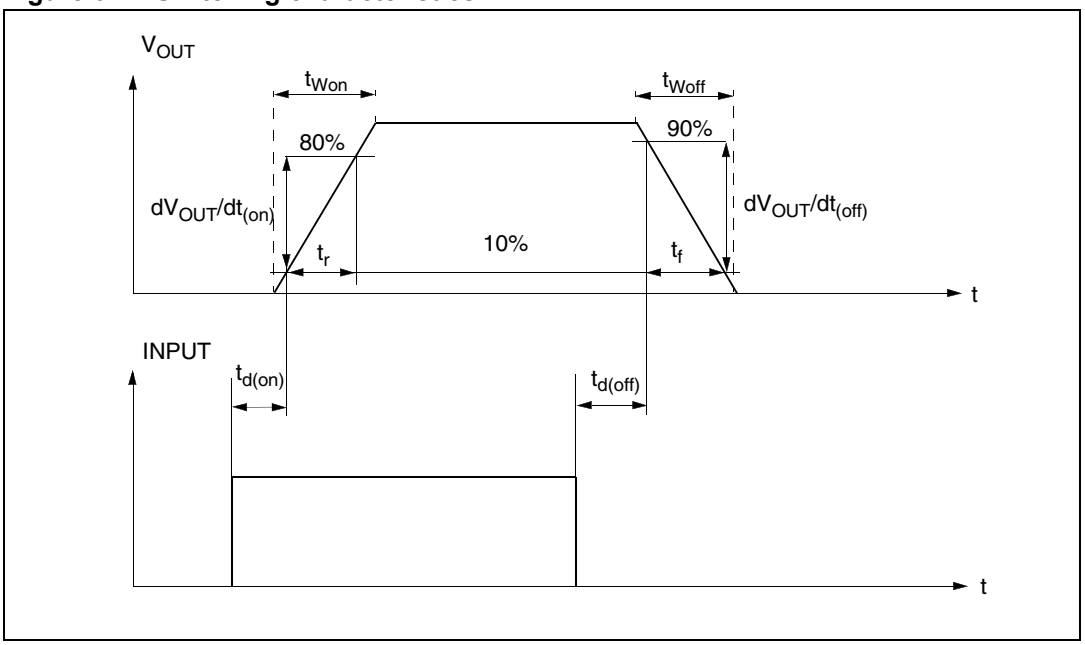


Figure 7. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

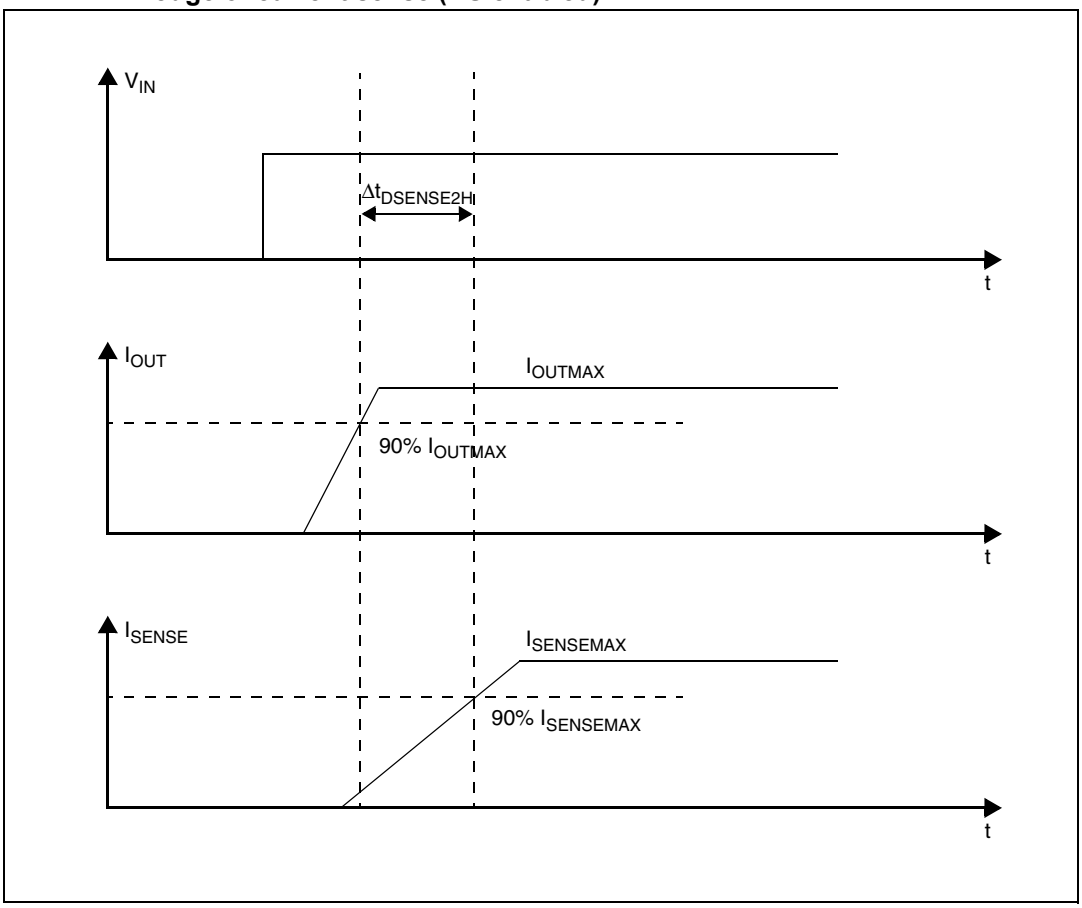


Figure 8. Output voltage drop limitation

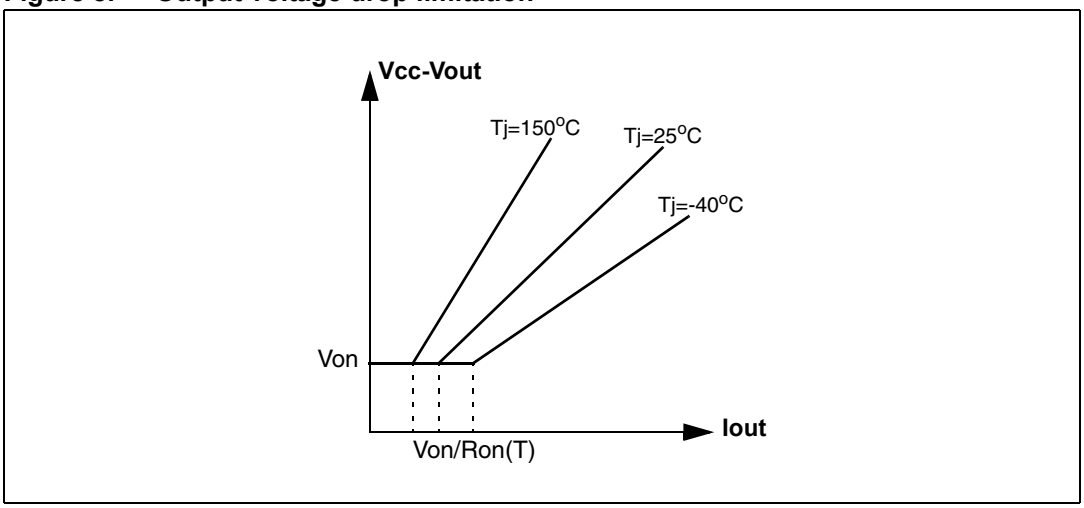


Figure 9. I_{OUT}/I_{SENSE} vs I_{OUT}

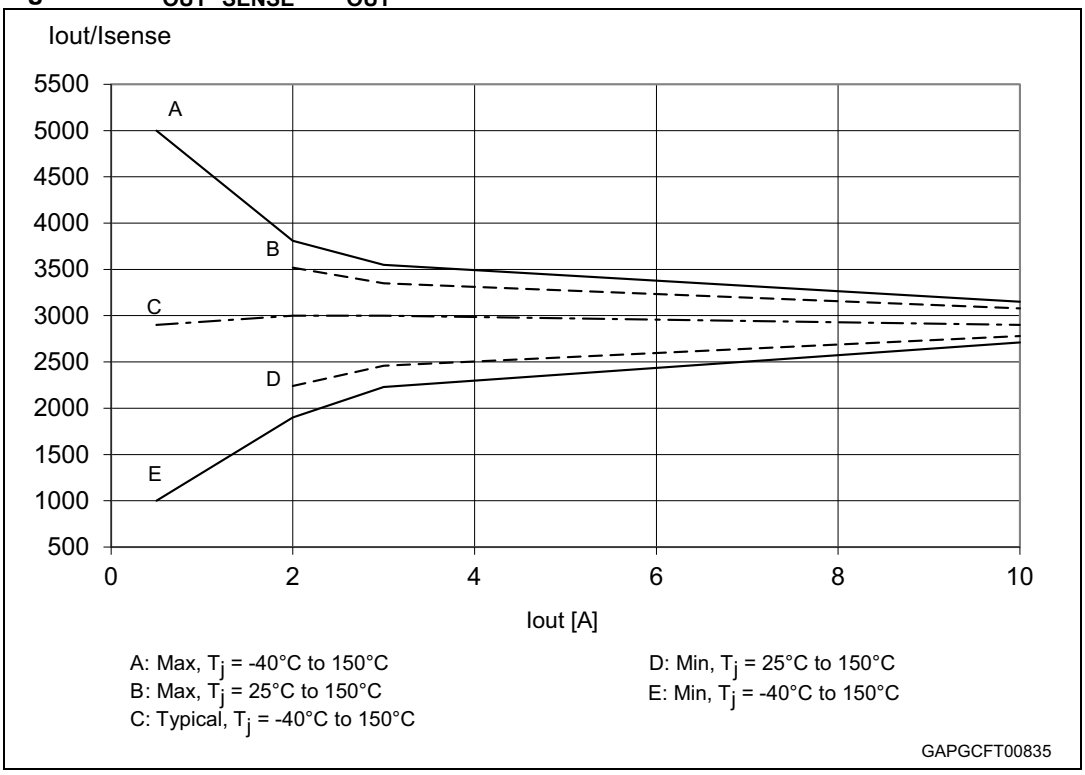
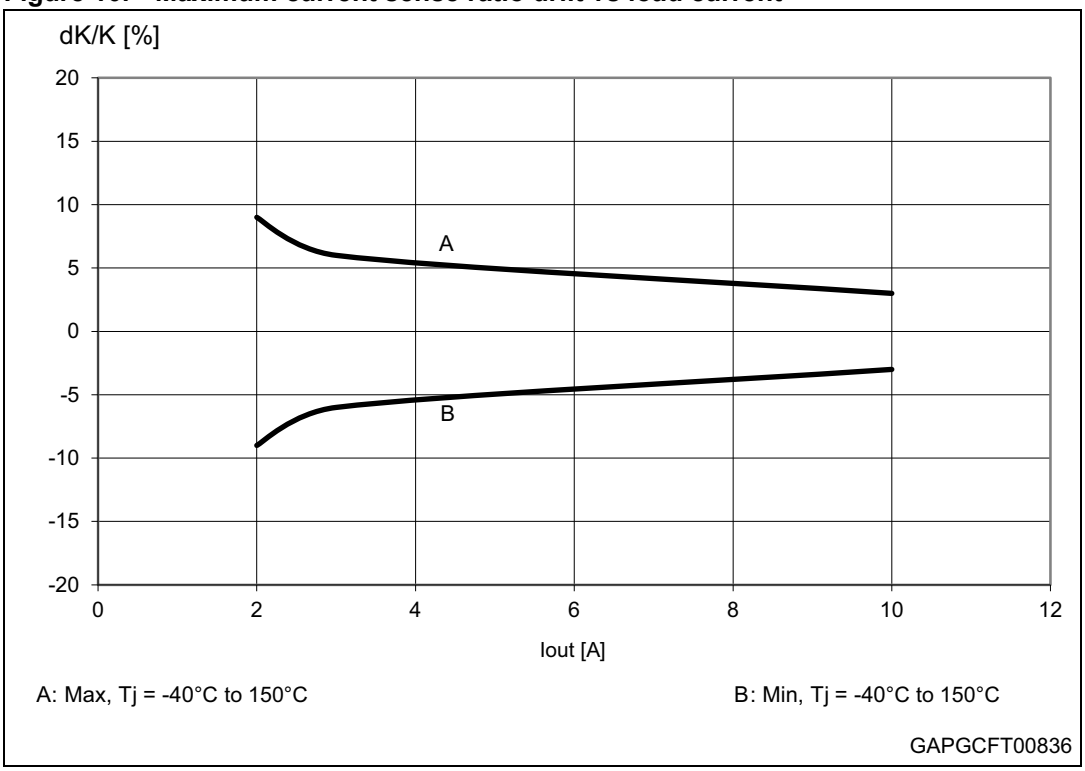


Figure 10. Maximum current sense ratio drift vs load current



1. Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	Input	Output	Sense (V_{CSD} = 0 V)(1)
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overload	H H	X (no power limitation) Cycling (power limitation)	Nominal V_{SENSEH}
Short-circuit to GND (Power limitation)	L H	L L	0 V_{SENSEH}
short-circuit to V_{CC} (external pull up disconnected)	L H	H H	V_{SENSEH} < Nominal
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b(2)	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. The above test levels must be considered referred to V_{CC} = 13.5V except for pulse 5b
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results(1)	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(2)(3)	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b
2. Valid in case of external load dump clamp: 40 V maximum referred to ground.
3. Suppressed load dump (pulse 5b) is withstood with a minimum load connected as specified in *Table 3: Absolute maximum ratings*.

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 11. Normal operation

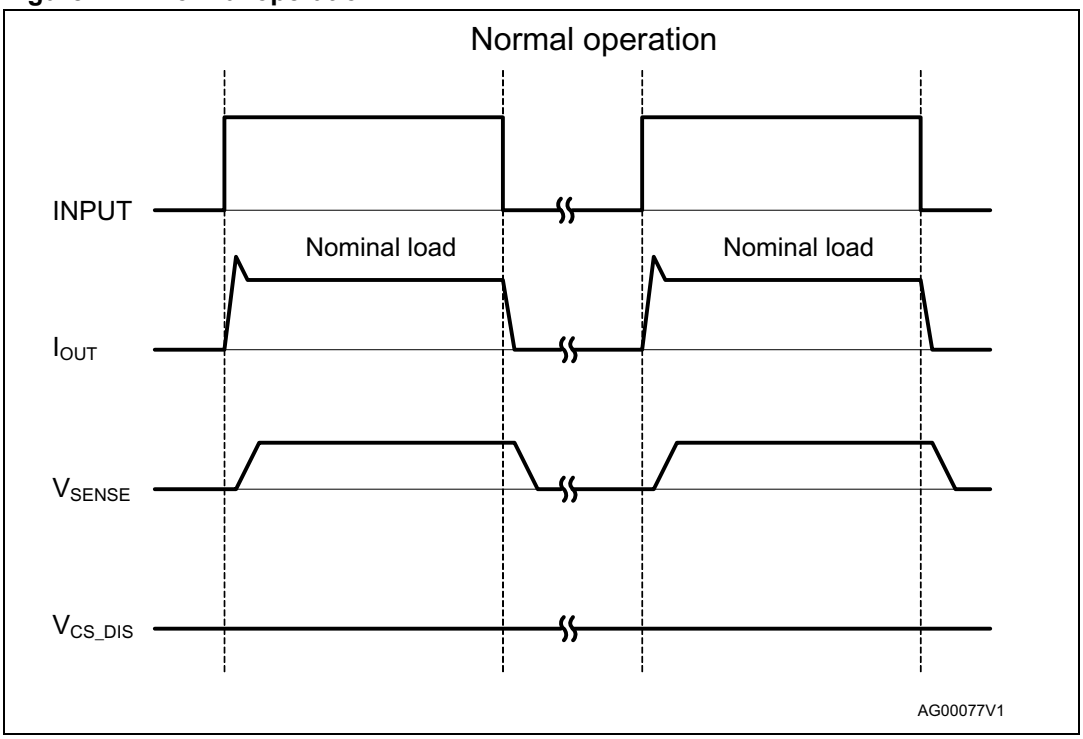


Figure 12. Overload or short to GND

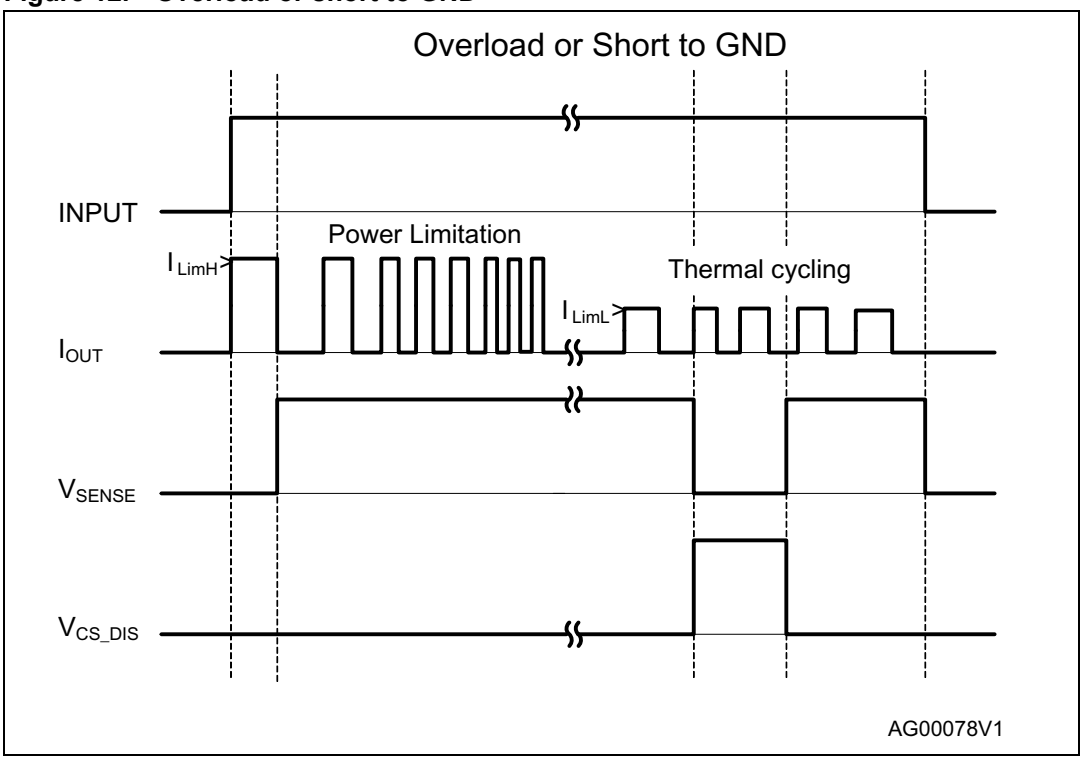


Figure 13. Intermittent overload

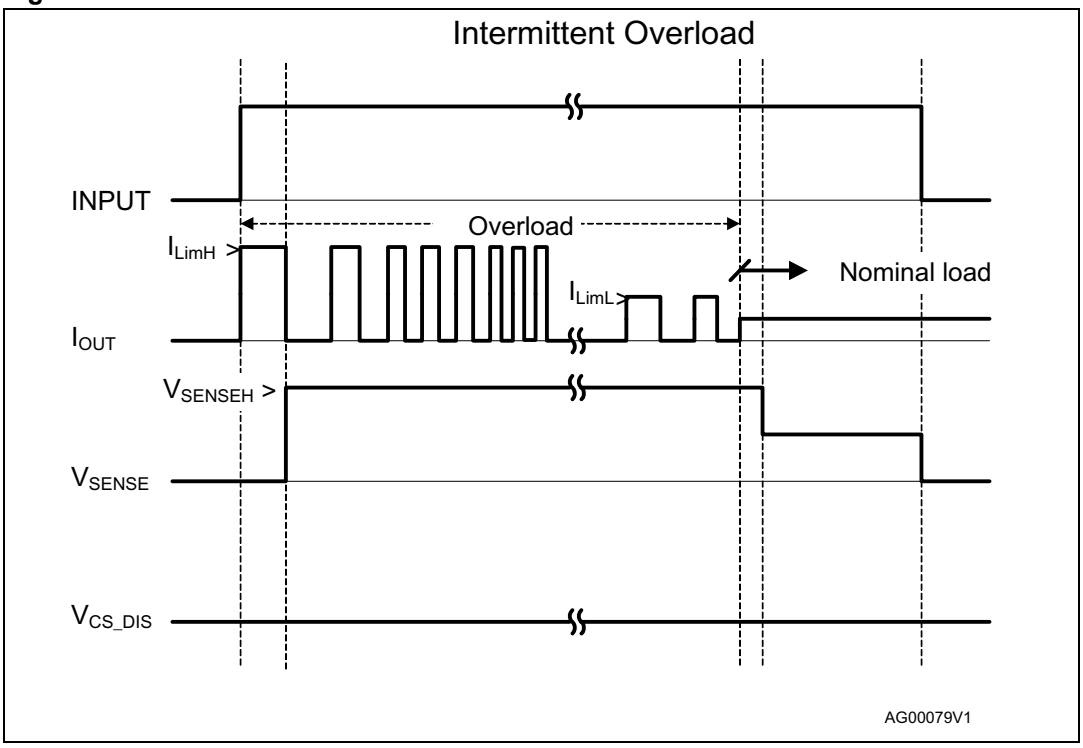


Figure 14. Short to V_{CC}

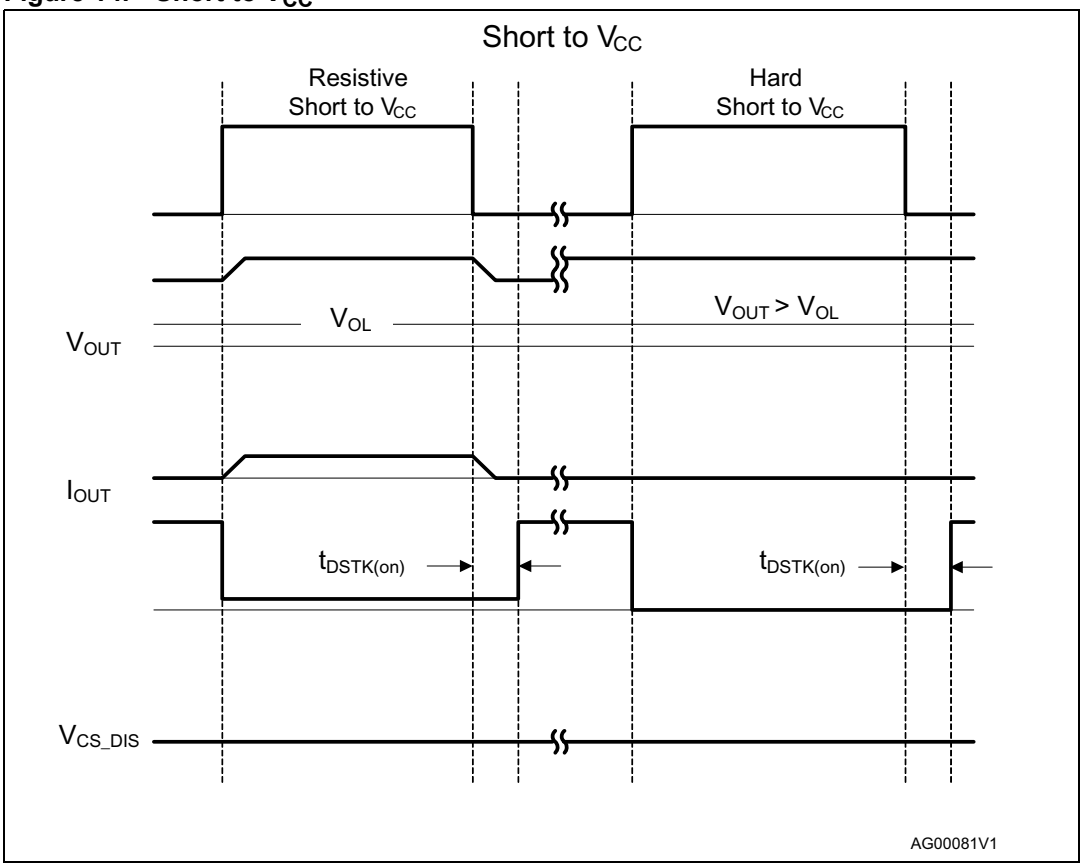
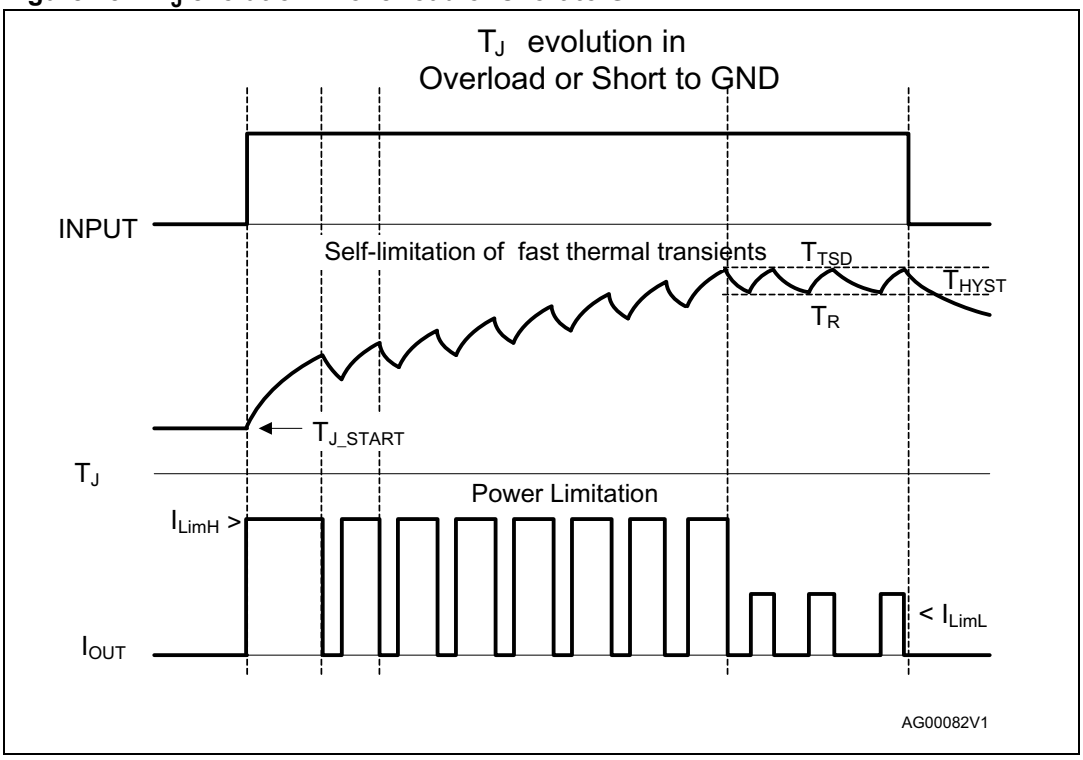


Figure 15. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 16. Off-state output current

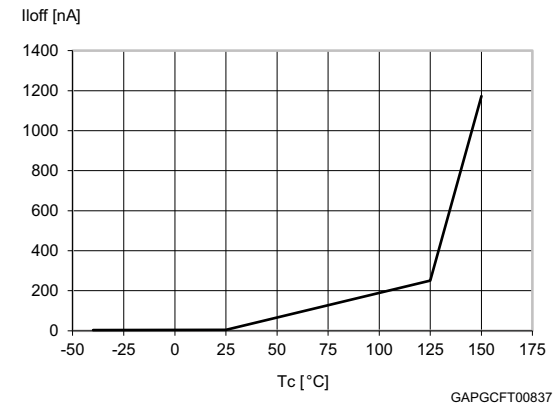


Figure 17. High-level input current

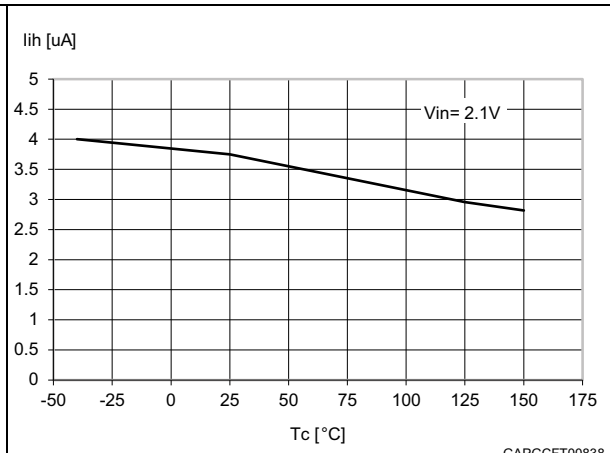


Figure 18. Input clamp voltage

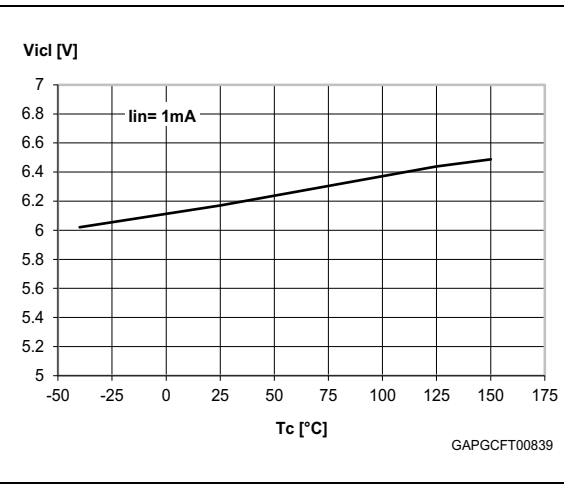


Figure 19. High-level input voltage

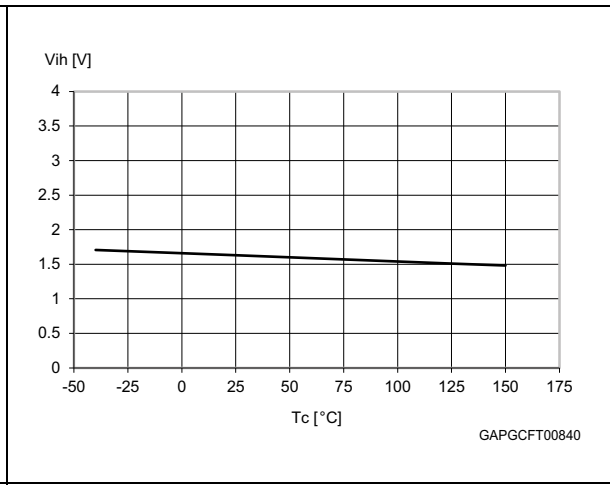


Figure 20. Low-level input voltage

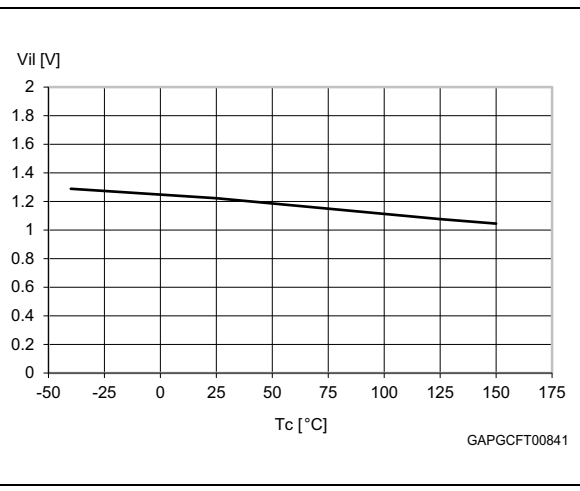


Figure 21. Input hysteresis voltage

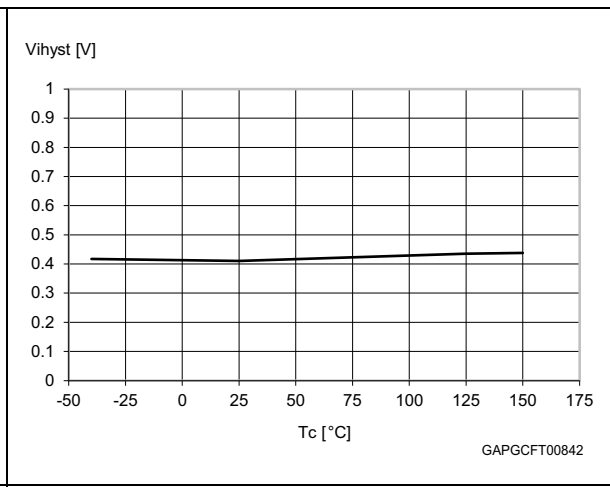


Figure 22. On-state resistance vs T_{case}

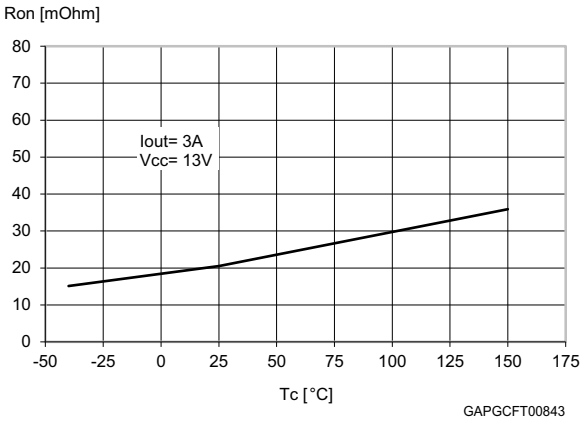


Figure 23. On-state resistance vs V_{CC}

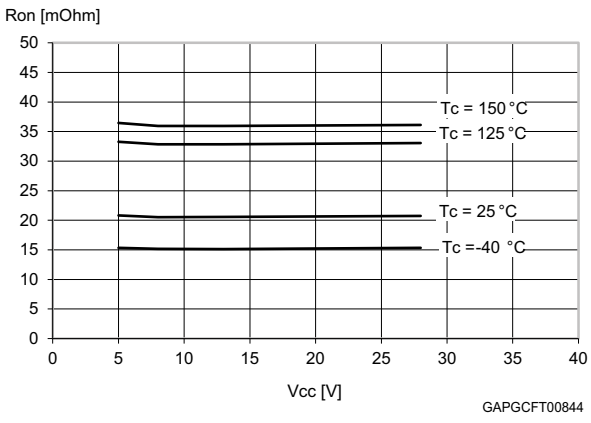


Figure 24. Undervoltage shutdown

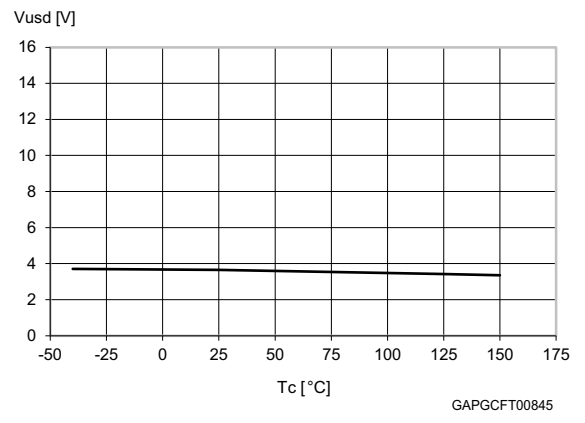


Figure 25. I_{LIMH} vs T_{case}

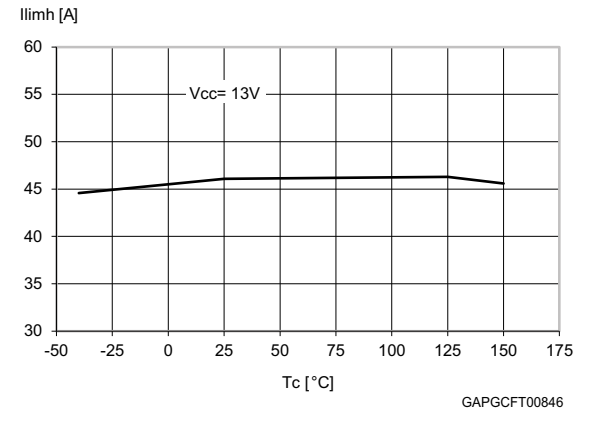


Figure 26. Turn-on voltage slope

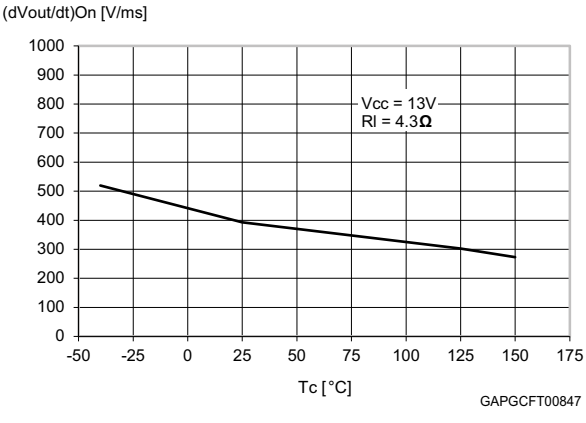


Figure 27. Turn-off voltage slope

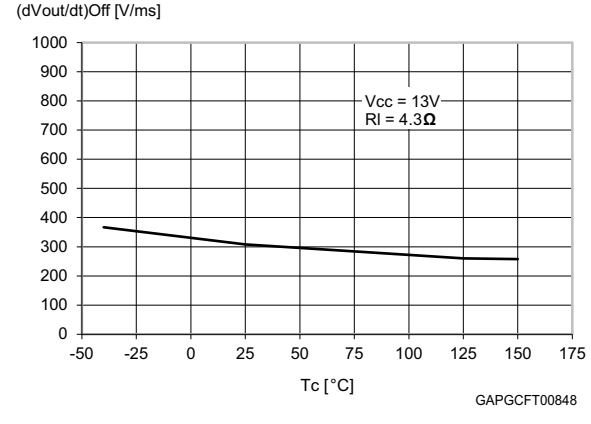


Figure 28. CS_DIS clamp voltage

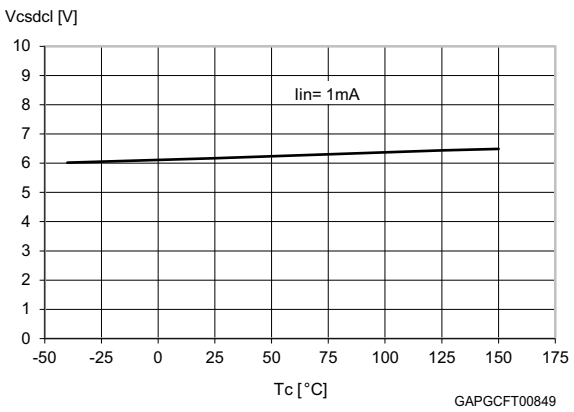


Figure 29. Low-level CS_DIS voltage

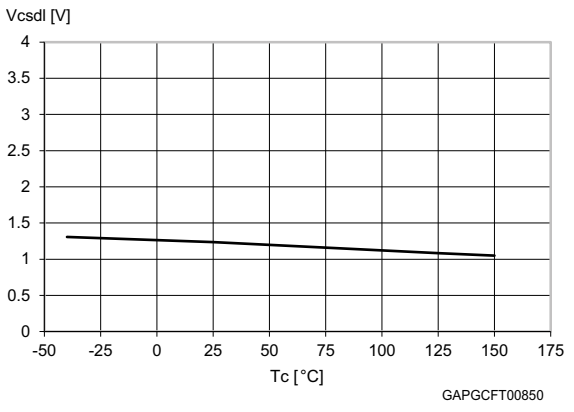
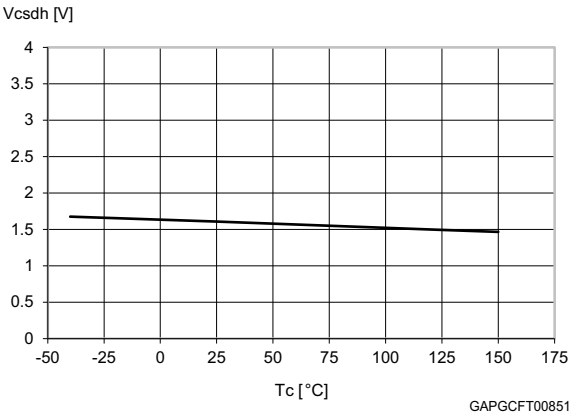
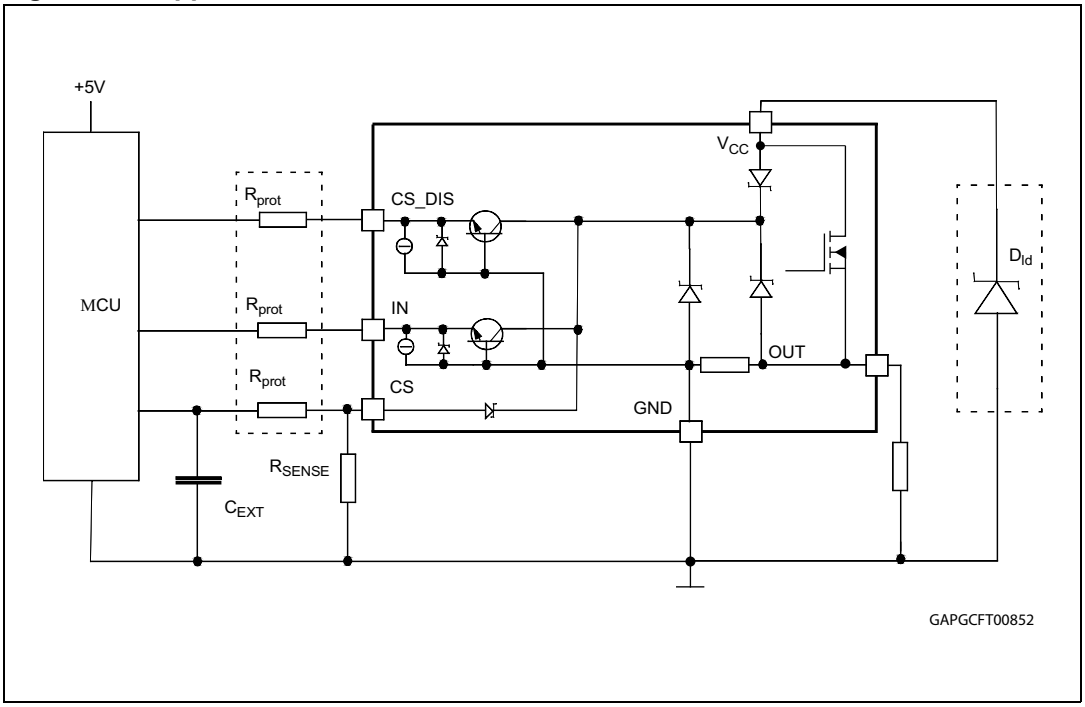


Figure 30. High-level CS_DIS voltage



3 Application information

Figure 31. Application schematic



1. Channel 2 has the same internal circuit as channel 1.

3.1 Load dump protection

D_{Id} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CCPK} max rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.2 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pins are pulled negative to approximately -1.5 V.

ST suggests the insertion of resistors (R_{prot}) in the lines to prevent the microcontroller I/O pins from latching up.

The values of these resistors provide a compromise between the leakage current of the microcontroller, the current required by the HSD I/Os (input levels compatibility) and the latch-up limit of the microcontroller I/Os.

Equation 1

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH}) / I_{IHmax}$$

Calculation example:

For V_{CCpeak} = -1.5 V; $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

$75\ \Omega \leq R_{prot} \leq 240\ k\Omega$.

Recommended values: R_{prot} =10 kΩ, C_{EXT} = 10 nF

3.3 Current sense and diagnostic

The current sense pin performs a double function (see *Figure 32: Current sense and diagnostic*):

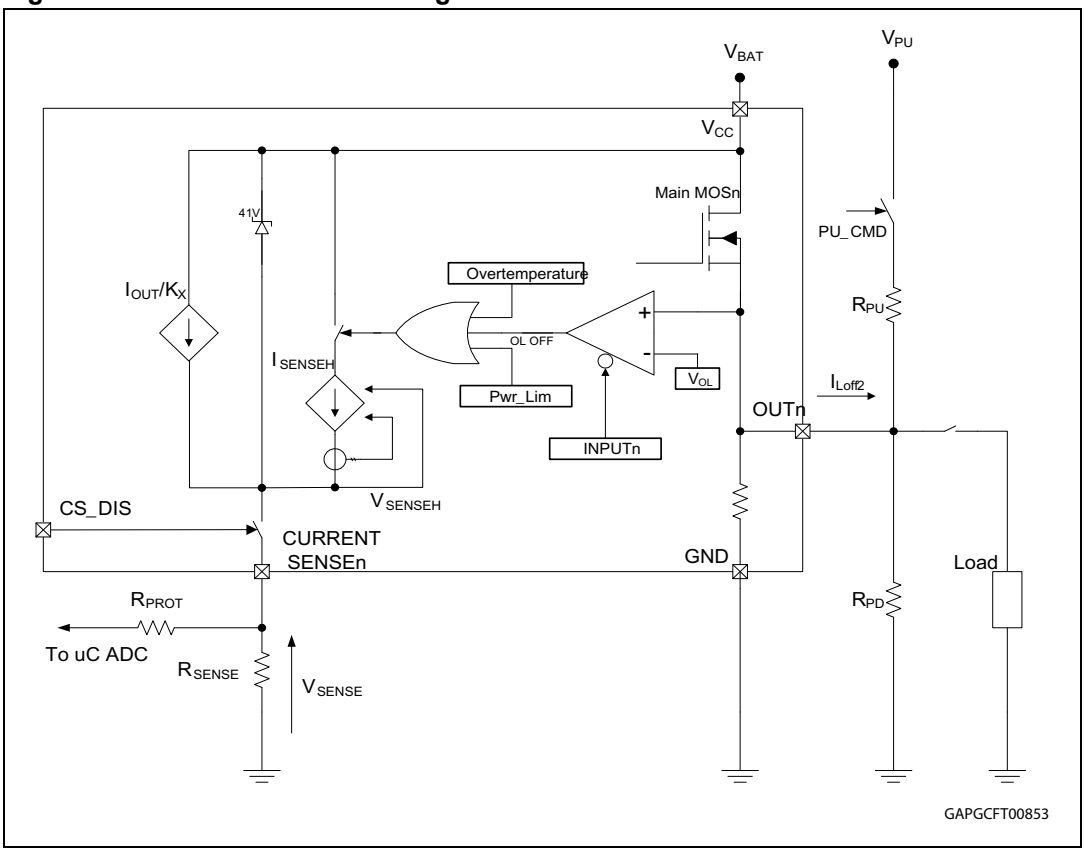
- **Current mirror of the load current in normal operation,** delivering a current proportional to the load one according to a known ratio **K_X**.
  The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE}. Linearity between I_{OUT} and V_{SENSE} is ensured up to 5 V minimum (see parameter V_{SENSE} in *Table 7: Current sense (8 V < V_{CC} < 18 V)*). The current sense accuracy depends on the output current (refer to current sense electrical characteristics *Table 7: Current sense (8 V < V_{CC} < 18 V)*).

- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to *Table 11: Truth table*):

  – Power limitation activation
  – Over temperature
  – Short to V_{CC} in off-state
  – Open-load in off-state with additional external components.

A logic level high on CS_DIS pin sets at the same time all the current sense pins of the device in a high-impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

Figure 32. Current sense and diagnostic



3.3.1 Short to V_{CC} and off-state open-load detection

Short to V_{CC}

A short-circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device OFF-state. Small or no current is delivered by the current sense during the ON-state depending on the nature of the short-circuit.

Off-state open-load with external circuitry

Detection of an open load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

An external pull-down resistor R_{PD} connected between output and GND is mandatory to avoid misdetection in case of floating outputs in off-state (see *Figure 32: Current sense and diagnostic*).

R_{PD} must be selected in order to ensure $V_{OUT} < V_{OLmin}$ unless pulled-up by the external circuitry:

Equation 2

$$V_{OUT}\big|_{Pull\text{-}up\_OFF} = R_{PD} \cdot I_{L(off2)f} < V_{OLmin} = 2V$$

$R_{PD} \leq 22\ k\Omega$ is recommended.

For proper open load detection in off-state, the external pull-up resistor must be selected according to the following formula:

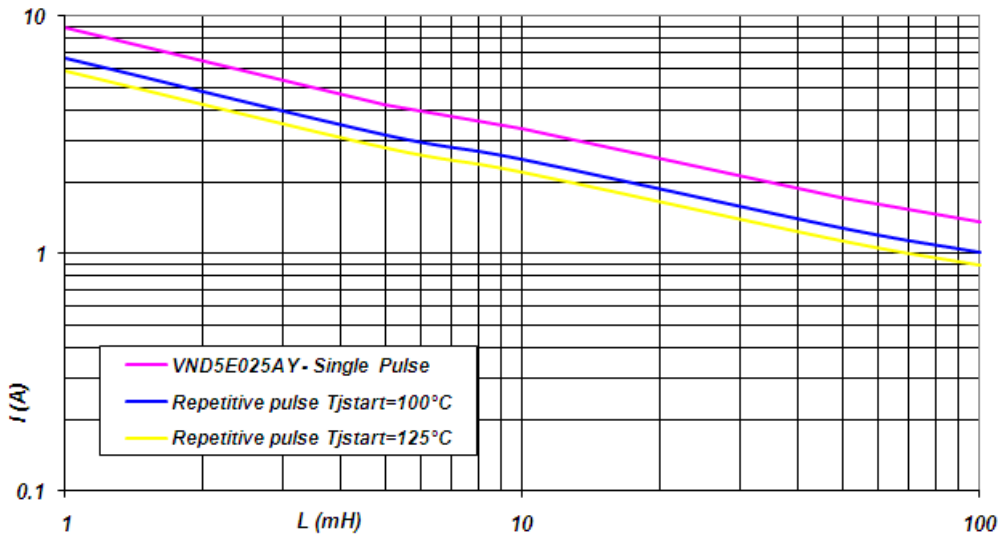
Equation 3

$$V_{OUT}\big|_{Pull\text{-}up\_ON} = \frac{(R_{PD} \cdot V_{PU}) - (R_{PU} \cdot R_{PD} \cdot I_{L(off2)r})}{(R_{PU} + R_{PD})} > V_{OLmax} = 4V$$

For the values of V_{OLmin},V_{OLmax}, $I_{L(off2)r}$ and $I_{L(off2)f}$ (see *Table 8: Open-load detection (8 V < V_{CC} < 18 V)*).

3.4 Maximum demagnetization energy (V_{CC} = 13.5 V)

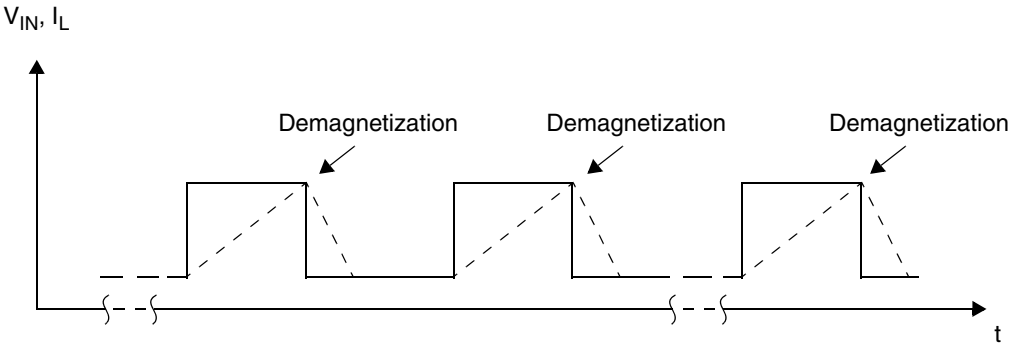
Figure 33. Maximum turn off current versus inductance



A: T_{jstart} = 150 °C single pulse

B: T_{jstart} = 100 °C repetitive pulse

C: T_{jstart} = 125 °C repetitive pulse

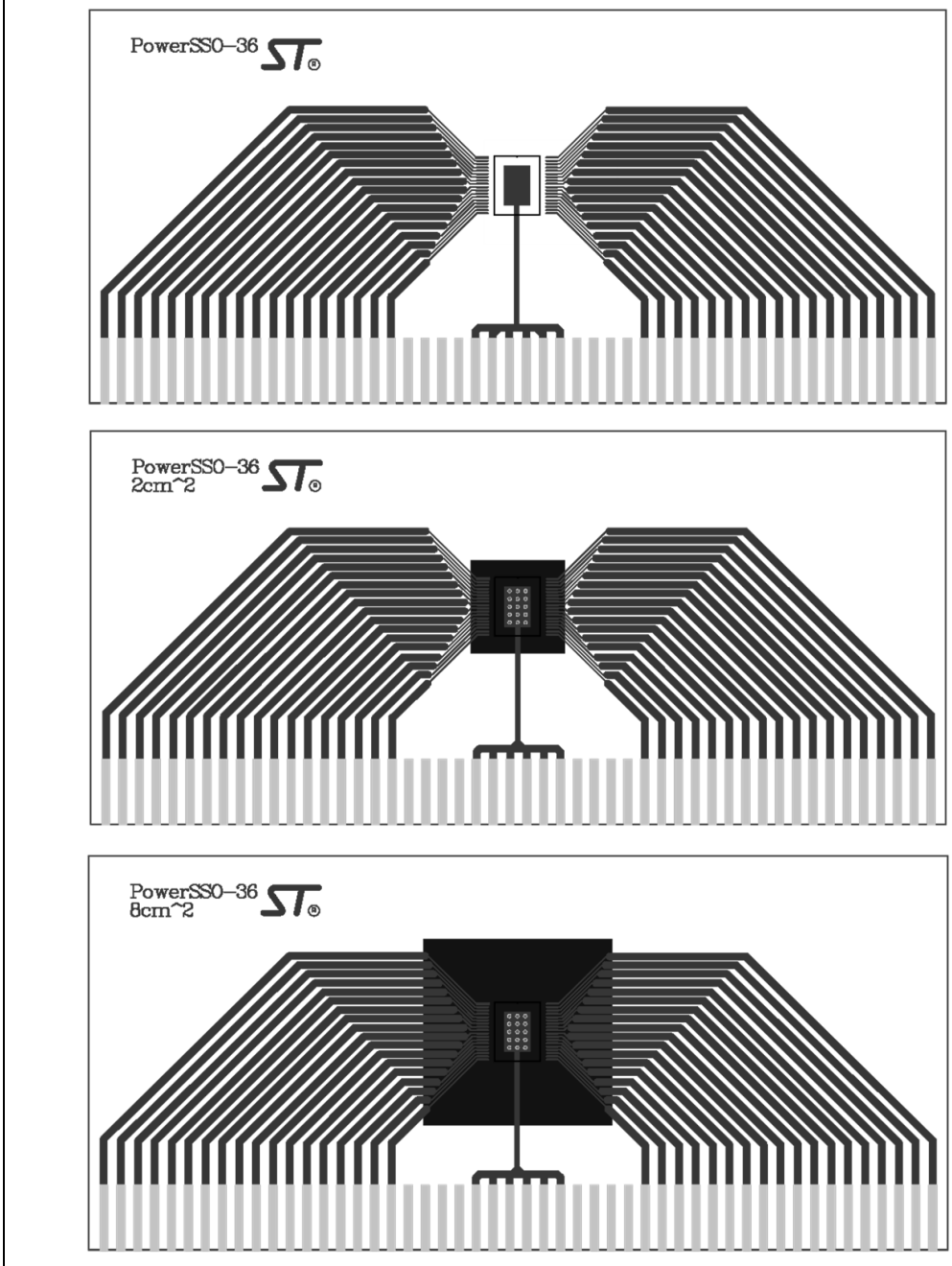


1. Values are generated with R_L = 0 Ω.
In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-36 thermal data

Figure 34. PowerSSO-36 PC board



1. Layout condition of Rth and Zth measurements (Board finish thickness 1.6 mm +/- 10%; Board double layer; Board dimension 129 mm x 60 mm; Board Material FR4; Cu thickness 0.070 mm; Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm; Footprint dimension 4.1 mm x 6.5 mm).

Figure 35. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition (one channel on)

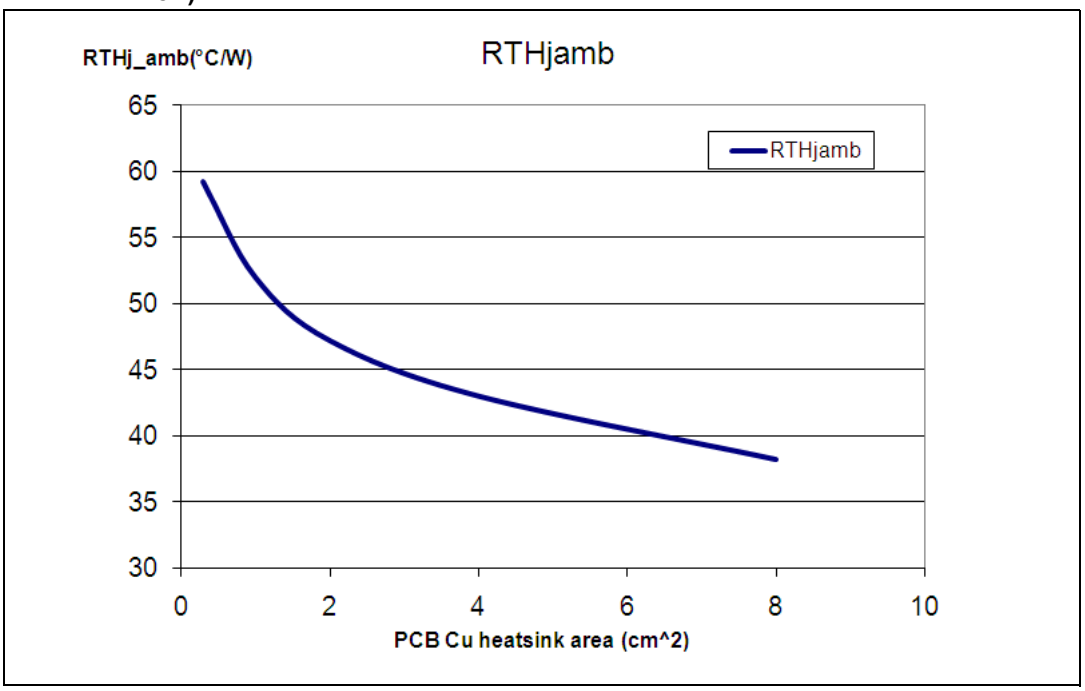
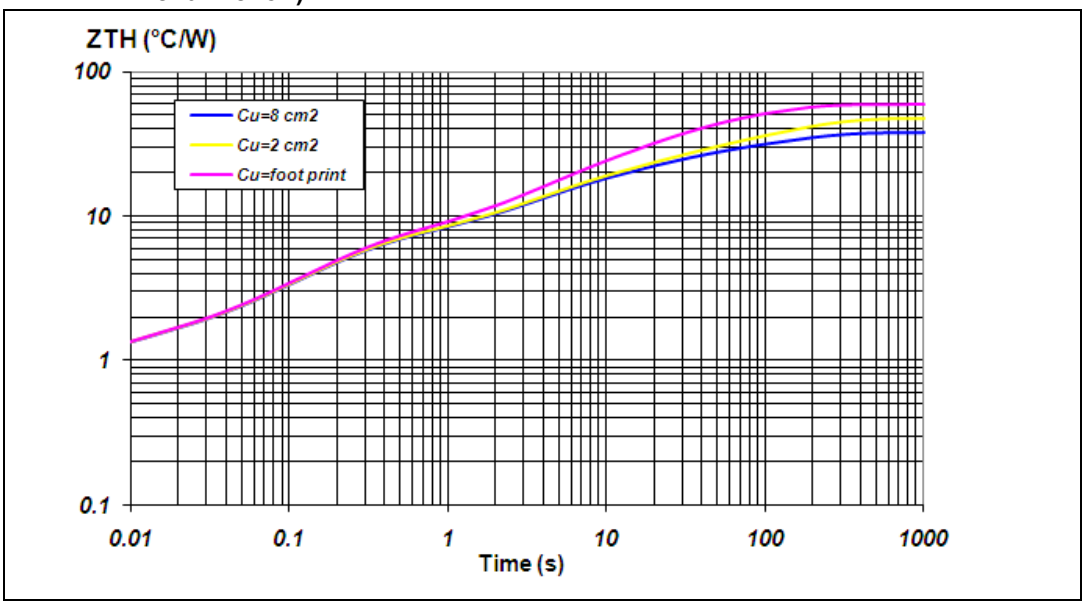


Figure 36. PowerSSO-36 thermal impedance junction ambient single pulse (one channel on)

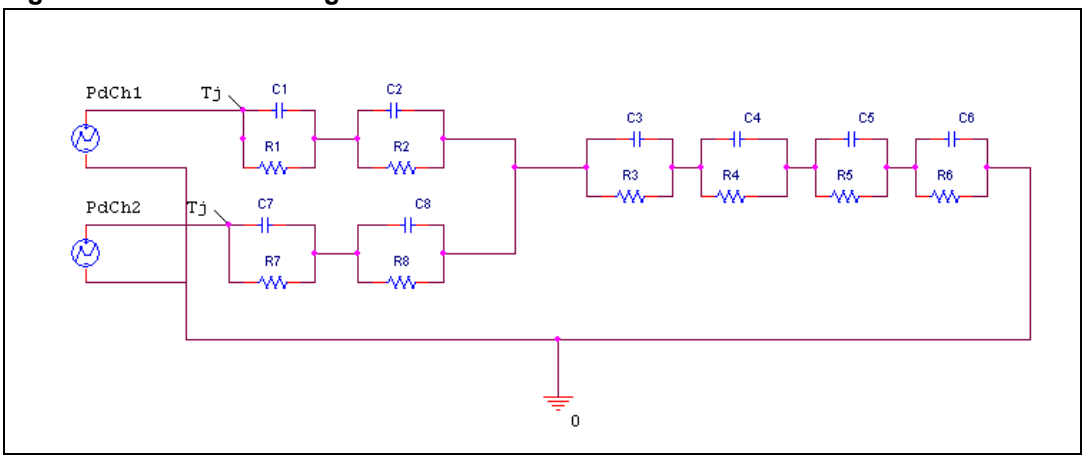


Equation 4: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 37. Thermal fitting model of a double-channel HSD in PowerSSO-36



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. Thermal parameters

Area/island (cm^2)	Footprint	2	8
R1 = R7 (°C/W)	0.3		
R2 = R8 (°C/W)	0.9		
R3 (°C/W)	5		
R4 (°C/W)	8		
R5 (°C/W)	18	10	10
R6 (°C/W)	27	23	14
C1 = C7 (W.s/°C)	0.001		
C2 = C8 (W.s/°C)	0.005		
C3 (W.s/°C)	0.04		
C4 (W.s/°C)	0.5		
C5 (W.s/°C)	1	2	2
C6 (W.s/°C)	3	6	9

5 Package information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 PowerSSO-36 mechanical data

Figure 38. PowerSSO-36 package dimensions

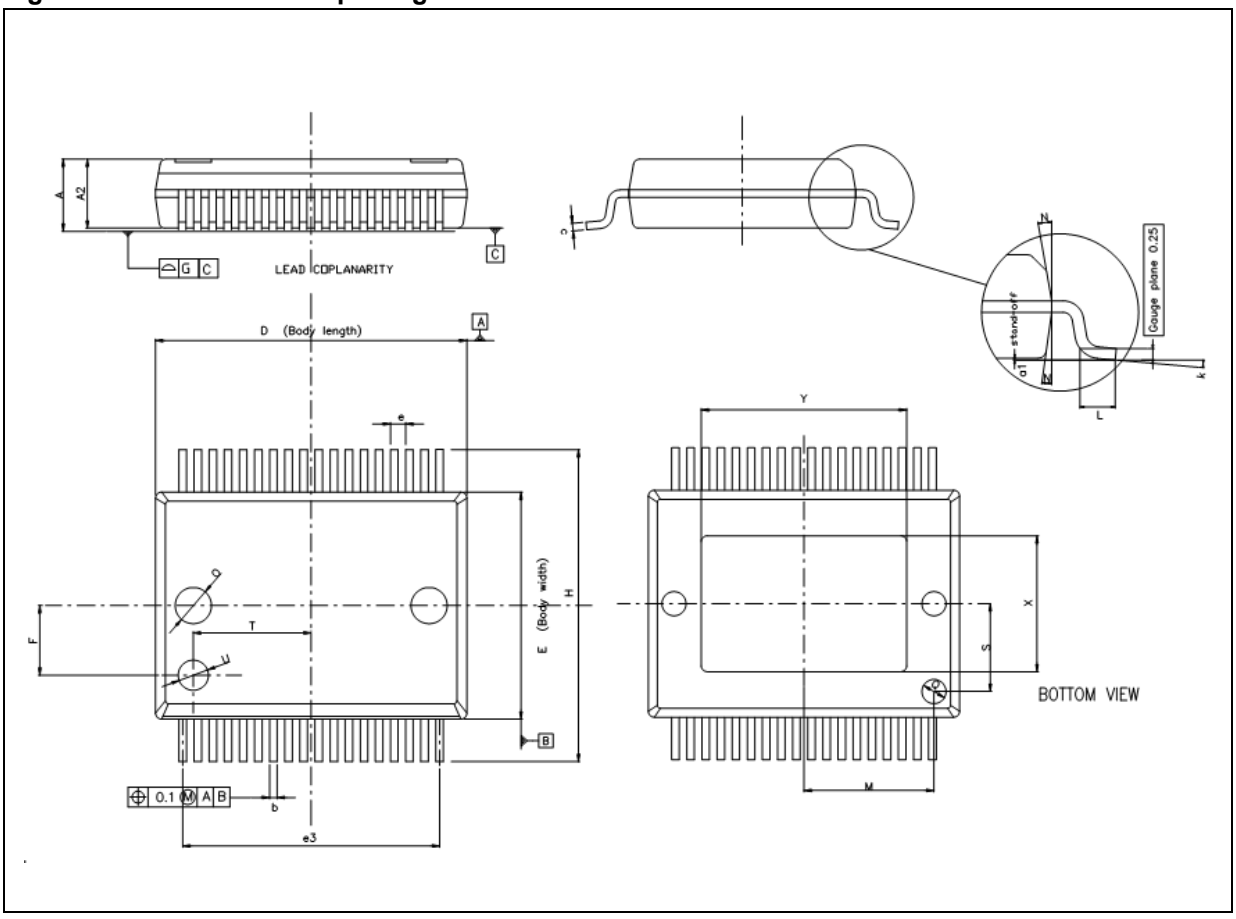


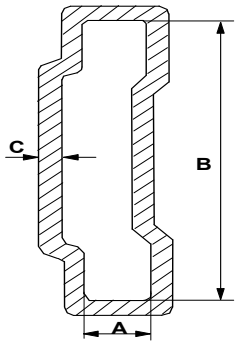
Table 16. PowerSSO-36 mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	2.15	-	2.45
A2	2.15	-	2.35
a1	0	-	0.1
b	0.18	-	0.36
c	0.23	-	0.32
D	10.10	-	10.50
E	7.4	-	7.6
e	-	0.5	-
e3	-	8.5	-
F	-	2.3	-
G	-	-	0.1
H	10.1	-	10.5
h	-	-	0.4
k	0°	-	8°
L	0.55	-	0.85
M	-	4.3	-
N	-	-	10°
O	-	1.2	
Q	-	0.8	-
S	-	2.9	-
T	-	3.65	-
U	-	1.0	-
X(1)	4.3	-	5.2
Y(1)	6.9	-	7.5

1. Corresponding to internal variation C.

5.3 Packing information

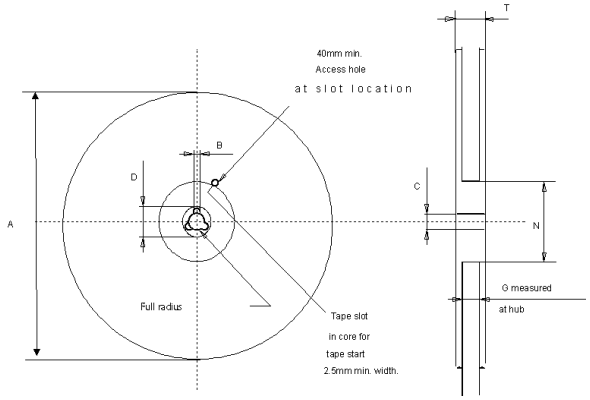
Figure 39. PowerSSO-36 tube shipment (no suffix)



Base q.ty	49
Bulk q.ty	1225
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 40. PowerSSO-36 tape and reel shipment (suffix "TR")



REEL DIMENSIONS

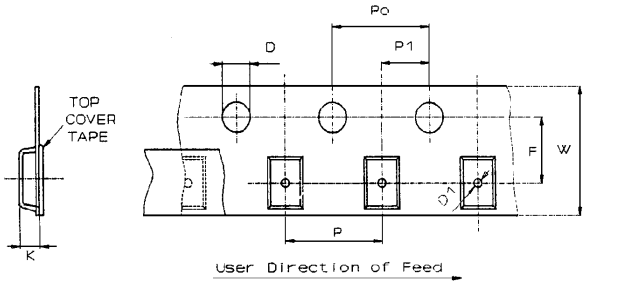
Base q.ty	1000
Bulk q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	100
T (max)	30.4

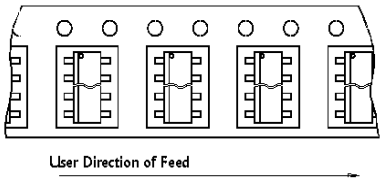
TAPE DIMENSIONS

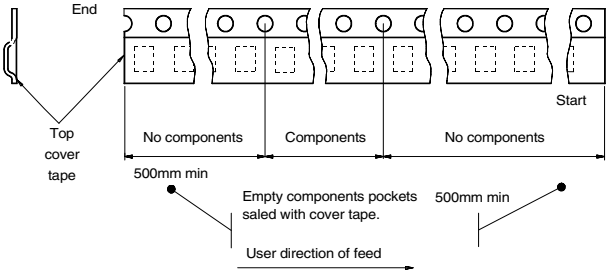
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape hole spacing	**P0 (± 0.1)**	4
Component spacing	**P**	12
Hole diameter	**D (± 0.05)**	1.55
Hole diameter	**D1 (min)**	1.5
Hole position	**F (± 0.1)**	11.5
Compartment depth	**K (max)**	2.85
Hole spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







6 Device summary

Table 17. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36	VND5E025AY-E	VND5E025AYTR-E

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
29-Jul-2010	1	Initial release.
05-Aug-2010	2	Updated following figures: – *Figure 35: $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition (one channel on)* – *Figure 36: PowerSSO-36 thermal impedance junction ambient single pulse (one channel on)* Updated *Table 15: Thermal parameters*
19-Jul-2012	3	Changed document status from “Preliminary data“ to “Production data“
19-Sep-2013	4	Updated Disclaimer

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