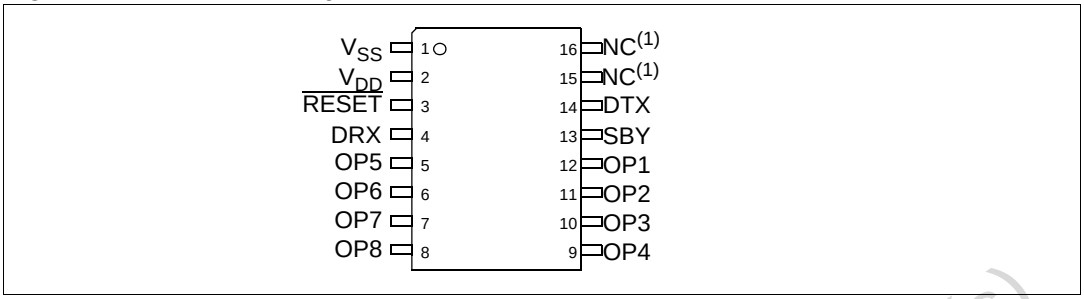
Contents

List of tables

List of figures

1 ST7LNB0V2Y0 pin description

Figure 2. SO16 narrow pinout



1. NC = not connected

See *Table 2* for a description of the pin functions.

Table 2. ST7LNB0V2Y0 pin functions

Pin number	Function name	Function description
1	Vss	Ground
2	V_{DD}	Power Supply (+5 volts)
3	$\overline{\text{RESET}}$	Reset (active low) input
4	DRX	Receive input
5	OP5	Output 5 (uncommitted port)
6	OP6	Output 6 (uncommitted port)
7	OP7	Output 7 (uncommitted port)
8	OP8	Output 8 (uncommitted port)
9	OP4	Output 4 (SO B/A)
10	OP3(1)	Output 3 (SB/SA)
11	OP2	Output 2 (H/V)
12	OP1	Output 1 (Hi/Lo)
13	SBY	Standby
14	DTX	DiSEqC™ data transmit output
15,16	-	Not used(2)

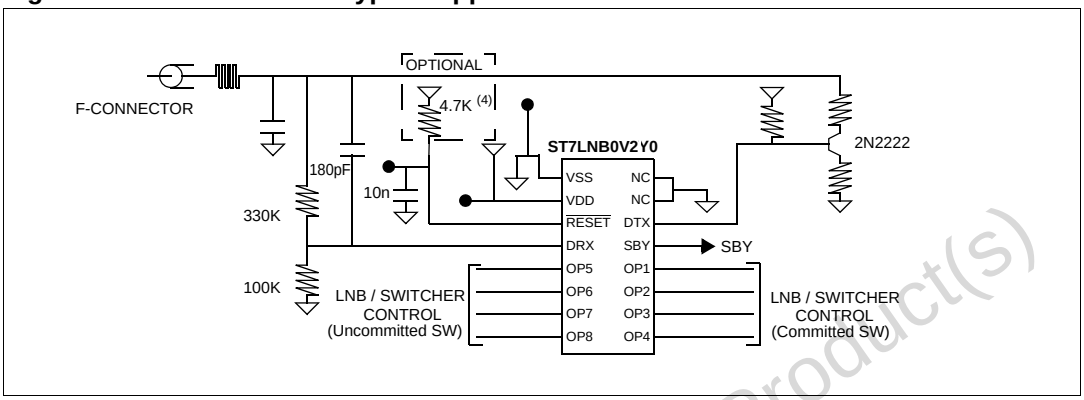
1. During normal operation this pin must be pulled-up internally or externally to avoid entering ICC mode unexpectedly during a reset. Using an external pull-up of 10 kΩ is mandatory in noisy environment. In the final application, a reset will put the pin back in input pull-up configuration even if it was configured as an output.

2. Unused pins must be tied to ground.

2 ST7LNB0V2Y0 implementation

Figure 3 shows a typical application circuit for the ST7LNB0V2Y0.

Figure 3. ST7LNB0V2Y0 typical application circuit



1. The divider chain connected to the DRX pin must have the following resistance values: 330KΩ and 100KΩ.
2. The reset circuitry linked to the $\overline{\text{RESET}}$ pin is optional. In fact the ST7LNB0V2Y0 has an internal voltage level detector (LVD) which generates a static reset when the V_{DD} supply is below a threshold voltage of 4.1 V.
3. The DiSEqC signalling must have a tone frequency of 2 2kHz (±20%) and an amplitude exceeding 150 mV peak to peak.
4. When the LVD is enabled (default state), it is mandatory not to connect a pull-up resistor. A 10 nF pull-down capacitor is recommended to filter noise on the reset line.

3 ST7LNB0V2Y0 functional description

3.1 ST7LNB0V2Y0 configuration

Unlike the original slave microcontroller described in the *Eutelsat DiSEqC slave microcontroller specifications* version 1.0, the ST7LNB0V2Y0 does not scan the control pins in order to determine the slave configuration. Instead all configuration parameters must be programmed for each specific application, and an option list (see *Section 8: Device configuration*) must be filled-in to program the necessary options at the manufacturing stage.

The slave configuration parameters are the following:

- The DiSEqC™ slave address: 11h for an LNB, and 15h for a switcher
- The local oscillator frequency table entry numbers
- The DiSEqC™ configuration byte (refer to page 15 of *DiSEqC slave microcontroller specifications*)
- The output mode (see next paragraph)
- 22 kHz tone use in backwards compatible mode (SB/SA or Hi/Lo switching)
- Standby pin use

3.2 ST7LNB0V2Y0 switching output modes

The ST7LNB0V2Y0 has 8 pins, OP1 to OP 8 available to provide ‘TTL’ logic levels to operate switches. The switches can be are used to select various signal conditions and sources (for example horizontal polarization, or satellite position).

As listed in *Table 2*, the committed output port is composed of OP1 to OP4 and the uncommitted output port is composed of OP5 to OP8.

Depending on the application hardware, the switching control pins OP1 to OP8 may be operated differently. Three possible output modes can be configured:

3.2.1 Single polarity output mode

In this mode each pin can be controlled individually as described in *Table 3*:

Table 3. Single polarity output mode

Function name	Function description
OP4	SO B/A
OP3	SB/SA
OP2	Hor/Ver
OP1	Hi/Lo
OP5	SW5
OP6	SW6
OP7	SW7
OP8	SW8

3.2.2 Decoded output mode

This mode offers the possibility to demultiplex three adjacent committed or uncommitted control lines (Hi/Lo, SB/SA and SOB/A) in order to have a 1 of 8 demux on the output port OP1 to OP8. For more details refer to page 10 of *DiSEqC™ slave microcontroller specifications.*

It is also possible to have a 1 of 4 demux by decoding only 2 control lines, SB/SA and SO B/A for controlling a 1 of 4 switcher for example.

3.2.3 Complementary output mode

In this mode the state of the uncommitted switching output port pins is the complementary of the state of the committed output ports pins. For more details refer to page 14 of *DiSEqC™ slave microcontroller specifications.*

4 Supported DiSEqC™ commands

Table 4. ST7LNB0V2Y0 DiSEqC™ supported commands

Command number (Hex byte)	Command name	Command function
00h	RESET	Reset DiSEqC™ microcontroller
01h	clr RESET	Clear the RESET flag
02h	STANDBY	Switch peripheral power off
03h	Power on	Switch peripheral power supply off
04h	Set Cont	Set contention flag
05h	Contend	Return address only if contention flag is set
06h	Clr Cont	Clear contention flag
07h	Address	Return address unless contention flag is set
08h	Move C	Change address only if contention flag is set
09h	Move	Change address unless contention flag is set
10h	STATUS	Read STATUS register
11h	Config	Read Configuration register
14h	Group 0	Read switching state (committed port)
15h	Group 1	Read switching state (uncommitted port)
20h	Set Lo	Select the low Local oscillator frequency
21h	Set VR	Select the vertical polarization
22h	Set Pos A	Select satellite position A
23h	Set SO A	Select switch Option A
24h	Set Hi	Select the Hi local oscillator frequency
25h	Set HL	Select the Horizontal polarization
26h	Set Pos B	Select satellite position B
27h	Set SO B	Select the switch Option B
28h	Set S1 A	Select switch S1 input A
29h	Set S2 A	Select switch S2 input A
2Ah	Set S3 A	Select switch S3 input A
2Bh	Set S4 A	Select switch S4 input A
2Ch	Set S1 B	Select switch S1 input B
2Dh	Set S2 B	Select switch S2 input B
2Eh	Set S3 B	Select switch S3 input B
2Fh	Set S4B	Select switch S4 input B
38h	Write N0	Write to port group 0 (committed switches)
39h	Write N1	Write to port group 1 (uncommitted switches)

Table 4. ST7LNB0V2Y0 DiSEqC™ supported commands (continued)

Command number (Hex byte)	Command name	Command function
51h	LO	Read current L.O frequency table entry number
52h	LO Lo	Read Lo L.O frequency table entry number
53h	LO Hi	Read Hi L.O frequency table entry number

Note: After a power-on, the ST7LNB0V2Y0 responds to backwards compatible signalling (13/18 V, 22 kHz, tone burst) until a valid DiSEqC frame is detected.

A RESET command must be sent in order to return to backwards compatible mode.

5 ST7LNB0V2Y0 configuration

A dedicated DiSEqC command is implemented to configure the ST7LNB0V2Y0 to the required target application. This configuration is stored in the ST7LNB0V2Y0 embedded EEPROM location.

5.1 Command 0Fh

ST7LNB0V2Y0 devices are shipped to customers with a default parameter value. These parameters can be updated using a dedicated 0Fh DiSEqC command.

The format of this command is described in *Table 5* where “data” is the parameter value to be programmed at the “index” location as shown in *Table 8*.

Table 5. Command 0Fh

E0h	DiSEqC Slave address	0Fh	index	data

Note: The special command E0 xx 0F FF FF protects the EEPROM data from any subsequent write access (where xx is the corresponding DiSEqC Slave address).

5.2 Command 0Dh

A dedicated 0Dh command has been added to read a parameter located in EEPROM.

The format of this command is described in *Table 6* where “index” is the address of the byte to be read in EEPROM area.

Table 6. Command 0Dh

E2h	DiSEqC Slave address	0Dh	index

The format of the reply frame is given in *Table 7* where “data” is the byte read from EEPROM:

Table 7. Reply to command 0Dh

E4h	data

Timings

The time required to update a byte parameter (write followed by read operation) is 130 ms; whereas the time required to update all the parameters is about 3.5 s.

Table 8. ST7LNB0V2Y0 EEPROM parameters

index	Parameter	Description	Default Value
00	slave address	DiSEqC slave address (00 to FFh)(1)	14h
01	L.O frequencies	(2)	00h
02	Output configuration	See *Table 9*	0Ah
03	Serial / version number	user can enter a value:0000h to FFFFh	1Bh, see note 4
04			FFh

1. Besides the address defined in the EEPROM at index 00h, addresses 10h and 00h are recognized also as valid addresses.
2. L.O frequencies: Local oscillator table entry numbers.
   - High nibble: High L.O frequency
   - Low nibble: Low L.O frequency

Table 9. Output configuration byte(1)

Bit number	Bit description	Value
0	22 kHz use	0: High/Low switching 1: SB/SA switching
[1:4]	Decoded mode selection	0: mode not selected [1 to 8]: decoded mode number
5	Complementary mode selection	0: mode not selected 1: mode selected
6	2 lines decoded mode selection	0: mode not selected 1: mode selected
7	Not used	0

1. If neither the Decoded mode nor the Complementary mode is set then the Single polarity mode is selected by default.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25 °C and T_A=$T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25 °C, V_{DD}=5 V for the 4.5 V≤V_{DD}≤5.5 V voltage range. They are given only as design guidelines and are not tested.

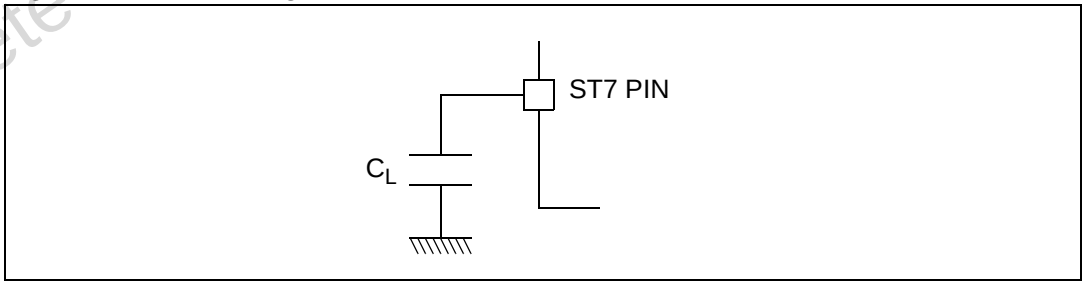
6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 4*.

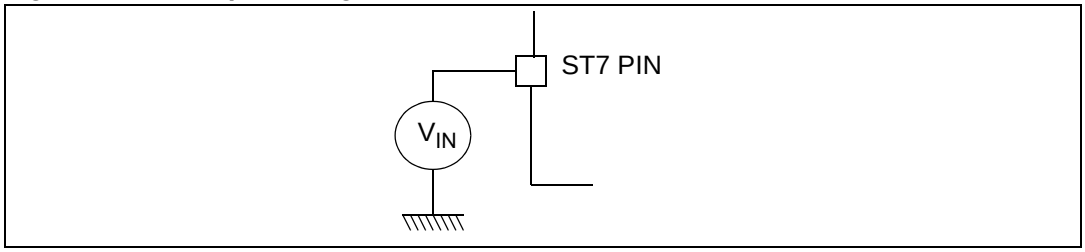
Figure 4. Pin loading conditions



6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 5*.

Figure 5. Pin input voltage



6.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 10. Voltage characteristics

Symbol	Ratings	Maximum value	Unit
V_{DD} - V_{SS}	Supply voltage	7.0	V
V_{IN}	Input voltage on any pin(1)(2)	V_{SS}-0.3 to V_{DD}+0.3	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	see *Section 6.5.3 on page 20*	
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)		

1. Directly connecting the I/O pins to V_{DD} or V_{SS} could damage the device if an unexpected change of the I/O configuration occurs (for example, due to a corrupted program counter). To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 10kΩ for I/Os). Unused I/O pins must be tied in the same way to V_{DD} or V_{SS} according to their reset configuration.
2. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.

Table 11. Current characteristics

Symbol	Ratings	Maximum value	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(1)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	100	
I_{IO}	Output current sunk by any standard I/O and control pin	25	
	Output current sunk by any high sink I/O pin	50	
	Output current source by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$(2)(3)	Injected current on $\overline{RESET}$ pin	± 5	
	Injected current on any other pin(4)(5)	± 5	
$\Sigma I_{INJ(PIN)}$ 2)	Total injected current (sum of all I/O and control pins)(4)	± 20	

1. All power (V_{DD}) and ground (V_{SS}) lines must always be connected to the external supply.
2. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
3. Negative injection disturbs the analog performance of the device. In particular, it induces leakage currents throughout the device including the analog inputs. To avoid undesirable effects on the analog functions, care must be taken:
   - Analog input pins must have a negative injection less than 0.8 mA (assuming that the impedance of the analog voltage is lower than the specified limits)
   - Pure digital pins must have a negative injection less than 1.6 mA. In addition, it is recommended to inject the current as far as possible from the analog input pins.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.
5. True open drain I/O port pins do not accept positive injection.

Table 12. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature (see *Section 7.2: Thermal characteristics*)		

6.3 Operating conditions

Table 13. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		4.5	5.5	V
T_A	Ambient temperature		-40	+85	°C

Table 14. Operating conditions with low voltage detector (LVD)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IT+(LVD)}$	Reset release threshold (V_{DD} rise)		4.00	4.25	4.50	V
$V_{IT-(LVD)}$	Reset generation threshold (V_{DD} fall)		3.80	4.10	4.30	
V_{hys}	LVD voltage threshold hysteresis	$V_{IT+(LVD)}$-$V_{IT-(LVD)}$		200		mV
Vt_{POR}	V_{DD} rise time rate(1)		20		20000	µs/V
$t_{g(VDD)}$	Filtered glitch delay on V_{DD}	Not detected by the LVD			150	ns
$I_{DD(LVD)}$	LVD/AVD current consumption			200		µA

1. Not tested in production. The V_{DD} rise time rate condition is needed to ensure a correct device power-on and LVD reset. When the V_{DD} slope is outside these values, the LVD may not ensure a proper reset of the MCU.

Table 15. Operating conditions with the DiSEqC™ signalling

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DiSEqC}	DiSEqC™ tone frequency		17.6	22	26.4	kHz
V_{DiSEqC}	DiSEqC™ tone voltage		150	650		mV_{PP}
$V_{Backward}$	13/18 volt backward compatibility voltage threshold(1)			15		V

1. In backwards compatible mode, bus DC voltage is compared with 15 V. If it exceeds this voltage then it is considered as 18 V else it is considered as 13 V.

6.4 Supply current characteristics

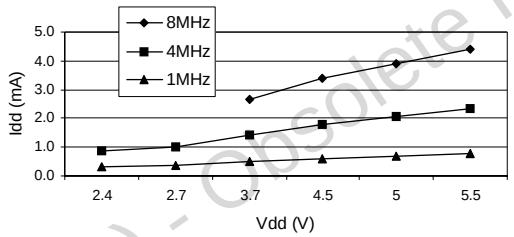
The following current consumption specified for the ST7 functional operating modes over temperature range does not take into account the clock source current consumption. To get the total device consumption, the two current values must be added.

Table 16. Supply current(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{DD}	Supply current in Run mode(2)	V_{DD}=5.5V, f_{CPU}=8MHz	4.50	7	mA
	Supply current for LNB or switcher applications(3)			20	

1. T_A = -40 to +125 °C unless otherwise specified.
2. CPU running with memory access, all I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load), all peripherals in reset state; clock input (CLKIN) driven by external square wave, LVD disabled.
3. Data based on typical ST7LNB0V2Y0 LNB or switcher application software running.

Figure 6. Typical I_{DD} in Run vs. f_{CPU}



6.5 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

6.5.1 Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

- Software recommendations:

  The software flowchart must include the management of runaway conditions such as:

  – Corrupted program counter
  – Unexpected reset
  – Critical Data corruption (control registers...)

- Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the $\overline{\text{RESET}}$ pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 17. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=5 V, T_A=+25 °C, f_{OSC}=8 MHz conforms to IEC 1000-4-2	2B
V_{FFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{DD} pins to induce a functional disturbance	V_{DD}=5 V, T_A=+25 °C, f_{OSC}=8 MHz conforms to IEC 1000-4-4	3B

6.5.2 Electromagnetic Interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 18. EMI characteristics(1)

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{OSC}/f_{CPU}]		Unit
				1/4MHz	1/8MHz	
S_{EMI}	Peak level	V_{DD}=5 V, T_A=+25 °C, SO16 package, conforming to SAE J 1752/3	0.1 MHz to 30 MHz	8	14	dBµV
			30 MHz to 130 MHz	27	32	
			130 MHz to 1 GHz	26	28	
			SAE EMI Level	3.5	4	-

1. Data based on characterization results, not tested in production.

6.5.3 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard.

Table 19. Absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=+25 °C	4000	V

1. Data based on characterization results, not tested in production.

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU**: Electrostatic discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Table 20. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A=+25 °C	A
DLU	Dynamic latch-up class	V_{DD}=5.5 V, f_{OSC}=4 MHz, T_A=+25 °C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

6.6 I/O port characteristics

6.6.1 General characteristics

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Table 21. General characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage				$0.3V_{DD}$	V
V_{IH}	Input high level voltage		$0.7V_{DD}$			
V_{hys}	Schmitt trigger voltage hysteresis(1)			400		mV
I_L	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	µA
I_S	Static current consumption(2)	Floating input mode			200	
R_{PU}	Weak pull-up equivalent resistor(3)	$V_{IN} = V_{SS}$, V_{DD} = 5 V	50	120	250	kΩ
C_{IO}	I/O pin capacitance			5		pF
$t_{f(IO)out}$	Output high to low level fall time(1)	C_L = 50 pF Between 10% and 90%		25		ns
$t_{r(IO)out}$	Output low to high level rise time(1)			25		

1. Data based on characterization results, not tested in production.
2. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor (see *Figure 7*). Data based on design simulation and/or technology characteristics, not tested in production.
3. The R_{PU} pull-up equivalent resistor is based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 8*).

Figure 7. Two typical applications with unused I/O pin

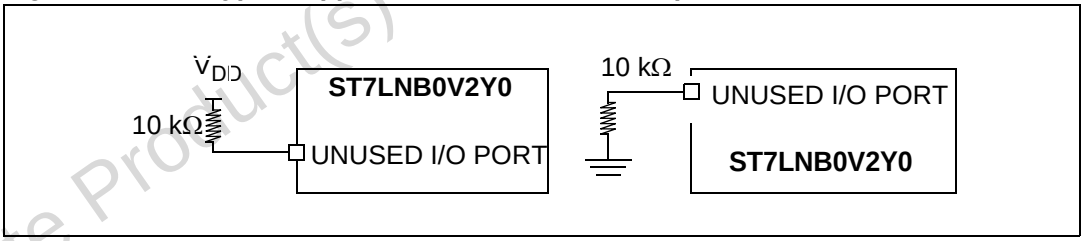
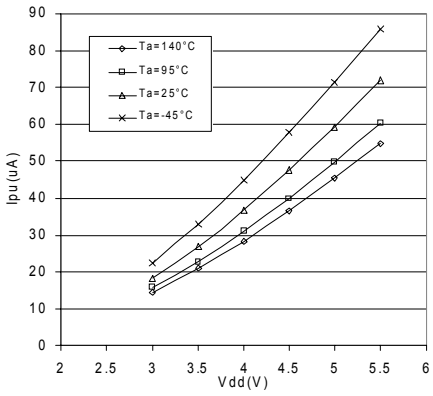


Figure 8. Typical I_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$



6.6.2 Output driving current

Subject to general operating conditions for V_{DD}, f_{CPU}, and T_A unless otherwise specified.

Table 22. Output driving current characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time (see *Figure 9*)	V_{DD}=5V	I_{IO}=+5 mA		1.0	V
			I_{IO}=+2 mA		0.4	
	Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time (see *Figure 10*)		I_{IO}=+20 mA		1.3	
			I_{IO}=+8 mA		0.75	
V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time (see *Figure 11*)		I_{IO}=-5 mA	V_{DD}-1.5		
			I_{IO}=-2 mA	V_{DD}-0.8		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section Table 11.* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Section Table 11.* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}. True open drain I/O pins does not have V_{OH}.

Figure 9. Typical V_{OL} at V_{DD}=5 V (standard)

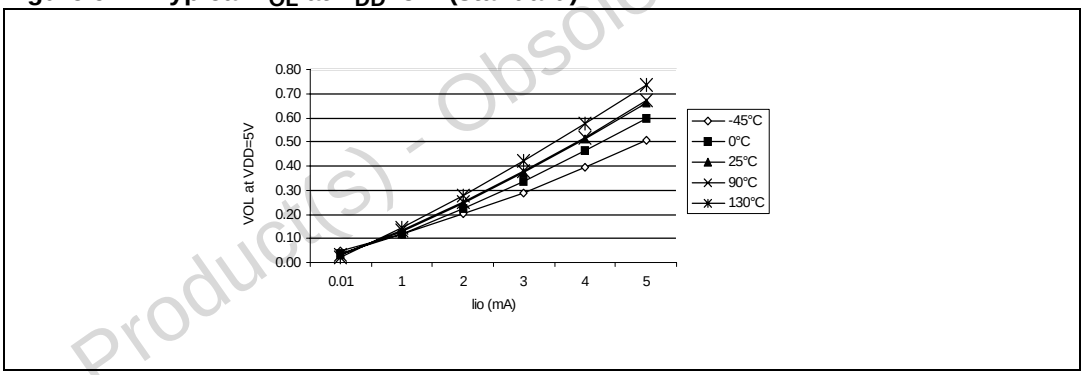


Figure 10. Typical V_{OL} at V_{DD}=5 V (high-sink)

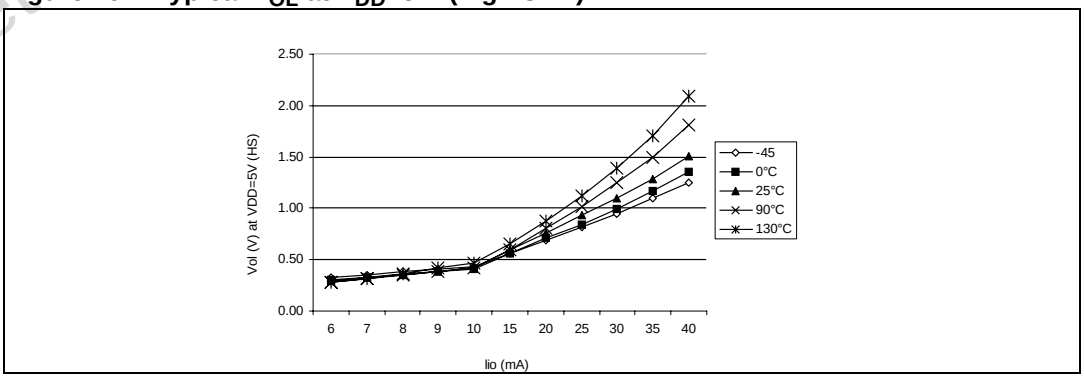
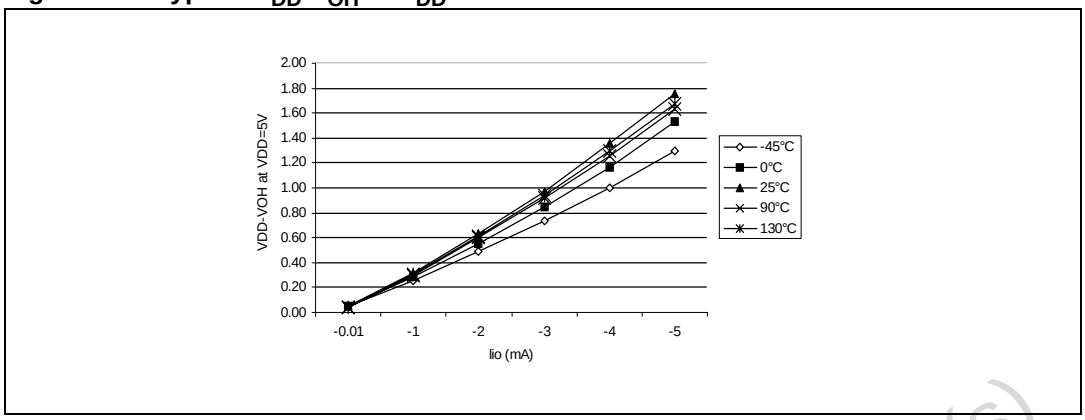


Figure 11. Typical V_{DD}-V_{OH} at V_{DD}=5 V



6.7 Control pin characteristics

Table 23. Asynchronous $\overline{\text{RESET}}$ pin(1)(2)(3)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	Input low level voltage					$0.3V_{DD}$	V
V_{IH}	Input high level voltage			$0.7V_{DD}$			
V_{hys}	Schmitt trigger voltage hysteresis(4)				1		V
V_{OL}	Output low level voltage(5)	V_{DD}=5 V	I_{IO}=+5 mA		0.5	1.0	V
			I_{IO}=+2 mA		0.2	0.4	
R_{ON}	Pull-up equivalent resistor (6)(4)	V_{DD}=5 V		20	40	80	kΩ
$t_{w(RSTL)out}$	Generated reset pulse duration	Internal reset sources			30		µs
$t_{h(RSTL)in}$	External reset pulse hold time(7)			20			µs
$t_{g(RSTL)in}$	Filtered glitch duration(8)				200		ns

1. The output of the external reset circuit must have an open-drain output to drive the ST7 reset pad. Otherwise the device can be damaged when the ST7 generates an internal reset (LVD or watchdog).
2. Whatever the reset source is (internal or external), the user must ensure that the level on the $\overline{\text{RESET}}$ pin can go below the V_{IL} max. level specified in *Section Table 23. on page 24*. Otherwise the reset will not be taken into account internally.
3. Because the reset circuit is designed to allow the internal RESET to be output in the $\overline{\text{RESET}}$ pin, the user must ensure that the current sunk on the $\overline{\text{RESET}}$ pin (by an external pull-up for example) is less than the absolute maximum value specified for $I_{INJ(RESET)}$ in *Section Table 11. on page 16*.
4. Data based on characterization results, not tested in production.
5. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section Table 11.* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
6. The R_{ON} pull-up equivalent resistor is based on a resistive transistor. Specified for voltage on $\overline{\text{RESET}}$ pin between V_{ILmax} and V_{DD}
7. 4. To guarantee the reset of the device, a minimum pulse has to be applied to the $\overline{\text{RESET}}$ pin. All short pulses applied on $\overline{\text{RESET}}$ pin with a duration below $t_{h(RSTL)in}$ can be ignored.
8. The reset network protects the device against parasitic resets.

7 Package characteristics

7.1 Package mechanical data

Figure 12. Pin plastic small outline package, 150-mil width, package outline

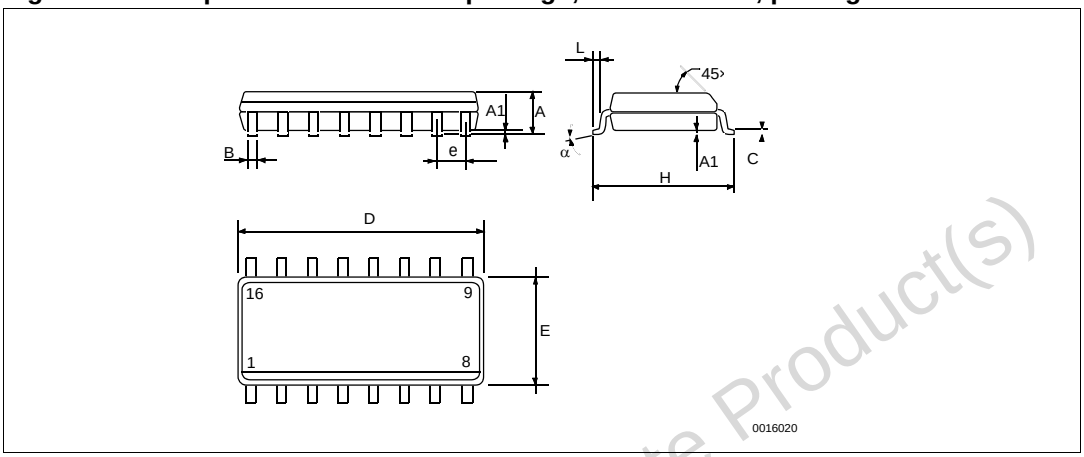


Table 24. Pin plastic small outline package, 150-mil width, mechanical data

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	9.80		10.00	0.386		0.394
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
α	0°		8°	0°		8°
L	0.40		1.27	0.016		0.050
	Number of pins					
N	16					

7.2 Thermal characteristics

Table 25. Thermal characteristics

Symbol	Ratings	Value	Unit
R_{thJA}	Package thermal resistance (junction to ambient)	85	°C/W
T_{Jmax}	Maximum junction temperature(1)	150	°C
P_{Dmax}	Power dissipation(2)	300	mW

1. The maximum chip-junction temperature is based on technology characteristics.
2. The maximum power dissipation is obtained from the formula $P_D = (T_J - T_A) / R_{thJA}$.
The power dissipation of an application can be defined by the user with the formula: $P_D=P_{INT}+P_{PORT}$ where P_{INT} is the chip internal power ($I_{DD}xV_{DD}$) and P_{PORT} is the port power dissipation depending on the ports used in the application.

7.3 Soldering information

In order to meet environmental requirements, ST offers the ST7LNB0V2Y0 in ECOPACK® package. The package have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*, together with specific technical application notes covering the main technical aspects related to lead-free conversion (AN2033, AN2034, AN2035, AN2036).

Backward and forward compatibility

The main difference between Pb and Pb-free soldering process is the temperature range.

- ECOPACK LQFP, SDIP, SO and QFN20 packages are fully compatible with Lead (Pb) containing soldering process (see application note AN2034)
- TQFP, SDIP and SO Pb-packages are compatible with Lead-free soldering process, nevertheless it's the customer's duty to verify that the Pb-packages maximum temperature (mentioned on the Inner box label) is compatible with their Lead-free soldering temperature.

Table 26. Soldering compatibility (wave and reflow soldering process)

Package	Plating material devices	Pb solder paste	Pb-free solder paste
SDIP & PDIP	Sn (pure Tin)	Yes	Yes(1)
QFN	Sn (pure Tin)	Yes	Yes(1)
LQFP and SO	NiPdAu (Nickel-palladium-Gold)	Yes	Yes(1)

1. Assemblers must verify that the Pb-package maximum temperature (mentioned on the Inner box label) is compatible with their Lead-free soldering process.

8 Device configuration

8.1 Data EEPROM option bytes

Table 27. Description of data EEPROM option bytes

Byte name	Description	Address
FAM	Device Family Address (11h:LNB; 15h: switcher)	1002h
LOFREQ	Local Oscillator Frequency Table Entry Numbers	1003h
PARAM	Output Mode and 22 kHz Tone Use (Hi/Lo or SB/SA)	1004h

FAM option byte: *Device Family Address*

11h: Normal LNB

15h: Normal Switcher

LOFREQ option byte *Local Oscillator Frequency Table Entry Number*

This byte indicates the value of a LNB local oscillator:

- Lowest Nibble = Lo Local Oscillator Frequency Table Entry Number
- Highest Nibble = Hi Local Oscillator Frequency Table Entry Number

Note: See Table 2 on page 8 of the Eutelsat DisEqC slave microcontroller specifications version 1.0.

PARAM option byte: *Output Mode and 22 kHz Tone Use (Hi/Lo or SB/SA)*

- Bit 7:8 = Not used
- Bit 6 = *Decoded Mode With Only Two Lines (*the lowest line of a selection group is kept low*)*

  0: Decoded mode with only two lines not selected

  1: Decoded mode with only two lines selected
- Bit 5 = *Complementary Mode Selection*

  0: Complementary Mode not selected
  1: Complementary Mode selected
- Bit 4:1 = *Decoded Mode Number*

  0: Decoded Mode not selected

  1 to 8: Decoded Mode Number (refer to table 5a on page 11 of the *Eutelsat DisEqC slave microcontroller speculations* version 1.0.
- Bit 0 = *22 kHz Tone Use*

  0: 22 kHz tone use for Hi/Lo switching in backwards compatible mode
  1: 22 kHz tone use for SB/SA switching in backwards compatible mode

Note: If neither a decoded mode nor a complementary output mode is selected, the output mode is the sinGle polarity output mode (refer to Table 3: Single polarity output mode).

Figure 13. Option list

ST7LNB0V2Y0 DiSEqC™ SLAVE MICROCONTROLLER OPTION LIST
(Last update: August 2007)

Customer: . . . . . .
Address: . . . . . .
. . . . . .
Contact: . . . . . .
Phone No: . . . . . .

- Package (tick one box)

ST7LNB0V2Y0M6	SO16 NARROW (16 pin)

- Family address (tick one box)

Normal LNB (11h)	[ ]
Normal Switcher (15h)	[ ]

- Backwards Compatible 22 kHz tone usage (tick one box)

Hi/Lo switching	[ ]
SB/SA switching	[ ]

- Local oscillator frequencies table entry number

Hi L.O table entry number	[ ]
Lo L.O table entry number	[ ]

- Switching output type: (tick or fill one box)

Single polarity output	[ ]
Decoded mode output (indicate the mode number)	
Complementary output	[ ]

Comments. . . . . .
. . . . . .
. . . . . .
Notes . . . . . .
. . . . . .

Date . . . . . Signature . . . . . .

Please download the latest version of this option list from: www.st.com

9 Revision history

Table 28. Document revision history

Date	Revision	Changes
	1.0	Initial release
Sep-04	2.0	First release on st.com
Dec-04	3.0	Changed note 4 and added “optional” in *Figure 3 Section Figure 3.: ST7LNB0V2Y0 typical application circuit on page 7* Added default values in *Table 8: ST7LNB0V2Y0 EEPROM parameters*
12-Oct-05	4.0	Changed package name to SO16 NARROW
03-Jan-06	5.0	Product code changed to ST7LNB0V2Y0 to reflect upgrade in firmware.
20-Sep-07	6.0	Document reformatted. Root part number ST7LNB0 changed to ST7LNB0V2Y0. Capacitor changed from 2.2 nF to 180 pF in *Figure 3: ST7LNB0V2Y0 typical application circuit*. Updated *Note 1* below *Table 15: Operating conditions with the DiSEqC™ signalling*. ECOPACK package description updated in *Section 7.3: Soldering information*. Removed note 3 below *Table 22: Output driving current characteristics*.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com