NO.EA-265-171220

APPLICATIONS

- Power source for battery-powered equipment.
- Power source for portable communication equipment
- Power source for electrical appliances such as cameras, VCRs and camcorders.
- Power source for home appliances and Notebook PC.

SELECTION GUIDE

The output voltage, the auto discharge function⁽¹⁾, and the package type for the IC can be selected at the user's request.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free	
RP132K001*-TR		5,000 per	Yes	Yes	
RP132Kxx1*-TR	DFN(PLP)1820-6	5,000 pcs	res	res	
RP132H001#-T1-FE	SOT-89-5	1.000	Yes	Yes	
RP132Hxx1#-T1-FE	301-69-5	1,000 pcs	res	res	
RP132S001#-E2-FE	HSOP-6J	1.000 peo	Yes	Yes	
RP132Sxx1*-E2-FE	ПЗОР-0J	1,000 pcs	res	res	
RP132J001#-T1-FE	TO-252-5-P2	2 000 500	Yes	Yes	
RP132Jxx1#-T1-FE	10-202-0-62	3,000 pcs	165	res	

RP132x001x is the adjustable output voltage type.

xx: The output voltage can be designated in the range from 0.8V(08) to 5.5V(55) in 0.1V step.

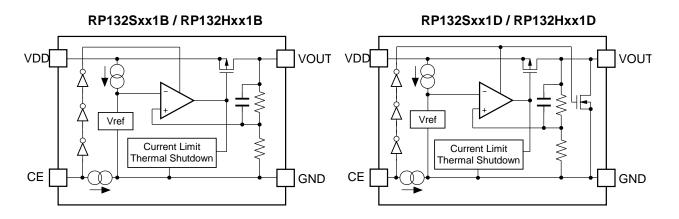
- *: The combination of the auto discharge function and delay pin (for setting inrush current limit time) are as follows.
 - B: without auto discharge function
 - D: with auto discharge function
 - E: without auto discharge function, with delay pin (for setting inrush current limit time)
 - F: with auto discharge function and delay pin (for setting inrush current limit time)
- #: The auto discharge function at off state are options as follows.
 - B: without auto discharge function at off state
 - D: with auto discharge function at off state

⁽¹⁾ Auto-discharge function quickly lowers the output voltage to 0V, when the chip enable signal is switched from the active mode to the standby mode, by releasing the electrical charge accumulated in the external capacitor.

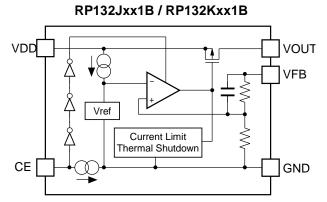
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BLOCK DIAGRAMS

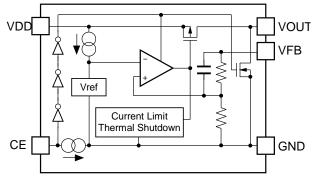
• Fixed Output Voltage Type (HSOP-6J / SOT89-5)



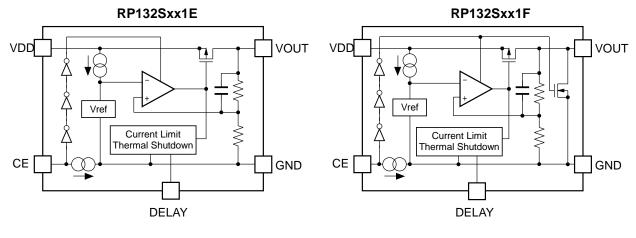
• Fixed Output Voltage Type (TO-252-5-P2 / DFN(PLP)1820-6)



RP132Jxx1D / RP132Kxx1D

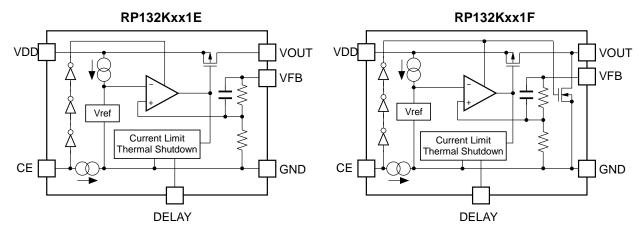


• Fixed Output Voltage Type with DELAY pin (HSOP-6J)

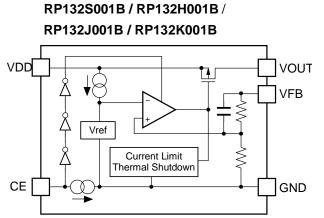


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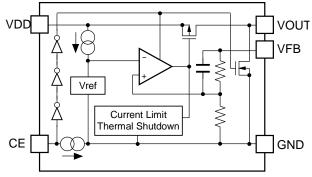
• Fixed Output Voltage Type with DELAY pin (DFN(PLP)1820-6)



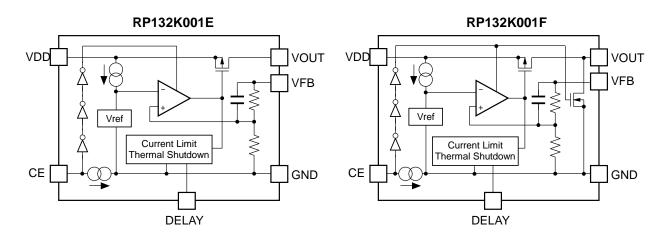
• Adjustable Output Voltage Type (HSOP-6J / SOT-89-5 / TO-252-5-P2 /DFN(PLP)1820-6)







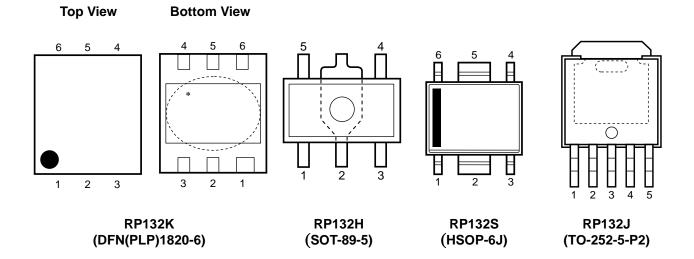
• Adjustable Output Voltage Type with DELAY pin (DFN(PLP)1820-6)



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PIN DESCRIPTIONS



RP132K⁽¹⁾ (DFN(PLP)1820-6) Pin Description

Pin No.	Symbol	Pin Description
1	VOUT	Output Pin ⁽²⁾
2	VFB	Feed Back Pin ⁽²⁾
3	GND	Ground Pin
4	CE	Chip Enable Pin ("H" Active)
F	NC	No Connection (RP132K001B/D, RP132Kxx1B/D)
5	DELAY	Delay Pin for setting inrush current limit time (RP132K001E/F, RP132Kxx1E/F)
6	VDD	Input Pin

*Tab is GND level. (They are connected to the reverse side of this IC.) The tab is better to be connected to the GND, but leaving it open is also acceptable.

⁽¹⁾ When using Adjustable Output Voltage Type (RP132K001x), please follow "Notes on the Adjustable Output Voltage Type Settings".

⁽²⁾ When using Fixed Output Voltage Type(RP132Kxx1x), the VOUT pin and the VFB pin should be connected.

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RP132H⁽¹⁾ (SOT-89-5) Pin Description

Pin No.	Symbol	Pin Description
1	CE	Chip Enable Pin ("H" Active) (RP132Hxx1B/D)
I	VFB	Feed Back Pin (RP132H001B/D)
2	GND	Ground Pin
3	NC	No Connection (RP132Hxx1B/D)
3	CE	Chip Enable Pin ("H" Active) (RP132H001B/D)
4	VDD	Input Pin
5	VOUT	Output Pin

RP132S⁽¹⁾ (HSOP-6J) Pin Description

Pin No.	Symbol	Pin Description
1	VOUT	Output Pin
2	GND	Ground Pin ⁽²⁾
	NC	No Connection (RP132Sxx1B/D)
3	VFB	Feed Back Pin (RP132S001B/D)
	DELAY	Delay Pin for setting inrush current limit time (RP132Sxx1E/F)
4	CE	Chip Enable Pin ("H" Active)
5	GND	Ground Pin ⁽²⁾
6	VDD	Input Pin

RP132J⁽¹⁾ (TO-252-5-P2) Pin Description

Pin No.	Symbol	Pin Description
1	CE	Chip Enable Pin ("H" Active)
2	VDD	Input Pin
3	GND	Ground Pin
4	VOUT	Output Pin ⁽³⁾
5	VFB	Feed Back Pin ⁽³⁾

*Tab is GND level. (They are connected to the reverse side of this IC.) The tab is better to be connected to the GND, but leaving it open is also acceptable.

⁽³⁾ When using Fixed Output Voltage Type(RP132Jxx1x),VOUT pin and VFB pin should be connected.

⁽¹⁾ When using Adjstable Output Voltage Type (RP132x001x), please follow "Notes on Adjustable Output Voltage Type Settings".

⁽²⁾ GND pins must be wired each other when mounted on boards.

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ABSOLUTE MAXIMUM RATINGS

Symbol		Rating	Unit		
Vin	Input Voltage		7.0	V	
VCE	Input Voltage (CE Pin))	-0.3 to 7.0	V	
V _{FB}	Input Voltage (VFB Pi	n)	-0.3 to 7.0	V	
Vout	Output Voltage		-0.3 to VIN+0.3	V	
		DFN(PLP)1820-6, JEDEC STD.51-7	2200		
PD	Dower Discipation(1)	SOT-89-5, JEDEC STD.51-7	2600	mW	
FD	Power Dissipation ⁽¹⁾	HSOP-6J, JEDEC STD.51-7	2700	TITVV	
		TO-252-5-P2, JEDEC STD.51-7	3800		
Tj	Junction Temperature Range		-40 to 125	°C	
Tstg	Storage Temperature Range		-55 to 125	°C	

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
Vin	Input Voltage	1.4 to 6.5	V
Та	Operating Temperature Range	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

⁽¹⁾ Refer to POWER DISSIPATION for detailed information.

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ELECTRICAL CHARACTERISTICS

 V_{IN} =Set V_{OUT} +1.0V, I_{OUT} =1mA, C_{IN} =2.2 μ F, C_{OUT} =2.2 μ F (V_{OUT} \leq 3.6V) / 4.7 μ F(V_{OUT} >3.6V) The specification in \square is checked and guaranteed by design engineering at -40°C \leq Ta \leq 85°C, unless otherwise noted.

RP132xxx1B/D(Fixed Output Voltage Type) / RP132S/Kxx1E/F(Fixed Output Voltage Type with DELAY pin) (Ta = 25°C)							
Symbol	Item	Conditi	. /	Min.	Тур.	Max.	Unit
		Ta 2500	Vout > 1.5V	×0.99		×1.01	V
		Ta = 25°C	Vouт ≤ 1.5V	-15		15	mV
Vout	Output Voltage	–40°C ≤ Ta ≤ 85°C	Vout > 1.5V	×0.981		×1.019	V
		-40 C \leq 1a \leq 65 C	Vout ≤ 1.5V	-29		29	mV
LIM	Output Current Limit			1			А
$\Delta V_{OUT}/$	Lead Devulation	0.1mA ≤ lout ≤ 300m	A		3	20	
ΔI_{OUT}	Load Regulation	0.1mA ≤ Iouт ≤ 1A			5	60	mV
V _{DIF}	Dropout Voltage	Refer	to the following "	Dropout \	/oltage"		
Iss	Supply Current	IOUT=0mA (VIN=6.5)	/)		65	85	μA
Istandby	Standby Current	V _{CE} =0V, V _{IN} =6.5V			0.15	0.60	μA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	Set V _{OUT} +0.5V ≤ V _{IN} ≤ 6.5V ∗ However, V _{IN} ≥1.6V			0.05	0.10	%/V
_	Ripple Rejection	f=1kHz	Vout ≤ 3.3V		70		
R _R		Ripple 0.2Vp-p lout=100mA	Vout > 3.3V		60	-	dB
Vin	Input Voltage			1.4		6.5	V
I _{SC}	Short Current Limit	V _{OUT} =0V			250		mA
IPD	CE Pull-down Current				0.3	0.7	μA
V _{CEH}	CE Input Voltage "H"			1.0			V
VCEL	CE Input Voltage "L"					0.4	V
en	Output Noise	BW=10Hz to 100kHz			70		µVrms
T _{TSD}	Thermal Shutdown Temperature	Junction Temperature			165		°C
T _{TSR}	Thermal Shutdown Released Temperature	Junction Temperature			95		°C
RLow	Low Output Nch Tr. ON Resistance (D/F version)	V _{IN} =4.0V, V _{CE} =0V			50		Ω
IDELAY	DELAY pin Current (DELAY pin version)	V _{IN} =4.0V		0.7	1.2	1.7	μA

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj≈Ta=25°C) except Output Noise, Ripple Rejection, Dropout Voltage at 1A Output Current and Load Regulation and Thermal Shutdown.

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The specification in \square is checked and guaranteed by design engineering at $-40^{\circ}C \le Ta \le 85^{\circ}C$, unless otherwise noted.

Dropout Voltage

(Ta = 25°C)

Output Voltage			Dropout Vo	Itage V _{DIF} (V)		
V _{оит} (V)	Condition	Тур.	Max.	Condition	Тур.	Max.
0.8 ≤ Vout < 0.9		0.67	0.89		1.20	1.54
0.9 ≤ V _{OUT} < 1.0		0.59	0.82		1.10	1.46
1.0 ≤ Vout < 1.1		0.51	0.73		1.05	1.39
1.1 ≤ Vout < 1.2	— Iолт=300mA	0.42	0.63	lou⊤=1A	0.96	1.31
1.2 ≤ Vout < 1.5	1001 =300 11A	0.36	0.54	1001=1A	0.90	1.23
1.5 ≤ Vout < 2.6		0.24	0.33		0.78	1.05
2.6 ≤ Vout < 3.3		0.15	0.21		0.52	0.72
3.3 ≤ Vout ≤ 5.5		0.13	0.18]	0.46	0.68

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 V_{IN} =Set V_{OUT} +1.0V, I_{OUT} =1mA, C_{IN} =2.2 μ F, C_{OUT} =2.2 μ F, V_{OUT} ≤ 3.6V, 4.7 μ F V_{OUT} >3.6V The specification in \square is checked and guaranteed by design engineering at $-40^{\circ}C \le Ta \le 85^{\circ}C$, unless otherwise noted.

RP132K001E/F(Adjustable Output Voltage Type with DELAY pin) (Ta = 25°C)							
Symbol	Item	Condition	ns	Min.	Тур.	Max.	Unit
Vfb	Feedback Voltage	Ta =25°C	Vout=Vfb	0.785	0.800	0.815	v
VFB	reeuback vollage	–40°C ≤ Ta ≤ 85°C	VOUTEVEB	0.771		0.829	v
V _{OUT}	Output Voltage Adjusting Range			0.8		5.5	V
I _{LIM}	Output Current Limit	$V_{OUT}=V_{FB}$		1			А
$\Delta V_{OUT}/$	Load Regulation	0.1mA ≤ I _{OUT} ≤ 300m.	A		3	20	mV
ΔI_{OUT}		$0.1 \text{mA} \le I_{\text{OUT}} \le 1 \text{A}$			5	60	111 V
V _{DIF}	Dropout Voltago	Vout=Vfb	Iout=300mA		0.67	0.89	V
V DIF	Dropout Voltage	V001=VFB	I _{OUT} =1A		1.20	1.54	v
ISS	Supply Current	Vout=Vfb, Iout=0mA	(Vin=6.5V)		65	85	μA
Istandby	Standby Current	Vce=0V, VIN=6.5V			0.15	0.60	μA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	$V_{OUT}=V_{FB}, 1.6V \le V_{IN}$	≤ 6.5V		0.05	0.10	%/V
R _R	Ripple Rejection	f=1kHz, Ripple 0.2Vp-p, I _{OUT} =100mA	Vout=Vfb		70		dB
Vin	Input Voltage			1.4		6.5	V
Isc	Short Current Limit	V _{OUT} =V _{FB} =0V			250		mA
IPD	CE Pull-down Current				0.3	0.7	μA
V _{CEH}	CE Input Voltage "H"			1.0			V
VCEL	CE Input Voltage "L"					0.4	V
en	Output Noise	BW=10Hz to 100kHz			70		μVrms
T _{TSD}	Thermal Shutdown Temperature	Junction Temperature	Э		165		°C
T _{TSR}	Thermal Shutdown Released Temperature	Junction Temperature	e		95		°C
RLOW	Low Output Nch Tr. ON Resistance (D/F version)	V _{IN} =4.0V, V _{CE} =0V			50		Ω
IDELAY	DELAY pin Current (DELAY pin version)	V _{IN} =4.0V		0.7	1.2	1.7	μA

RP132x001B/D(Adjustable Output Voltage Type) /

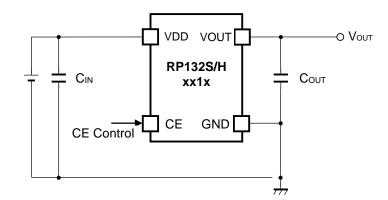
All test items listed under Electrical Characteristics are done under the pulse load condition (Tj≈Ta=25°C) except Output Noise, Ripple Rejection, Dropout Voltage at 1A Output Current and Load Regulation and Thermal Shutdown.

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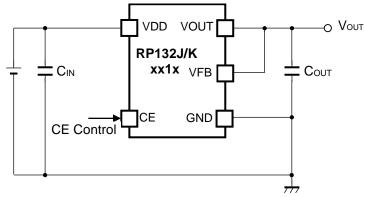
APPLICATION INFORMATION

Typical Application Circuits

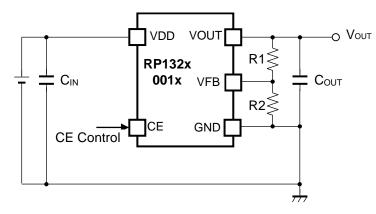
Fixed Output Voltage Type (HSOP-6J/ SOT89-5)



Fixed Output Voltage Type (TO-252-5-P2/ DFN(PLP)1820-6)

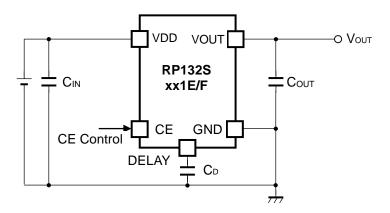


Adjustable Output Voltage Type (HSOP-6J / SOT89-5/ TO-252-5-P2 / DFN(PLP)1820-6)

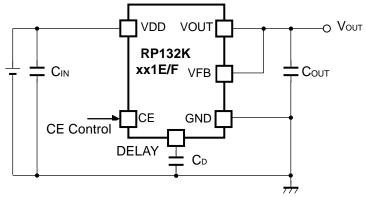


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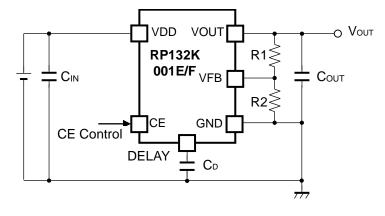
Fixed Output Voltage Type with DELAY pin (HSOP-6J)



Fixed Output Voltage Type with DELAY pin (DFN(PLP)1820-6)



Adjustable Output Voltage Type with DELAY pin (DFN(PLP)1820-6)



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Recommended					
Vout	Capacitors				
Vout ≤ 3.6V	C _{IN} (C1)	Kyocera 2.2µF (size:1005) [CM05X5R225M06A]			
vour≤ 3.0v	C _{OUT} (C2)	Kyocera 2.2µF (size:1608) [CM105X5R225K06AB]			
Vout > 3.6V	C _{IN} (C1)	Kyocera 2.2µF (size:1005) [CM05X5R225K06A]			
	С _{ОUT} (С2)	Kyocera 4.7µF (size:1608) [CM105X5R475M06AB]			

Recommended External Components

Please refer to "Technical Notes on Adjustable Output Voltage Type" when using R1 and R2 as output capacitors. Also refer to "Inrush Current Limit Time Settings" concerning with C_D .

Technical Notes on the External Components

When using this IC, consider the following points:

Phase Compensation

In this IC, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, use a 4.7μ F or more capacitor C_{OUT} between V_{OUT} pin and GND pin, and as close as possible to the pins.

If a tantalum capacitor is used, and its ESR (Equivalent Series Resistance) of C_{OUT} is large, the loop oscillation may result. Because of this, select C_{OUT} carefully considering its frequency characteristics.

PCB Layout

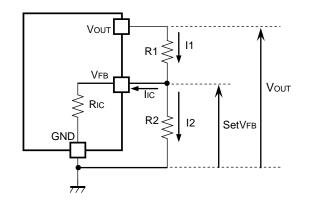
Make V_{DD} and GND lines sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect a 2.2 μ F or more capacitor C_{IN} between V_{DD} and GND pin with a capacitance value as "Recommendation value of the external capacitors" above or more, and as close as possible to the pins. Set external components, especially the output capacitor C_{OUT} , as close as possible to the IC, and make wiring as short as possible.

When using the Adjustable Output Voltage Type, the transient response could be affected by the external resistors. Evaluate the circuit taking the actual conditions of use into account.

Output Voltage Setting Method (Adjustable Output Voltage Type)

RP132x081x can be adjusted the output voltage up to 5.5V by using the external divider resistors. Also, please use $16k\Omega$ or less for R2 resistor. If the V_{FB} voltage is described as setV_{FB}, the output voltage can be set by using the following equations. SetV_{FB} is equal to 0.8V. The V_{OUT} pin of RP132x081x should be connected to the V_{FB} pin.

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	$11 = 1_{1C} + 12 \dots (1)$
Thus,	I2= setV _{FB} / R2(2)
	I1= I _{IC} + setV _{FB} /R2(3)
Therefore,	
	$V_{OUT} = setV_{FB} \times R1 \times I1 \dots (4)$
Put Equation	on (3) into Equation (4), then
	Vout = setVFB + R1(IIc + setVFB / R2)
	= setV _{FB} × (1+R1/R2) + R1 × I _{IC}
In Equation	n (5), R1x lic is the error-causing factor in Vout.
As for Ic,	
	IIC = setVFB / RIC
Therefore,	the error-causing factor R1x IIc can be described as follows.
	R1×Iıc= R1 × setV _{FB} / R _{IC}
	$= setV_{FB} \times R1 / R_{IC}(7)$
For better a	accuracy, choosing R1 (< <ric) error.<="" reduces="" td="" this=""></ric)>
Without the	e error-causing factor R1x lic, the output voltage can be calculated by the following equation
	$V_{OUT} = setV_{FB} \times ((R1 + R2) / R2)$

 R_{IC} of RP132x is approximately Typ.1.3M Ω (Ta=25°C, this value is guaranteed by design.). The value could be affected by the temperature, therefore evaluate the circuit taking the actual conditions of use into account.

Inrush Current Limit Time Settings

The RP132xSeries include the circuit which can limit the inrush current at start-up to 500mA or less. The current limit time of B/D version is fixed internally as approximately Typ.500 μ s. On the other hand, the current limit times of E/F versions are adjustable by controlling the DELAY pin value, which is the capacitance value connected between DLEAY pin and GND pin. The relation between Inrush Current Limit Time (t_D[s]) and the DELAY pin capacitance (C_D[F]) can be described in the following equation.

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 $t_D = (C_D + 70 \times 10^{-12}) \times 0.525 \times 10^6$

When not using C_D on E/F versions, DELAY pin should be open. In this case, $C_D=0$ is applied to the above equation and as a result, $37\mu s$ can be obtained. That means, when using C_D on E/F versions, the inrush current limit time will be more than $37\mu s$. Please note that during the inrush current limit time, the load current cannot be more than the limited current.

ESR vs. Output Current

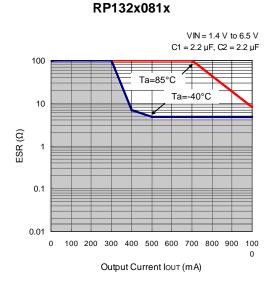
The relations between I_{OUT} (Output Current) and ESR of an output capacitor are shown below. The conditions when the white noise level is under $40\mu V$ (Avg.) are marked as the hatched area in the graph.

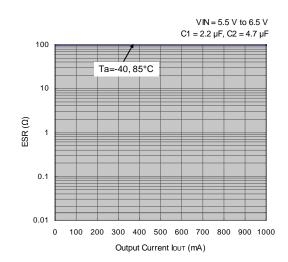
Measurement Conditions

Temperature : -40°C to 85°C

Hatched Area : Noise level is under 40μ Vms (Avg.)

- C_{IN} (C1) : 2.2μF (Kyocera CM05X5R225M06A)
- Cout (C2) : 2.2μ F (Vout = 0.8V, Kyocera CM105X5R225K06AB)
 - 4.7µF (V_{OUT} = 5.5V, Kyocera CM105X5R475M06AB)



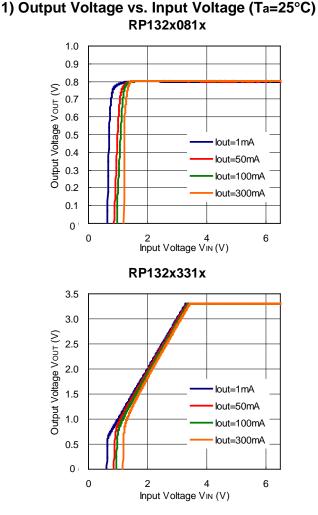


RP132x551x

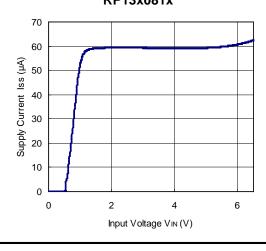
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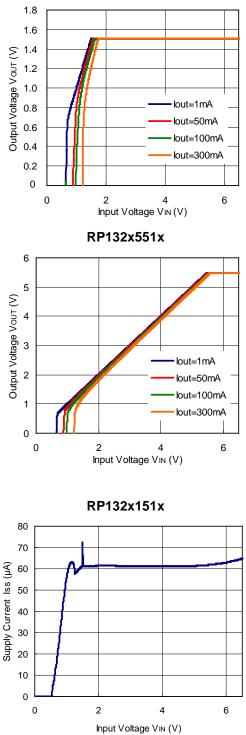
TYPICAL CHARACTERISTICS

Typical Characteristics are intended to be used as reference data; they are not guaranteed.



2) Supply Current vs. Input Voltage (Ta=25°C) RP13x081x

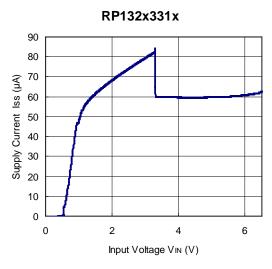


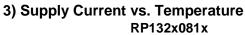


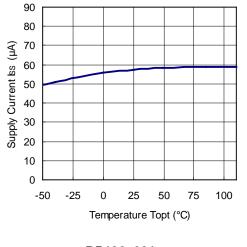
RP132x151x

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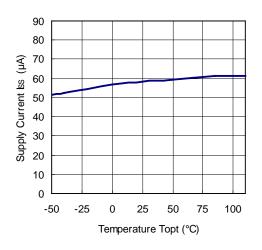
NO.EA-265-171220

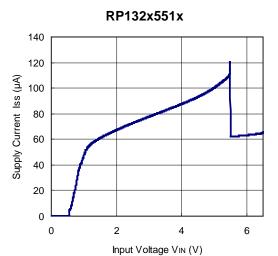




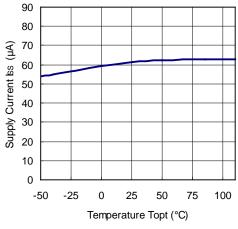




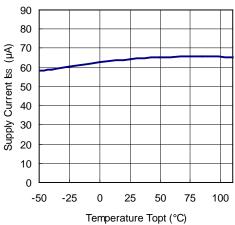


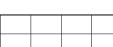








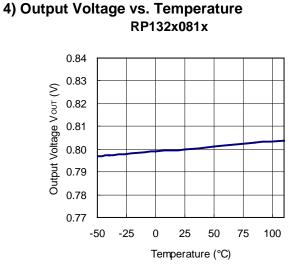




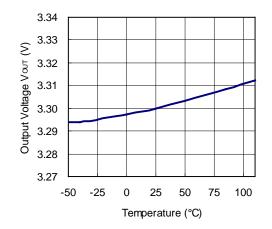




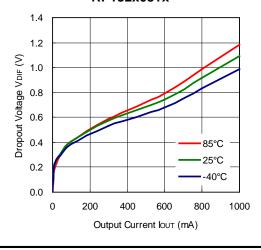
NO.EA-265-171220



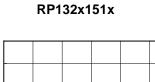
RP132x331x



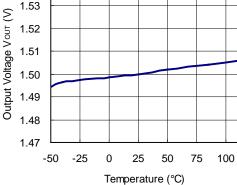




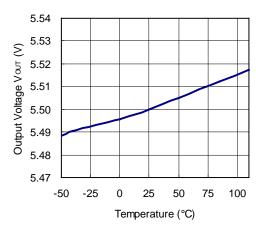
RICOH



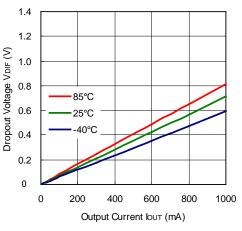
1.54









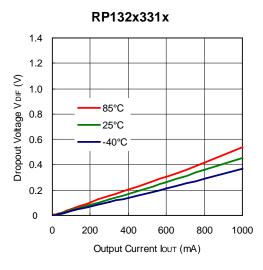


18

<u>RP132x</u>

1000

NO.EA-265-171220



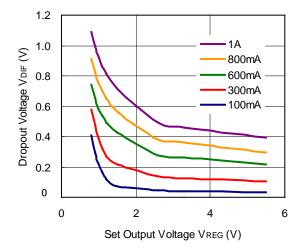
Dropout Voltage V DIF (V) 1.0 85°C 0.8 25°C 40°C 0.6 0.4 0.2 0 0 200 400 600 800 Output Current lout (mA)

1.4

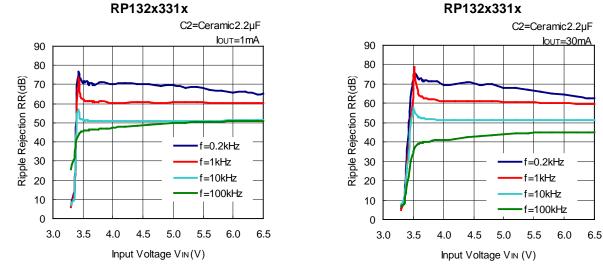
1.2

RP132x551x

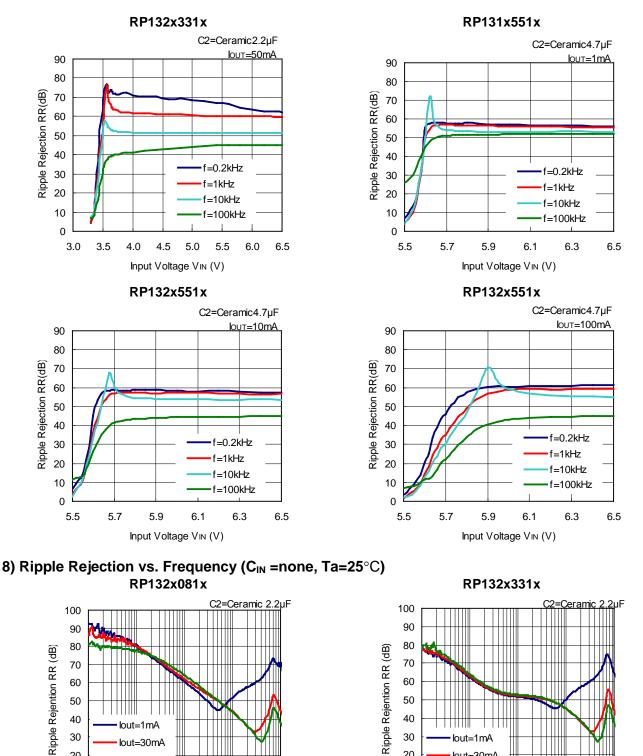
6) Dropout Voltage vs. Set Output Voltage



7) Ripple Rejection vs. Input Voltage (C_{IN}=none, Ripple=0.2Vp-p, Ta=25°C)



NO.EA-265-171220



RICOH

1000

20

10

0

0.1

lout=30mA

lout=100mA

1

1 1 1 1

10

Frequency f (kHz)

100

1000

10

Frequency f (kHz)

100

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20

20

10

0

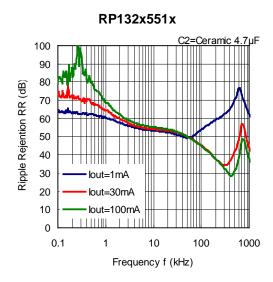
0.1

lout=100mA

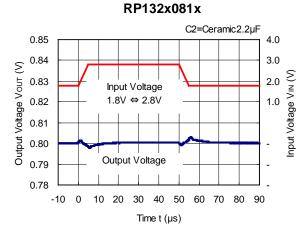
1

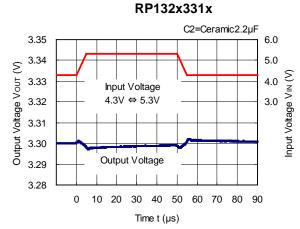
<u>RP132x</u>

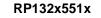
NO.EA-265-171220

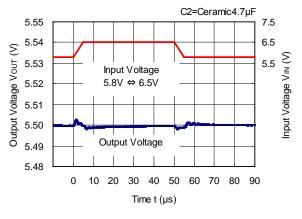


9) Input Transient Response (C_{IN} =none, I_{OUT}=100mA, tr=tf=5µs, Ta=25°C)

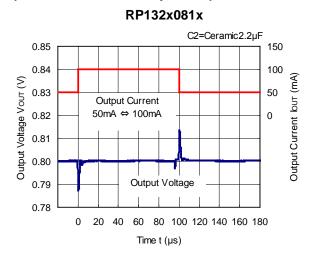




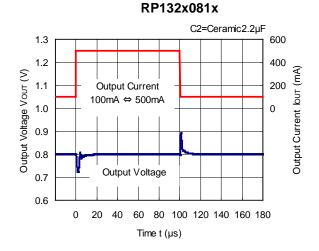




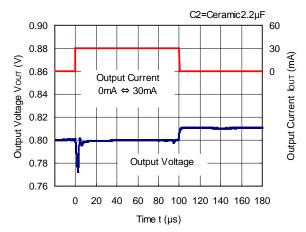
NO.EA-265-171220



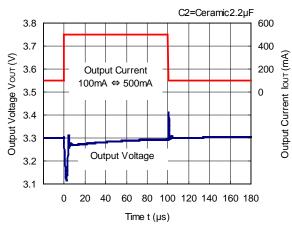
10) Load Transient Response (VIN=VOUT+1.0V, CIN =Ceramic 2.2µF, tr=tf=0.5µs, Ta=25°C)



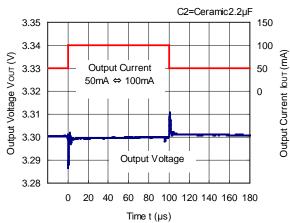




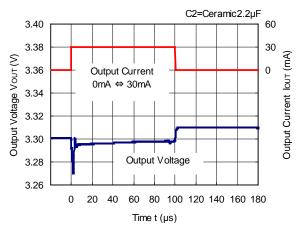








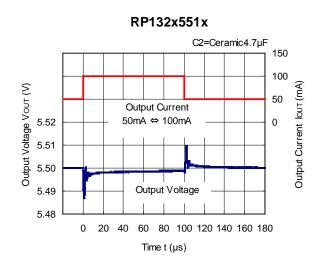


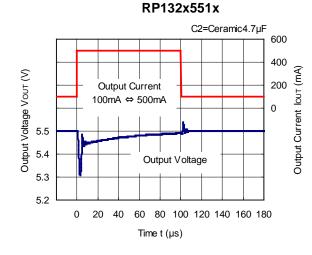


22

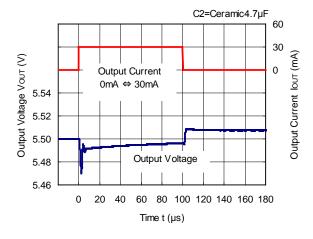
<u>RP132x</u>

NO.EA-265-171220

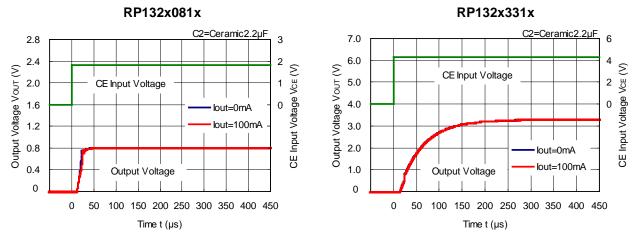




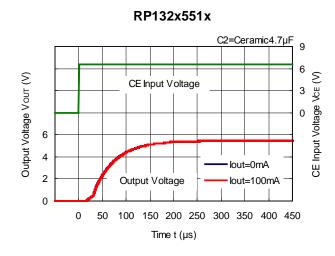
RP132x551x



11) Turn on Speed with CE pin (C_{IN} =Ceramic 2.2 μ F, Ta=25°C)

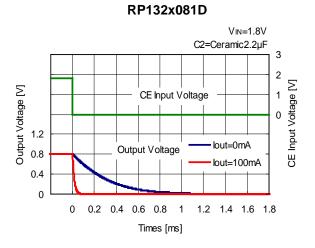


NO.EA-265-171220

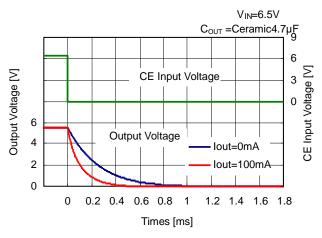


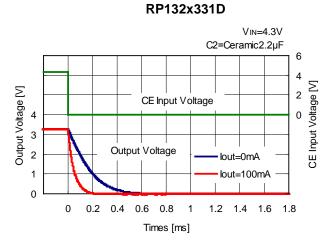


RICOH



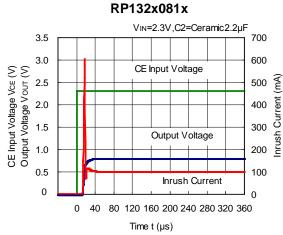






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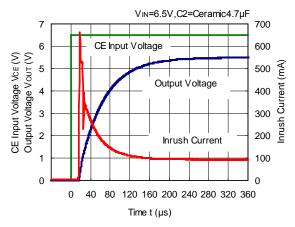
NO.EA-265-171220



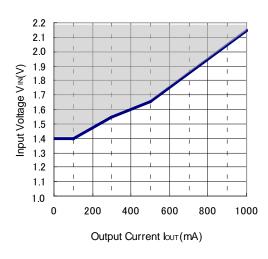
13) Inrush Current (C_{IN} =Ceramic 2.2µF, I_{OUT}=100mA, Ta=25°C)

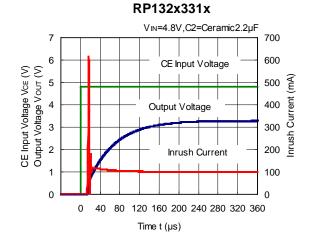
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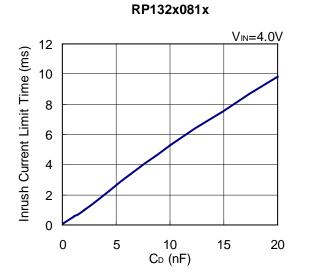






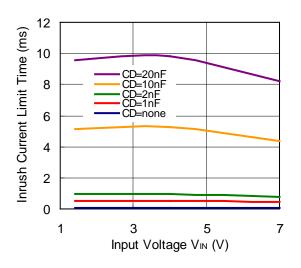
The operation rage that can output 0.8V is shown by the hatched area in the graph.

NO.EA-265-171220



15) Inrush Current Limit Time vs. C_D Capacitance (E / F Version)

16) Inrush Current Limit Time vs. Input Voltage (E / F Version) RP132x081x



POWER DISSIPATION

DFN(PLP)1820-6

(Ta = 25°C, Tjmax = 125°C)

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

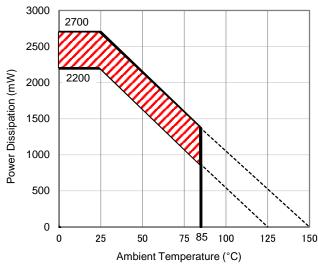
ltem	Measurement Conditions	
Environment	Mounting on Board (Wind Velocity = 0 m/s)	
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)	
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm	
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square	
Through-holes	φ 0.2 mm × 34 pcs	

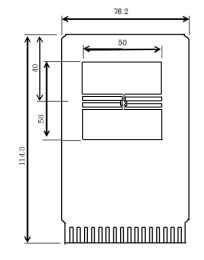
Measurement Result

Item	Measurement Result
Power Dissipation	2200 mW
Thermal Resistance (θja)	θja = 45°C/W
Thermal Characterization Parameter (wjt)	ψjt = 18°C/W

θja: Junction-to-Ambient Thermal Resistance

wit: Junction-to-Top Thermal Characterization Parameter





Power Dissipation vs. Ambient Temperature

Measurement Board Pattern

The above graph shows the power dissipation of the package at $Tjmax = 125^{\circ}C$ and $Tjmax = 150^{\circ}C$. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

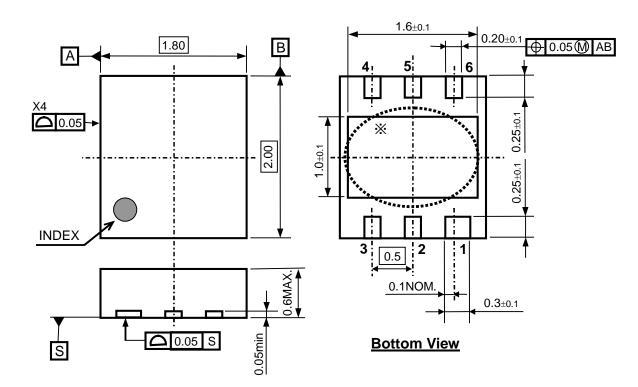
Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years

PACKAGE DIMENSIONS

DFN(PLP)1820-6

Ver. A

i



DFN(PLP)1820-6 Package Dimensions (Unit: mm)

^{*} The tab on the bottom of the package is substrate level (GND). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.



POWER DISSIPATION

SOT-89-5

(Ta = 25°C, Tjmax = 125°C)

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

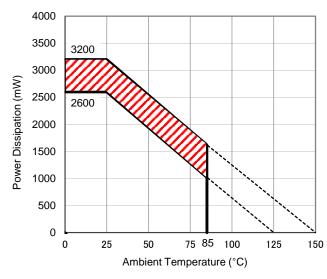
ltem	Measurement Conditions	
Environment	Mounting on Board (Wind Velocity = 0 m/s)	
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)	
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm	
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square	
Through-holes	Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square \$\oplus 0.3 mm \times 13 pcs	

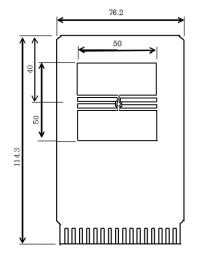
Measurement Result

Item	Measurement Result
Power Dissipation	2600 mW
Thermal Resistance (θ ja)	θja = 38°C/W
Thermal Characterization Parameter (wjt)	ψjt = 13°C/W

θja: Junction-to-Ambient Thermal Resistance

wjt: Junction-to-Top Thermal Characterization Parameter





Power Dissipation vs. Ambient Temperature

Measurement Board Pattern

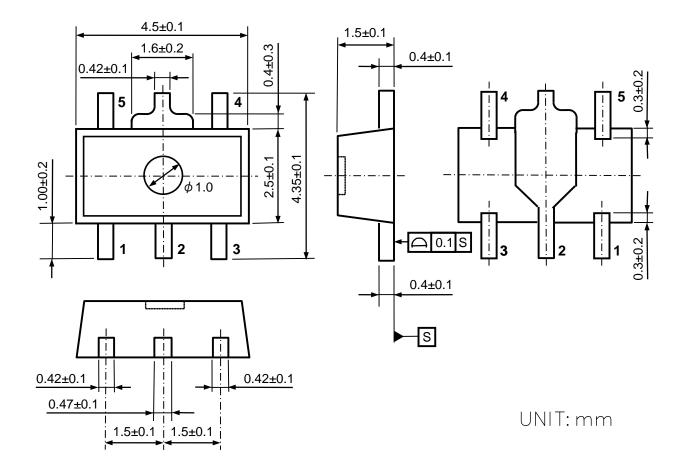
The above graph shows the power dissipation of the package at $Tjmax = 125^{\circ}C$ and $Tjmax = 150^{\circ}C$. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years

SOT-89-5

Ver. A

i



SOT-89-5 Package Dimensions

POWER DISSIPATION

HSOP-6J

(Ta = 25°C, Tjmax = 125°C)

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement	Conditions
-------------	------------

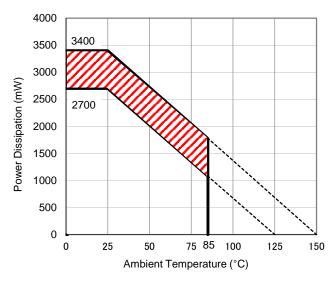
ltem	Measurement Conditions	
Environment	Mounting on Board (Wind Velocity = 0 m/s)	
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)	
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm	
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square	
Through-holes	φ 0.3 mm × 28 pcs	

Measurement Result

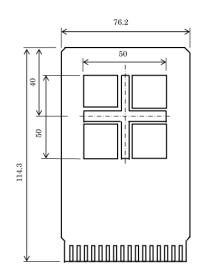
Item	Measurement Result
Power Dissipation	2700 mW
Thermal Resistance (θ ja)	θja = 37°C/W
Thermal Characterization Parameter (wjt)	ψjt = 7°C/W

θja: Junction-to-Ambient Thermal Resistance

wjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

i

The above graph shows the power dissipation of the package at $Tjmax = 125^{\circ}C$ and $Tjmax = 150^{\circ}C$. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

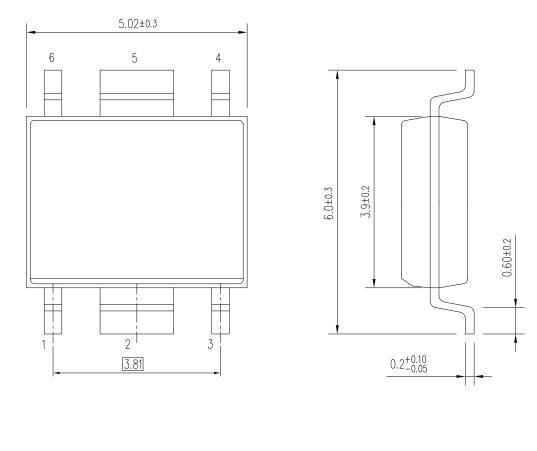
Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years

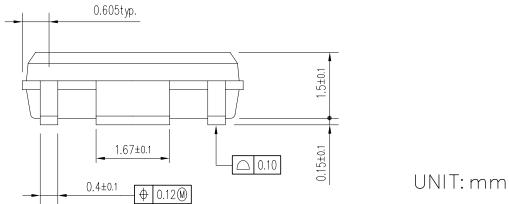
PACKAGE DIMENSIONS

HSOP-6J

Ver. A

i





HSOP-6J Package Dimensions

POWER DISSIPATION

TO-252-5

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

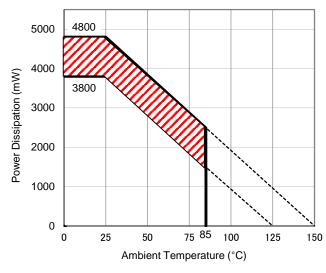
Measurement Conditions

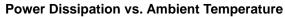
ltem	Measurement Conditions	
Environment	Mounting on Board (Wind Velocity = 0 m/s)	
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)	
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm	
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square	
Through-holes	φ 0.3 mm × 21 pcs	
Measurement Result		(Ta = 25°C, Tjmax = 125°C)
Item		Measurement Result
Power Dissipation		3800 mW
Thermal Resistance (θja)		θja = 26°C/W

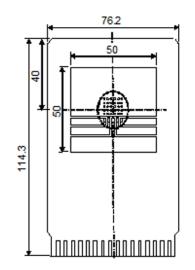
θja: Junction-to-Ambient Thermal Resistance

Thermal Characterization Parameter (wjt)

wjt: Junction-to-Top Thermal Characterization Parameter







 $\psi it = 7^{\circ}C/W$

Measurement Board Pattern

i

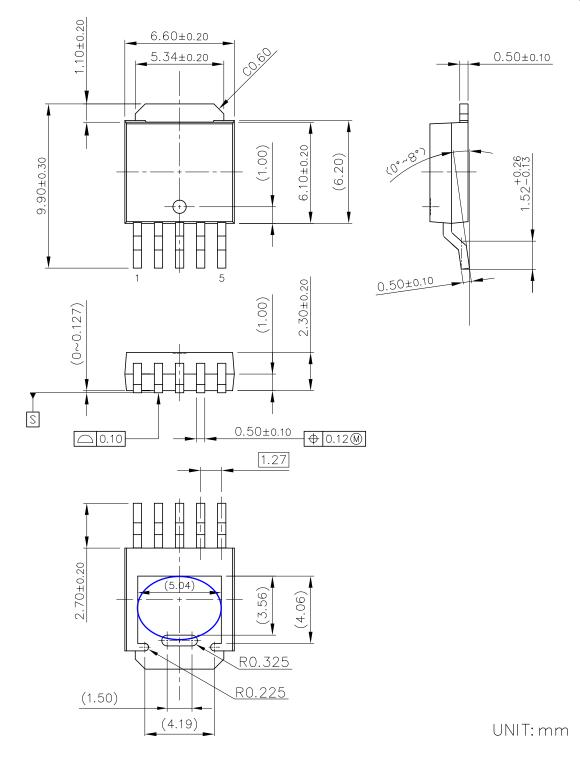
The above graph shows the power dissipation of the package at $Tjmax = 125^{\circ}C$ and $Tjmax = 150^{\circ}C$. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years

PACKAGE DIMENSIONS

TO-252-5-P2

Ver. A



TO-252-5-P2 Package Dimensions

^{*} The tab on the bottom of the package shown by blue circle is a substrate potential (GND). It is recommended that this tab be connected to the ground plane on the board but it is possible to leave the tab floating.

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