

Low-Power, Low-Glitch, Octal 12-Bit Voltage-Output DACs with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND -0.3V to +6V
 All Other Pins to GND -0.3V to (V_{DD} + 0.3V)
 Continuous Power Dissipation (T_A = +70°C)
 16-Pin TSSOP (derate 9.4mW/°C above +70°C) 775mW

Maximum Current Into Any Pin ±50mA
 Operating Temperature Range -40°C to +85°C
 Junction Temperature +150°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (soldering, 10s) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.5V, GND = 0, V_{REF} = V_{DD}, C_L = 200pF, R_L = 2kΩ, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY (Notes 1, 2)						
Resolution	N		12			Bits
Integral Nonlinearity	INL			±1	±4	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error (Note 3)	VOE			±10	±60	mV
Offset Error Temperature Coefficient				±10		μV/°C
Gain Error (Note 3)	VGE			±0.1	±1	% of FS
Gain Error Temperature Coefficient				±5		ppm/°C
REFERENCE INPUT						
Reference Input Voltage Range (Note 4)	V _{REF}		0.8		V _{DD}	V
Reference Input Impedance	R _{REFIN}		135	200	265	kΩ
Reference Current	I _{REFPD}	In power-down mode		1	10	μA
DAC OUTPUTS						
Output Voltage Range		With no load	0.020		V _{DD} - 0.020	V
DC Output Impedance				0.5		Ω
Capacitive Load	C _L			500		pF
Resistive Load	R _L			2		kΩ
Short-Circuit Current		V _{DD} = +5V		33		mA
		V _{DD} = +2.7V		20		
Wake-Up Time		From shutdown mode		24		μs

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MAX5306/MAX5307

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +2.7V$ to $+5.5V$, $GND = 0$, $V_{REF} = V_{DD}$, $C_L = 200pF$, $R_L = 2k\Omega$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{DD} = +5V$, $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, CS, LDAC, CLR-MAX5307)						
Input High Voltage	V_{IH}	$V_{DD} = +5V \pm 10\%$	2.4			V
		$V_{DD} = +3V \pm 10\%$	2.1			
Input Low Voltage	V_{IL}	$V_{DD} = +5V \pm 10\%$			0.8	V
		$V_{DD} = +3V \pm 10\%$			0.6	
Input Leakage Current	I_{IN}	All digital inputs 0 or V_{DD}		± 0.1	± 10	μA
Input Capacitance	C_{IN}			10		pF
DIGITAL OUTPUT (MAX5306)						
Output Low Voltage	V_{OL}	$I_{SINK} = 1mA$			0.5	V
Output High Voltage	V_{OH}	$I_{SOURCE} = 1mA$	$V_{DD} - 0.5$			V
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR	Positive and negative		1		V/ μs
Voltage-Output Settling Time	t_s	400hex to C00hex		5		μs
Digital Feedthrough		Code 0, all digital inputs from 0V to V_{DD}		0.5		nV/s
DAC Glitch Impulse		Major carry transition		2		nV/s
DAC Output Noise				600		μV_{p-p}
DAC to DAC Crosstalk				0.5		nV/s
POWER REQUIREMENTS						
Supply Voltage Range	V_{DD}		2.7		5.5	V
Supply Current with No Load (Note 5)	I_{DD}	All digital inputs at 0 or V_{DD} , $V_{DD} = V_{REF} = +5.5V$		1.5	1.7	mA
		All digital inputs at 0 or V_{DD} , $V_{DD} = +5.5V$, $V_{REF} = +1.2V$		1.1	1.3	
		All digital inputs at 0 or V_{DD} , $V_{DD} = V_{REF} = +3V$		1.3		
		Shutdown mode		1	10	μA

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +2.7V$ to $+5.5V$, $GND = 0$, $V_{REF} = V_{DD}$, $C_L = 200pF$, $R_L = 2k\Omega$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{DD} = +5V$, $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS						
Serial Clock Frequency	f _{SCLK}		0		15	MHz
SCLK Pulse Width High	t _{CH}		33			ns
SCLK Pulse Width Low	t _{CL}		33			ns
$\overline{CS}$ Fall to SCLK Fall Setup Time	t _{CSS}		16			ns
SCLK Fall to $\overline{CS}$ Rise Setup Time	t _{CSH}		20			ns
LDAC Pulse Width Low	t _{LDACPWL}		20			ns
$\overline{CLR}$ Pulse Width Low	t _{CLR PWL}	MAX5307 only	20			ns
DIN to SCLK Fall Setup Time	t _{DS}		16			ns
DIN to SCLK Fall Hold Time	t _{DH}		10			ns
CS Pulse Width High	t _{CSPWH}		20			ns
SCLK Rise to DOUT Fall	t _{SDL}	Load capacitance = 20pF			50	ns
SCLK Rise to DOUT Rise	t _{SDH}	Load capacitance = 20pF			50	ns

Note 1: Static accuracy tested without load.

Note 2: Linearity is tested within codes 73hex to F8Dhex.

Note 3: Gain and offset tested within codes 73hex to F8Dhex.

Note 4: Static accuracy specifications valid for $V_{REF} = 1.2V$ to V_{DD} .

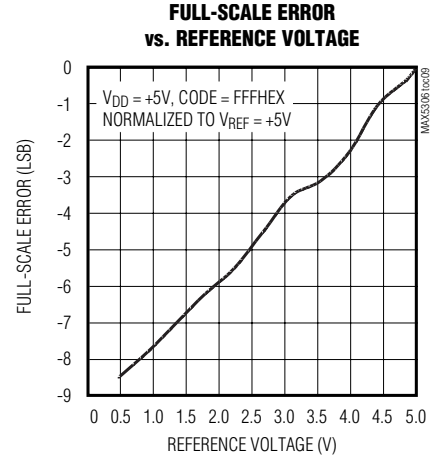
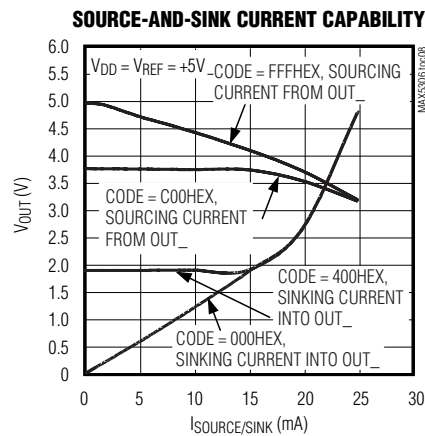
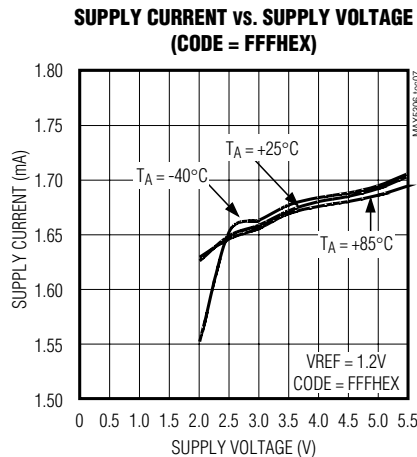
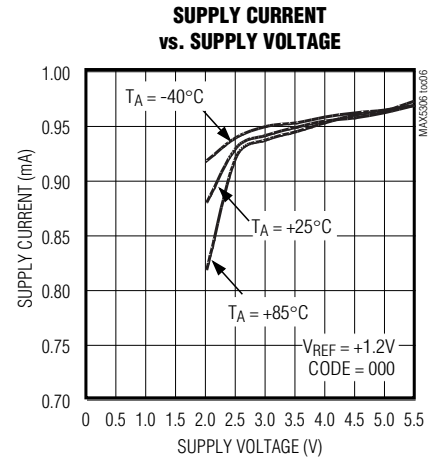
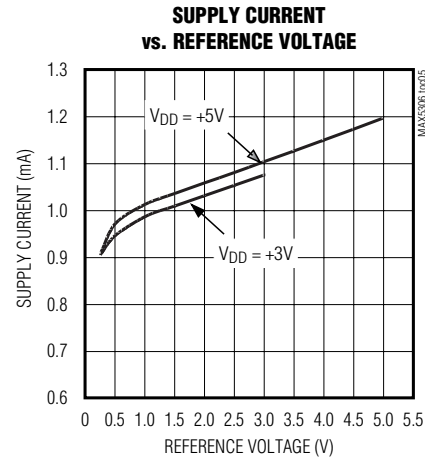
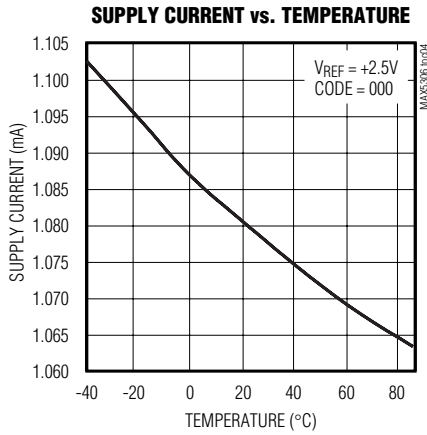
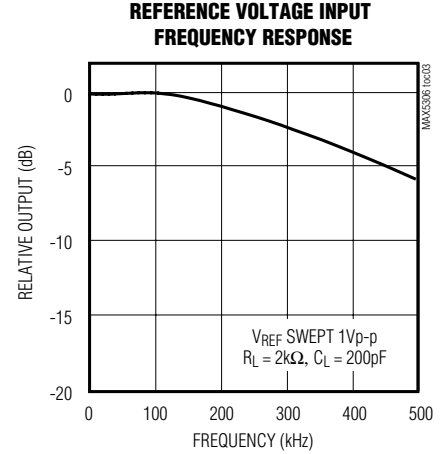
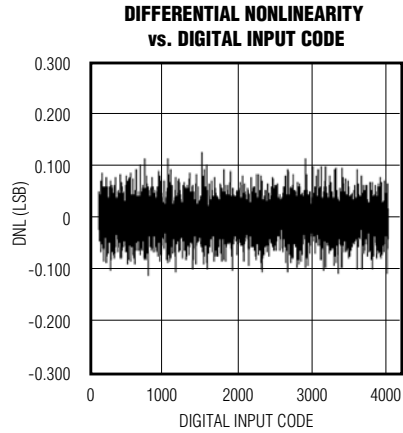
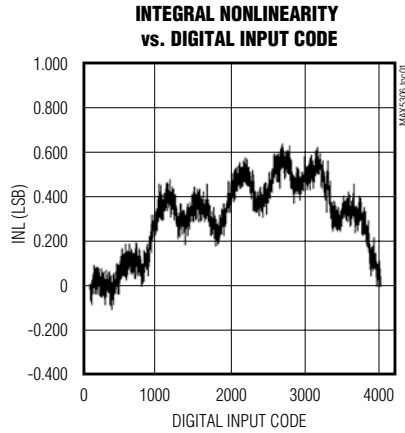
Note 5: Current scales linearly between these two extremes of V_{REF} .

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Typical Operating Characteristics

($V_{DD} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)

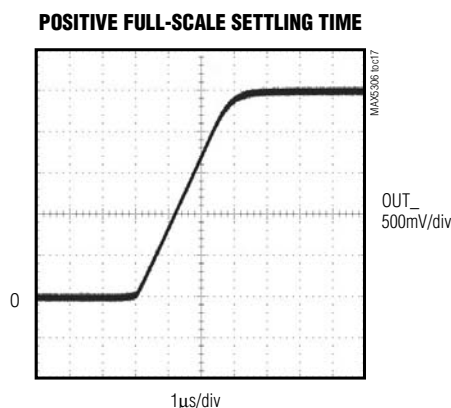
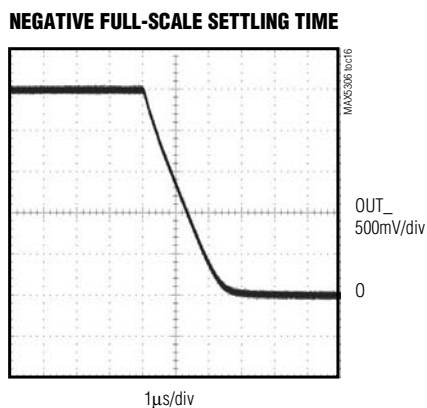
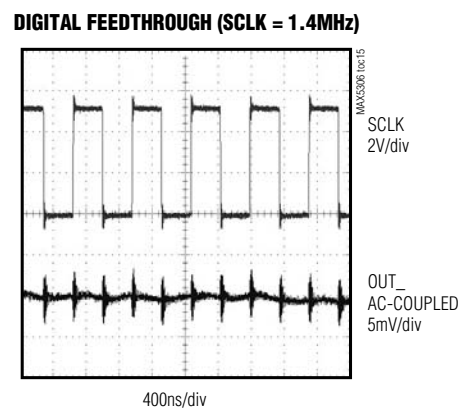
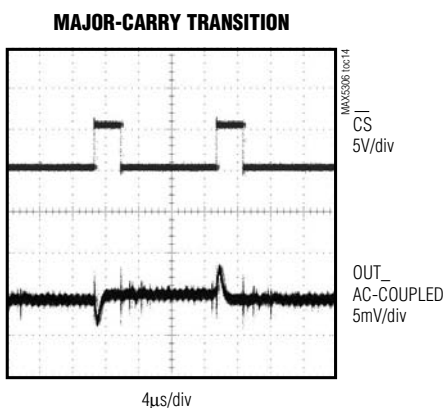
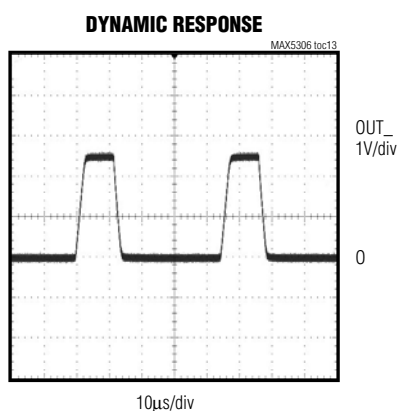
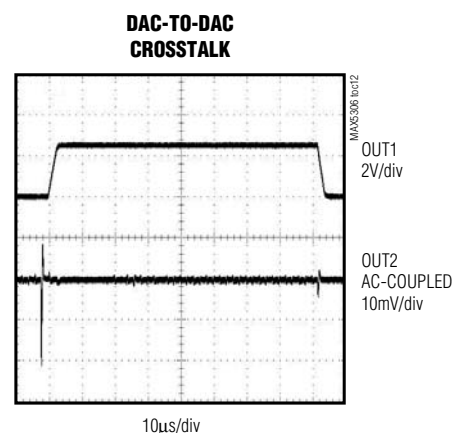
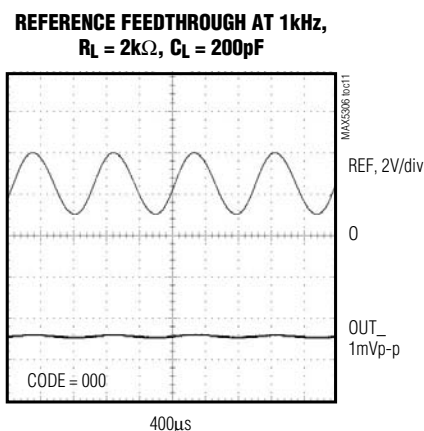
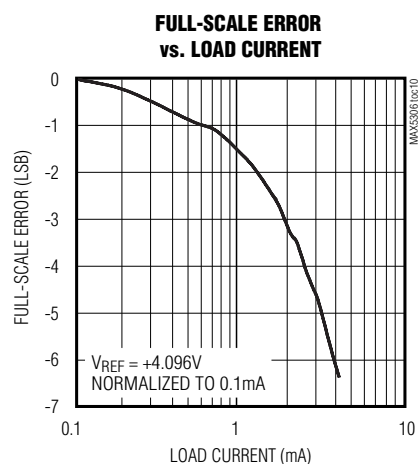
MAX5306/MAX5307



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Typical Operating Characteristics (continued)

($V_{DD} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Description

PIN	NAME	FUNCTION
1	SCLK	Serial Clock Input. Serial data is loaded on the falling edge of SCLK.
2	DIN	Serial Data Input
3	$\overline{\text{LDAC}}$	Load DAC. $\overline{\text{LDAC}}$ is an asynchronous active-low input that updates the DAC outputs simultaneously. If $\overline{\text{LDAC}}$ is driven low, the DAC registers are transparent.
4	REF	Reference Voltage Input
5–12	OUT_	Analog Output Signal
13	GND	Ground
14	V _{DD}	Power Supply. Bypass V _{DD} to GND with a 0.1μF capacitor.
15	DOUT	Data Output (MAX5306). DOUT is updated on the falling edge of SCLK.
	$\overline{\text{CLR}}$	Asynchronous Clear DAC (MAX5307). Active-low input to clear all DACs and registers. Resets all outputs to zero.
16	$\overline{\text{CS}}$	Chip-Select Input (active-low)

Detailed Description

The MAX5306/MAX5307 are 12-bit, eight-channel, low-power, voltage-output digital-to-analog converters (DACs) that are easily addressed using a simple 3-wire serial interface. These devices feature eight double-buffered DACs using a common 16-bit serial to parallel shift register, a power-on reset (POR) circuit and eight output buffer amplifiers.

Figure 1 shows the block diagram of MAX5306/MAX5307. The shift register converts a serial 16-bit word to parallel data for each input register operating with a clock rate of up to 15MHz. The 3-wire digital interface to the shift register consist of chip-select ($\overline{\text{CS}}$), serial clock (SCLK), and data input (DIN). Serial data at DIN is loaded on the falling edge of SCLK.

The eight double-buffered DACs consist of input and DAC registers. The input registers are directly connected to the shift register and hold the result of the most recent write operation. The eight 12-bit DAC registers hold the current output code for the respective DAC. Data can be transferred from the input registers to the DAC registers by either the hardware interface ($\overline{\text{LDAC}}$) or by software command. The output of DACs are buffered through eight Rail-to-Rail® op amps.

The MAX5306 has a digital output (DOUT) which can be used to daisy chain multiple devices on a single serial bus. The MAX5307 contains a hardware shutdown (CLR) to clear all internal registers and power-down all DACs.

The MAX5306/MAX5307 require an external reference such as the MAX6161 family. The reference voltage range is from 0.8V to V_{DD}.

POR circuitry gives the DACs a defined state during startup. At power-on, the DAC outputs reset to zero through a 100kΩ resistor, providing additional safety for applications that drive valves or other transducers that need to be off at power-up.

The MAX5306/MAX5307 feature low digital feedthrough and minimize glitch energy on MSB transitions. The 3-wire SPI, QSPI, MICROWIRE and DSP-compatible serial interface saves additional circuit board space.

Serial Interface Configuration

The MAX5306/MAX5307 3-wire serial interface are compatible with MICROWIRE, SPI, QSPI, and DSPs (Figure 2 and Figure 3). The chip-select input ($\overline{\text{CS}}$) frames the serial data loading at DIN. Following $\overline{\text{CS}}$'s high-to-low transition, the data is shifted synchronously and latched into the input register on each falling edge of the serial clock input (SCLK). Each serial word is 16 bits, the first four bits are the control word followed by 12 data bits (MSB first) as shown in Table 1. The 12-bit DAC code is unipolar binary with 1LSB = V_{REF}/4096.

The serial input register transfers its contents to the input registers after loading 16 bits of data and driving $\overline{\text{CS}}$ high. $\overline{\text{CS}}$ must be brought high for a minimum of 20ns before the next write sequence since a write

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Table 1. Serial Interface Configuration

16-BIT SERIAL WORD																DESC.	FUNCTION
CONTROL BITS				DATA BITS													
MSB				LSB													
C3	C2	C1	C0	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00		
0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	NOP	No Operation
0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	RESET	RESET All Internal Registers. Power-down DACs, outputs pulled down with 100kΩ. Equivalent to software $\overline{\text{CLR}}$.
0	0	1	0													DAC 1	D11–D0 to Input Register 1, DAC Output Unchanged
0	0	1	1													DAC 2	D11–D0 to Input Register 2, DAC Output Unchanged
0	1	0	0													DAC 3	D11–D0 to Input Register 3, DAC Output Unchanged
0	1	0	1													DAC 4	D11–D0 to Input Register 4, DAC Output Unchanged
0	1	1	0													DAC 5	D11–D0 to Input Register 5, DAC Output Unchanged
0	1	1	1													DAC 6	D11–D0 to Input Register 6, DAC Output Unchanged
1	0	0	0													DAC 7	D11–D0 to Input Register 7, DAC Output Unchanged
1	0	0	1													DAC 8	D11–D0 to Input Register 8, DAC Output Unchanged
1	0	1	0													DAC 1–4	D11–D0 to Input Registers 1–4 and DAC Registers 1–4, DAC Outputs Updated (Write-Thru).
1	0	1	1													DAC 5–8	D11–D0 to Input Registers and DAC Registers, DAC Outputs Updated (Write-Thru).
1	1	0	0													DAC 1–8	D11–D0 to Input Registers and DAC Registers, DAC Outputs Updated (Write-Thru).
1	1	0	1													DAC 1–8	D11–D0 to Input Registers, DAC Outputs Unchanged
1	1	1	0	DAC 8	DAC 7	DAC 6	DAC 5	DAC 4	DAC 3	DAC 2	DAC 1	X	X	X	X	DAC 1–8	Input Registers to DAC Registers Indicated by Ones, DAC Outputs Updated, Equivalent to Software LDAC (No effect on DACs indicated by 0's.)

X = Don't Care

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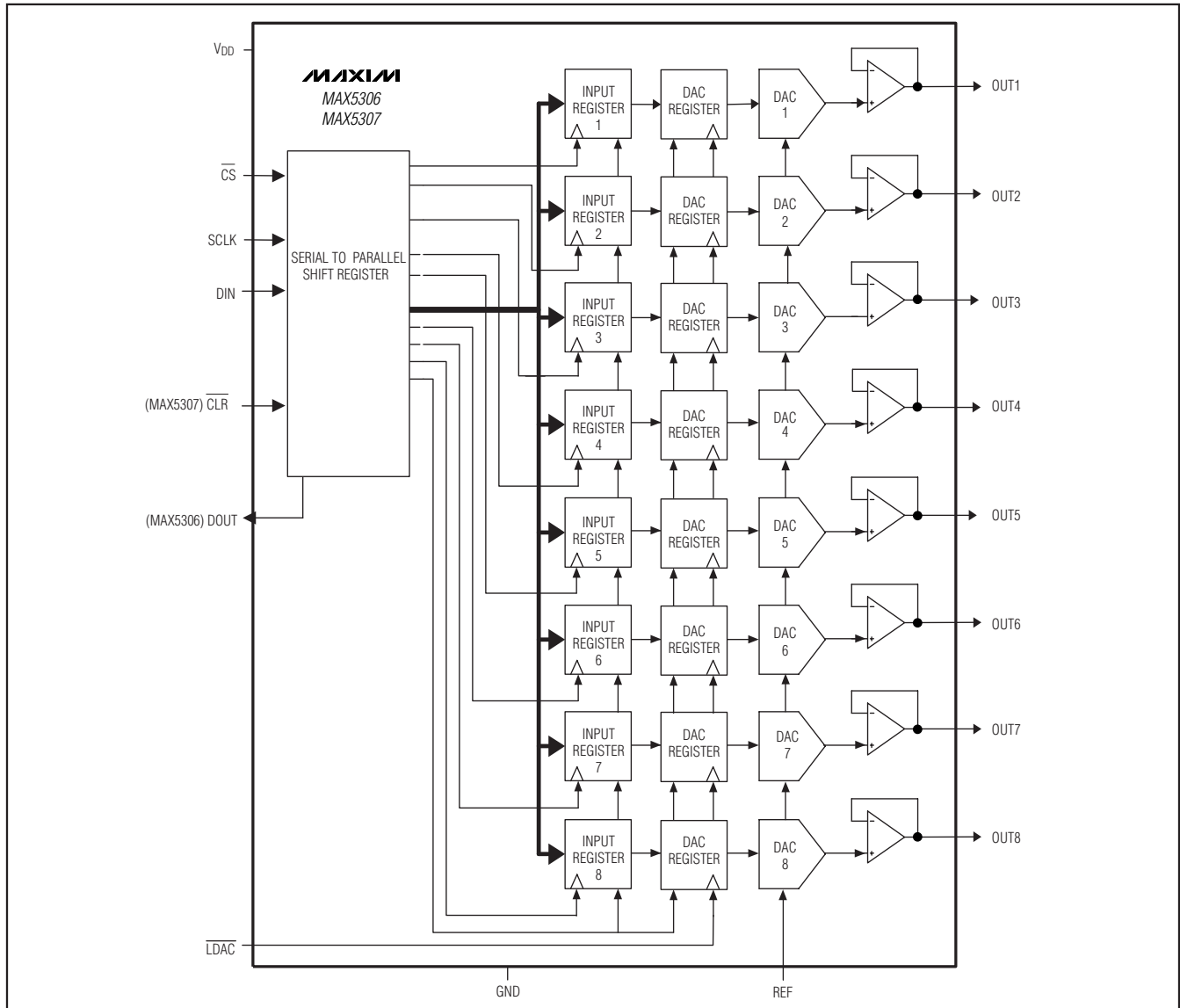


Figure 1. Functional Block Diagram

sequence is initiated on a falling edge of $\overline{CS}$. If $\overline{CS}$ goes high prior to completing 16 cycles of SCLK, the input data is discarded. To initiate a new data transfer, drive $\overline{CS}$ low again. The serial clock (SCLK) can be either high or low between $\overline{CS}$ write pulses. Figure 4 shows the timing diagram for the complete 3-wire serial interface transmission.

The MAX5306/MAX5307 digital inputs are double-buffered. Depending on the command issued through

the serial interface, the input register(s) can be loaded without affecting the DAC register(s), the DAC register(s) can be loaded directly, or all eight registers can be updated simultaneously from the input registers.

Shutdown Modes

The MAX5306/MAX5307 include three software-controlled shutdown modes that reduce the supply current to less than 1 μ A. In two of the three shutdown modes (shutdown 2 and 3) the outputs are independently con-

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Table 2. Serial Interface Power-up and Power-down Commands

CONTROL BITS				DATA BITS												DESC.	FUNCTION
C3	C2	C1	C0	DAC 8	DAC 7	DAC 6	DAC 5	DAC 4	DAC 3	DAC 2	DAC 1	D03	D02	D01	D00		
1	1	1	1									1	1	X	X	Power-Up	Power-Up individual DAC buffers indicated by data in DAC1 through DAC8. A one indicates the DAC output is active. A zero does not affect the DACs present state.
1	1	1	1									0	1	X	X	Shutdown 1	Shutdown individual DAC buffers indicated by data in DAC1 through DAC8. A one indicates the DAC output is high-impedance. A zero does not affect the DACs present state.
1	1	1	1									1	0	X	X	Shutdown 2	Shutdown individual DAC buffers indicated by data in DAC1 through DAC8. A one indicates the DAC is shutdown and the output is connected to GND through a 1k Ω resistor. A zero does not affect the DACs present state.
1	1	1	1									0	0	X	X	Shutdown 3	Shutdown individual DAC buffers indicated by data in DAC1 through DAC8. A one indicates the DAC is shutdown and the output is connected to GND through a 100k Ω resistor. A zero does not affect the DACs present state.

X = Don't Care

nected to ground through a 1k Ω or 100k Ω (default) resistor for each DAC. The third shutdown (shutdown 1) command leaves the DACs outputs high impedance. Table 2 lists the three shutdown modes of operation as well as the power-up command.

Serial-Data Output (DOUT)

The DOUT (MAX5306) follows DIN with a 16 clock cycle delay. The DOUT is capable of driving 20pF load with a 50ns (max) delay from the falling edge of SCLK.

DOUT is primarily used for daisy-chaining multiple devices. Optionally, DOUT can be used to monitor the serial interface for valid communications by connecting DOUT to a microprocessor input.

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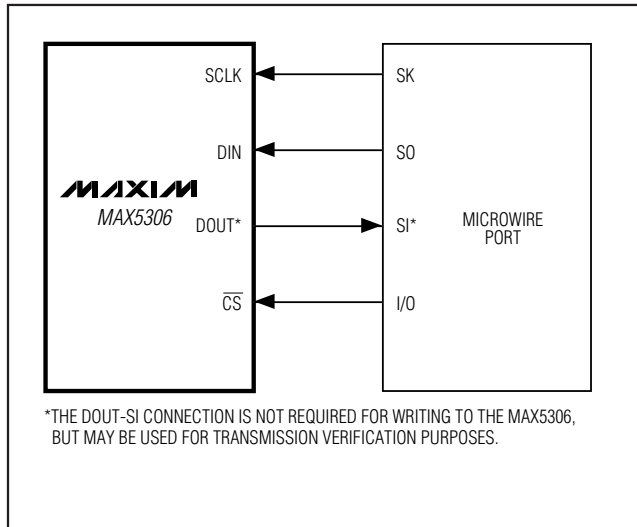


Figure 2. Connections for MICROWIRE

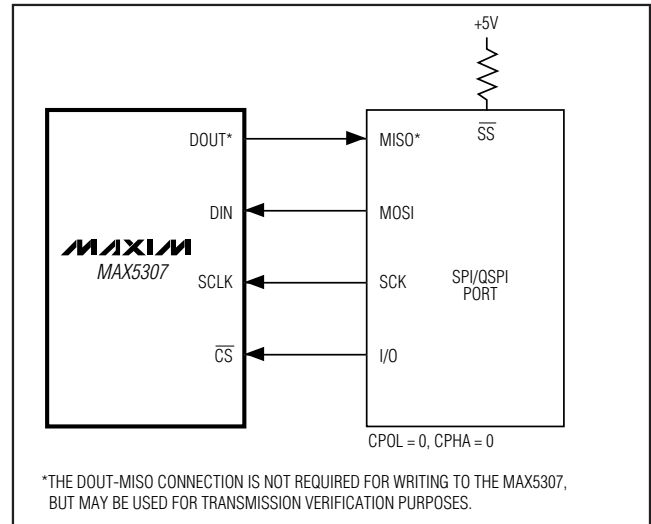


Figure 3. Connections for SPI/QSPI

Hardware Clear (CLR)

The MAX5307 has an active low $\overline{\text{CLR}}$ input. Drive $\overline{\text{CLR}}$ low to clear all internal registers, shutdown all DACs, and terminate all DAC outputs to GND through 100k Ω resistors. $\overline{\text{CLR}}$ is asynchronous and can be applied at any time. If $\overline{\text{CLR}}$ is toggled low during loading of a serial word, that word will terminate and must be reloaded.

Reference Input

The external reference input has a typical input impedance of 200k Ω . The input voltage range is from 800mV to V_{DD} . V_{DD} can be used as the reference for the MAX5306/MAX5307. The DAC outputs are then ratio-metric to V_{DD} .

Output Buffer

The rail-to-rail buffer amplifier is stable with any combination of resistive loads greater than 2k Ω and capacitive loads less than 500pF. With a capacitive load of 200pF the output buffers have a slew rate of 1V/ μ s. For a 1/4 FS to 3/4 FS output transition, the amplifier output typically settles to 1/2 LSB in less than 10 μ s when loaded with 2k Ω in parallel with 200pF.

Power-On Reset

The MAX5306/MAX5307 have a POR circuit to set the DACs output to zero when V_{DD} is first applied. This ensures that unwanted DAC output voltages will not occur immediately following a system startup, such as after a loss of power. Upon initial power-up the POR circuit ensures that all DAC registers are cleared, the DACs are powered-down, and their outputs are terminated to GND through a 100k Ω resistor.

Application Information

Daisy-Chaining Devices

Any number of MAX5306 can be daisy-chained by connecting the DOUT pin of one device to the DIN pin of the following device in the chain (Figure 5). To write to the chain, drive $\overline{\text{CS}}$ low until all $n \times 16$ clock cycles (where n is the number of devices in the chain) and associated data have been applied to the first device. When $\overline{\text{CS}}$ is driven high, each device in the chain acts on the 16 bits in its input register. To adjust a single device in the chain, a No-Operation (NOP) command must be loaded for all other devices.

Figure 6 shows an alternate method of connecting several MAX5306s or MAX5307s. In this configuration, the data bus is common to all devices; data is not shifted through a daisy chain. More I/O lines are required in this configuration because a dedicated chip-select input ($\overline{\text{CS}}$) is required for each IC.

Unipolar Output

The MAX5306/MAX5307 are normally configured for unipolar output. Table 3 lists the unipolar output voltages vs. digital codes.

Bipolar Output

The MAX5306/MAX5307 outputs can be configured for bipolar operation using Figure 7's circuit.

$$V_{\text{OUT}} = V_{\text{REF}} [(2D / 4096) - 1]$$

where D is the decimal value of the DACs binary input code. Table 4 shows digital codes (offset binary) and corresponding output voltages for the Figure 7 circuit.

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Power-Supply Considerations

On power-up, all input and DAC registers are cleared and DOUT is in low.

Bypass V_{DD} to GND with a $4.7\mu\text{F}$ capacitor in parallel with a $0.1\mu\text{F}$ capacitor. Use short lead lengths and place the bypass capacitors as close to the supply pins as possible.

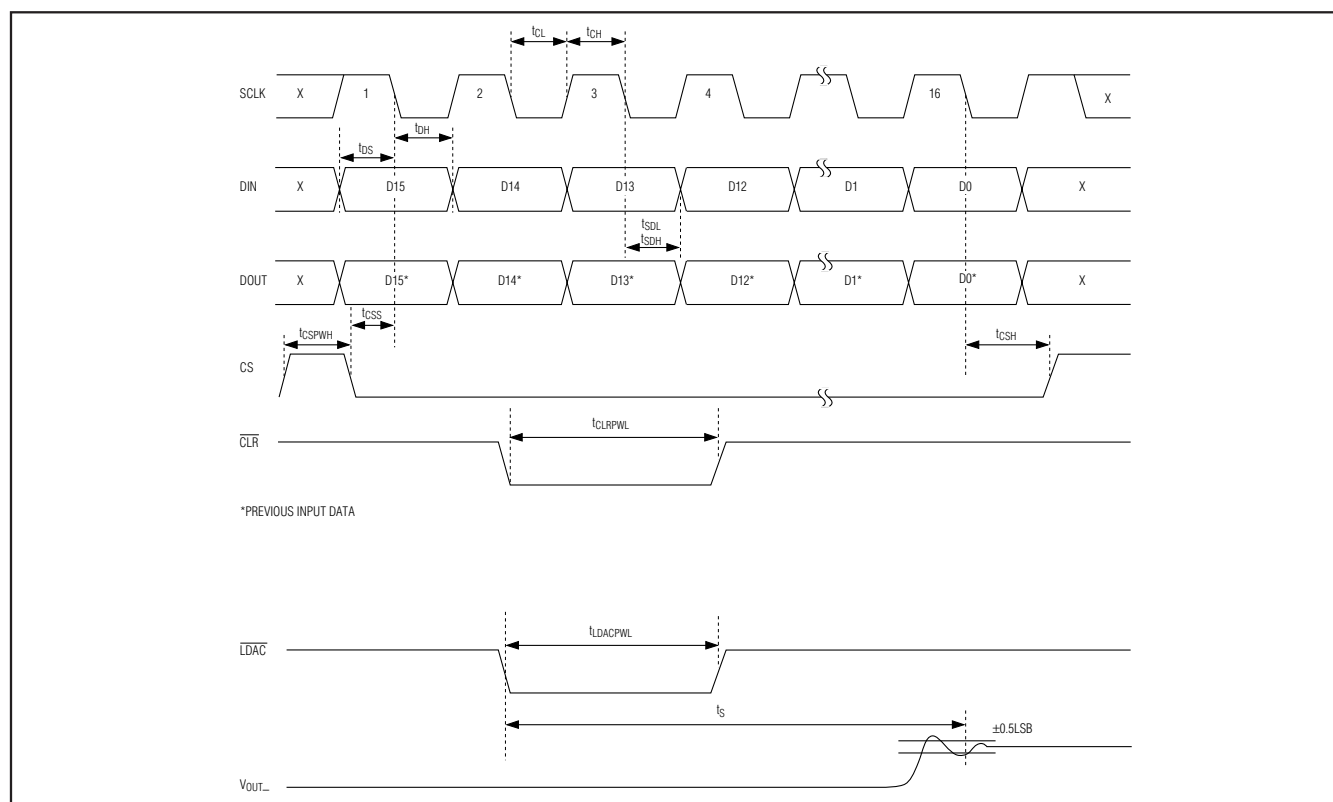


Figure 4. Timing Diagram

Table 3. Unipolar Code Table

DAC CONTENTS			ANALOG OUTPUT
MSB	LSB		
1111	1111	1111	$+V_{REF} \left(\frac{4095}{4096} \right)$
1000	0000	0001	$+V_{REF} \left(\frac{2049}{4096} \right)$
1000	0000	0000	$+V_{REF} \left(\frac{2048}{4096} \right) = \frac{+V_{REF}}{2}$
0111	1111	1111	$+V_{REF} \left(\frac{2047}{4096} \right)$
0000	0000	0001	$+V_{REF} \left(\frac{1}{4096} \right)$
0000	0000	0000	0V

Table 4. Bipolar Code Table

DAC CONTENTS			ANALOG OUTPUT
MSB	LSB		
1111	1111	1111	$+V_{REF} \left(\frac{2047}{2048} \right)$
1000	0000	0001	$+V_{REF} \left(\frac{1}{2048} \right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{REF} \left(\frac{1}{2048} \right)$
0000	0000	0001	$-V_{REF} \left(\frac{2047}{2048} \right)$
0000	0000	0000	$-V_{REF} \left(\frac{2048}{2048} \right) = -V_{REF}$

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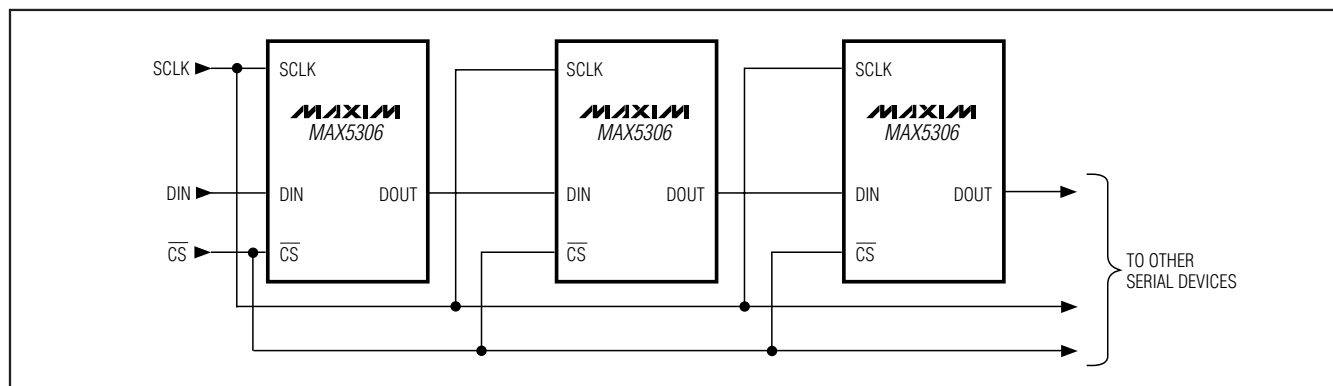


Figure 5. Daisy-Chaining MAX5306s

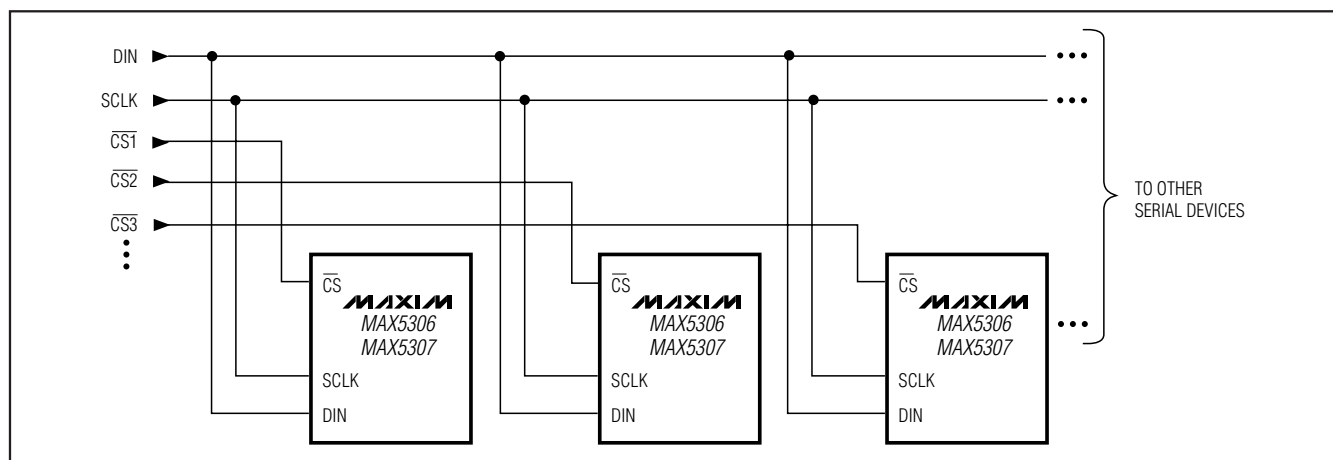


Figure 6. Multiple MAX5306s or MAX5307s Sharing a Common DIN Line

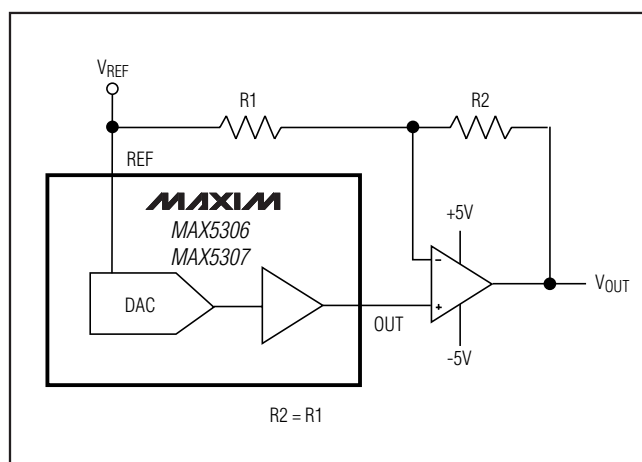


Figure 7. Bipolar Output Circuit

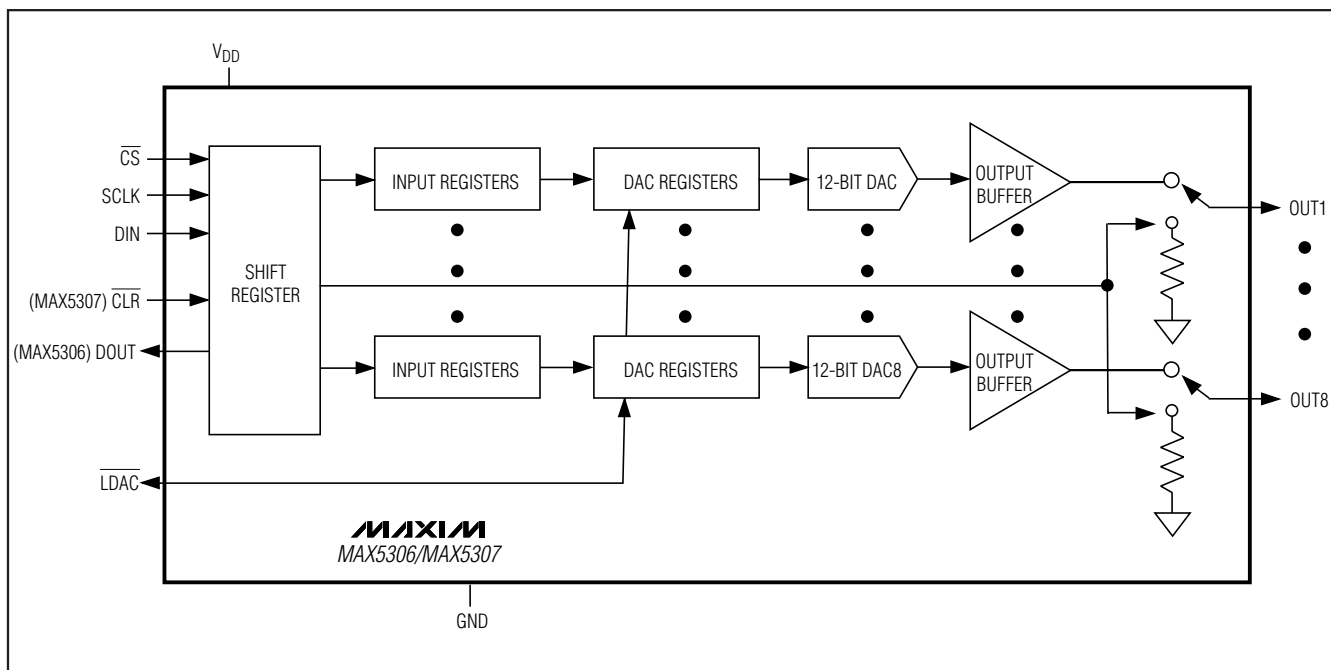
Chip Information

TRANSISTOR COUNT: 19,000

PROCESS TECHNOLOGY: BiCMOS

Low-Power, Low-Glitch, Octal 12-Bit Voltage-Output DACs with Serial Interface

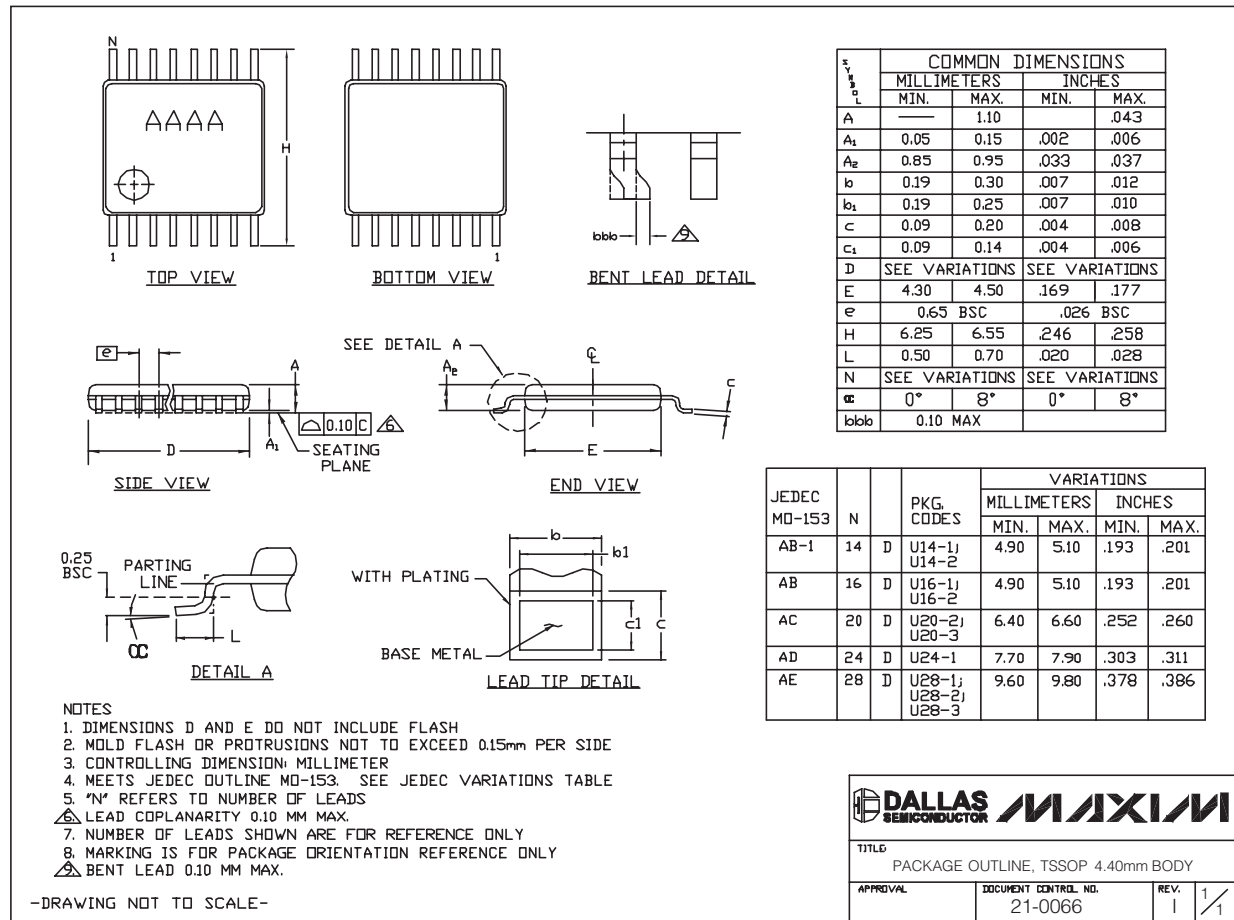
Simplified Block Diagram



Low-Power, Low-Glitch, Octal 12-Bit Voltage-Output DACs with Serial Interface

Package Information

MAX5306/MAX5307



TSSOP4, 40mm body

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