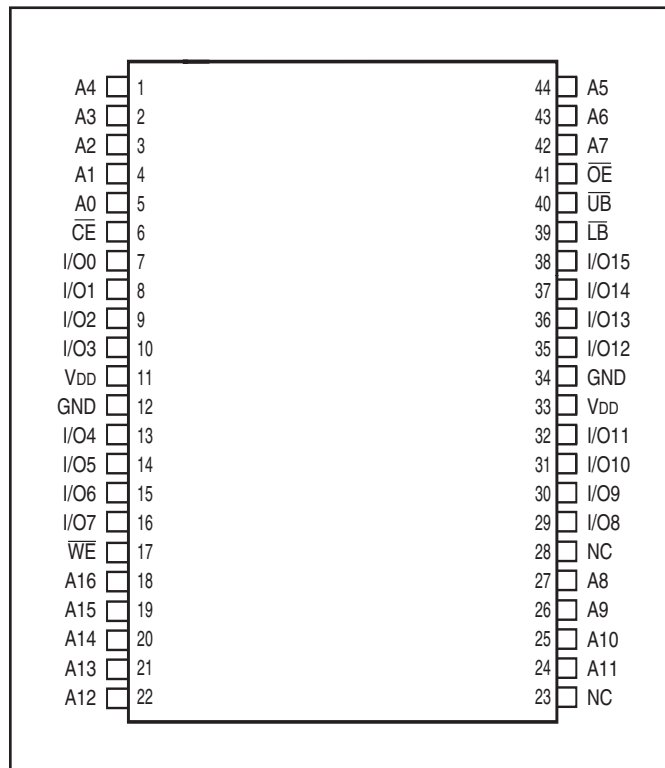


TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN		V _{DD} Current
						I/O0-I/O7	I/O8-I/O15	
Not Selected	X	H	X	X	X	High-Z	High-Z	I _{SB1} , I _{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I _{CC}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D _{OUT}	High-Z	I _{CC}
	H	L	L	H	L	High-Z	D _{OUT}	
	H	L	L	L	L	D _{OUT}	D _{OUT}	
Write	L	L	X	L	H	D _{IN}	High-Z	I _{CC}
	L	L	X	H	L	High-Z	D _{IN}	
	L	L	X	L	L	D _{IN}	D _{IN}	

PIN CONFIGURATION

44-Pin TSOP (Type II) (T)

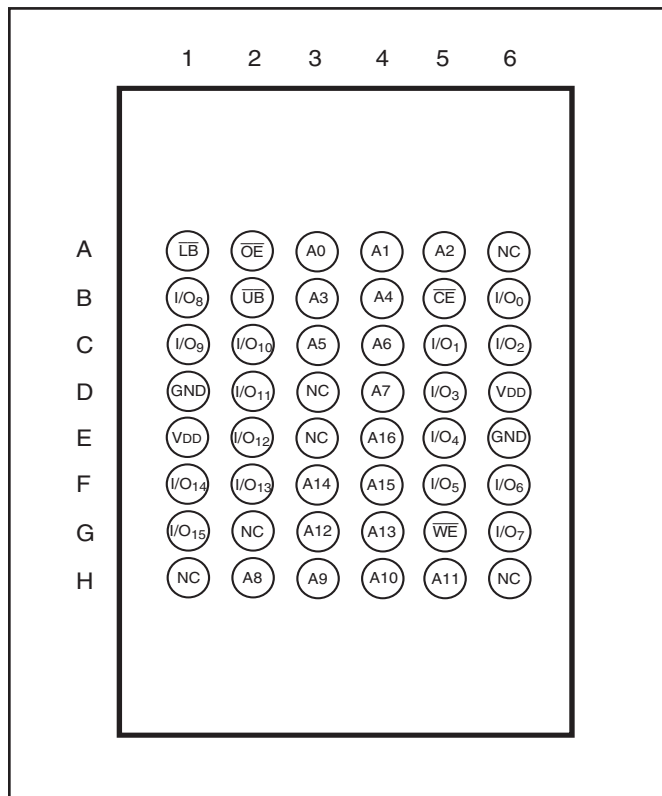


PIN DESCRIPTIONS

A0-A16	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CE	Chip Enable Input
OE	Output Enable Input
WE	Write Enable Input
LB	Lower-byte Control (I/O0-I/O7)
UB	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V _{DD}	Power
GND	Ground

PIN CONFIGURATION

48-Pin mini BGA (B)



PIN DESCRIPTIONS

A0-A16 Address Inputs

I/O0-I/O15 Data Inputs/Outputs

CE Chip Enable Input

OE Output Enable Input

WE Write Enable Input

LB Lower-byte Control (I/O0-I/O7)

UB Upper-byte Control (I/O8-I/O15)

NC No Connection

VDD Power

GND Ground

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

$V_{DD} = 3.3V \pm 5\%$

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{DD} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4	—	V
V_{OL}	Output LOW Voltage	$V_{DD} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$	—	0.4	V
V_{IH}	Input HIGH Voltage		2	$V_{DD} + 0.3$	V
V_{IL}	Input LOW Voltage ⁽¹⁾		-0.3	0.8	V
I_{LI}	Input Leakage	$GND \leq V_{IN} \leq V_{DD}$	-1	1	μA
I_{LO}	Output Leakage	$GND \leq V_{OUT} \leq V_{DD}$, Outputs Disabled	-1	1	μA

Note:

- $V_{IL} (\text{min.}) = -0.3V \text{ DC}; V_{IL} (\text{min.}) = -2.0V \text{ AC}$ (pulse width < 10 ns). Not 100% tested.
 $V_{IH} (\text{max.}) = V_{DD} + 0.3V \text{ DC}; V_{IH} (\text{max.}) = V_{DD} + 2.0V \text{ AC}$ (pulse width < 10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

$V_{DD} = 2.4V-3.6V$

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{DD} = \text{Min.}, I_{OH} = -1.0 \text{ mA}$	1.8	—	V
V_{OL}	Output LOW Voltage	$V_{DD} = \text{Min.}, I_{OL} = 1.0 \text{ mA}$	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	$V_{DD} + 0.3$	V
V_{IL}	Input LOW Voltage ⁽¹⁾		-0.3	0.8	V
I_{LI}	Input Leakage	$GND \leq V_{IN} \leq V_{DD}$	-1	1	μA
I_{LO}	Output Leakage	$GND \leq V_{OUT} \leq V_{DD}$, Outputs Disabled	-1	1	μA

Note:

- $V_{IL} (\text{min.}) = -0.3V \text{ DC}; V_{IL} (\text{min.}) = -2.0V \text{ AC}$ (pulse width < 10 ns). Not 100% tested.
 $V_{IH} (\text{max.}) = V_{DD} + 0.3V \text{ DC}; V_{IH} (\text{max.}) = V_{DD} + 2.0V \text{ AC}$ (pulse width < 10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

$V_{DD} = 1.65V-2.2V$

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -0.1 \text{ mA}$	1.65-2.2V	1.4	—	V
V_{OL}	Output LOW Voltage	$I_{OL} = 0.1 \text{ mA}$	1.65-2.2V	—	0.2	V
V_{IH}	Input HIGH Voltage		1.65-2.2V	1.4	$V_{DD} + 0.2$	V
$V_{IL}^{(1)}$	Input LOW Voltage		1.65-2.2V	-0.2	0.4	V
I_{LI}	Input Leakage	$GND \leq V_{IN} \leq V_{DD}$		-1	1	μA
I_{LO}	Output Leakage	$GND \leq V_{OUT} \leq V_{DD}$, Outputs Disabled		-1	1	μA

Note:

- $V_{IL} (\text{min.}) = -0.3V \text{ DC}; V_{IL} (\text{min.}) = -2.0V \text{ AC}$ (pulse width < 10 ns). Not 100% tested.
 $V_{IH} (\text{max.}) = V_{DD} + 0.3V \text{ DC}; V_{IH} (\text{max.}) = V_{DD} + 2.0V \text{ AC}$ (pulse width < 10 ns). Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit (2.4V-3.6V)	Unit (3.3V $\pm$ 5%)	Unit (1.65V-2.2V)
Input Pulse Level	0.4V to $V_{DD} - 0.3V$	0.4V to $V_{DD} - 0.3V$	0.4V to $V_{DD} - 0.3V$
Input Rise and Fall Times	1V/ ns	1V/ ns	1V/ ns
Input and Output Timing and Reference Level (V_{Ref})	$V_{DD} / 2$	$\frac{V_{DD}}{2} + 0.05$	0.9V
Output Load	See Figures 1 and 2	See Figures 1 and 2	See Figures 1 and 2
R1 (Ω)	1909	317	13500
R2 (Ω)	1105	351	10800
V_{TM} (V)	3.0V	3.3V	1.8V

AC TEST LOADS

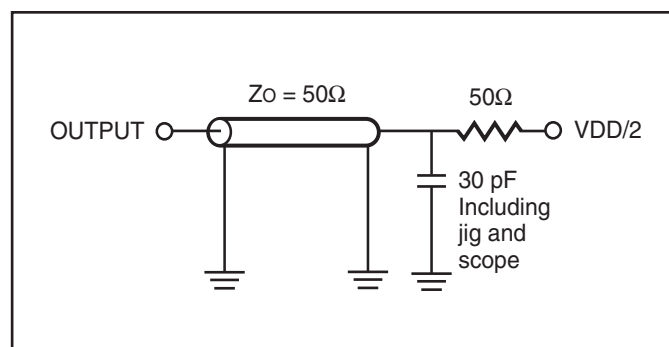


Figure 1.

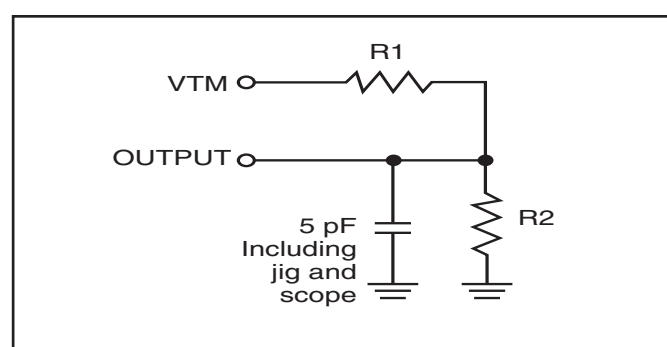


Figure 2.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	−0.5 to V _{DD} + 0.5	V
V _{DD}	V _{DD} Relates to GND	−0.3 to 4.0	V
T _{STG}	Storage Temperature	−65 to +150	°C
P _T	Power Dissipation	1.0	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{I/O}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

HIGH SPEED (IS61WV12816DALL/DBLL)

OPERATING RANGE (V_{DD}) (IS61WV12816DALL)

Range	Ambient Temperature	V _{DD}	Speed
Commercial	0°C to +70°C	1.65V-2.2V	20ns
Industrial	-40°C to +85°C	1.65V-2.2V	20ns

OPERATING RANGE (V_{DD}) (IS61WV12816DBLL)⁽¹⁾

Range	Ambient Temperature	V _{DD} (8 ns) ¹	V _{DD} (10 ns) ¹
Commercial	0°C to +70°C	3.3V ± 5%	2.4V-3.6V
Industrial	-40°C to +85°C	3.3V ± 5%	2.4V-3.6V

Note:

1. When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V ± 5%, the device meets 8ns.

OPERATING RANGE (V_{DD}) (IS64WV12816DBLL)^(2,3)

Range	Ambient Temperature	V _{DD} (10 ns) ²	V _{DD} (12 ns) ²
Automotive	-40°C to +125°C	3.3V ± 5%	2.4V-3.6V

Note:

2. When operated in the range of 2.4V-3.6V, the device meets 12ns. When operated in the range of 3.3V ± 5%, the device meets 10ns.
3. If the device is operated in the temperature range of -40°C to +85°C, the device meets 10ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-8		-10		-12		-20		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I _{CC}	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max.,	Com.	—	65	—	60	—	55	—	40	mA
		I _{OUT} = 0 mA, f = f _{MAX}	Ind.	—	70	—	65	—	55	—	45	
		$\overline{CE} = V_{IL}$	Auto. ⁽³⁾	—	—	—	75	—	60	—	50	
		V _{IN} ≥ V _{DD} - 0.3V, or V _{IN} ≤ 0.4V	typ. ⁽²⁾			45		45				
I _{CC1}	Operating Supply Current	V _{DD} = Max.,	Com.	—	2	—	2	—	2	—	2	mA
		I _{OUT} = 0 mA, f = 0	Ind.	—	2	—	2	—	2	—	2	
		$\overline{CE} = V_{IL}$	Auto.	—	—	—	2	—	2	—	2	
		V _{IN} ≥ V _{DD} - 0.3V, or V _{IN} ≤ 0.4V										
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max.,	Com.	—	50	—	50	—	50	—	50	μA
		$\overline{CE} \geq V_{DD} - 0.2V$,	Ind.	—	70	—	70	—	70	—	70	
		V _{IN} ≥ V _{DD} - 0.2V, or	Auto.	—	—	—	100	—	100	—	100	
		V _{IN} ≤ 0.2V, f = 0	typ. ⁽²⁾			4		4				

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.
3. For Automotive grade at 15ns, typ. I_{CC} = 38mA, not 100% tested.

LOW POWER (IS61WV12816DALS/DBLS)

OPERATING RANGE (V_{DD}) (IS61WV12816DALS)

Range	Ambient Temperature	V _{DD}	Speed
Commercial	0°C to +70°C	1.65V-2.2V	45ns
Industrial	-40°C to +85°C	1.65V-2.2V	45ns

OPERATING RANGE (V_{DD}) (IS61WV12816DBLS)

Range	Ambient Temperature	V _{DD} (35 ns)
Commercial	0°C to +70°C	2.4V-3.6V
Industrial	-40°C to +85°C	2.4V-3.6V

OPERATING RANGE (V_{DD}) (IS64WV12816DBLS)

Range	Ambient Temperature	V _{DD} (35 ns)
Automotive	-40°C to +125°C	2.4V-3.6V

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-25		-35		-45		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I _{CC}	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max.,	Com.	—	20	—	20	—	18	mA
		I _{OUT} = 0 mA, f = f _{MAX}	Ind.	—	25	—	25	—	20	
		$\overline{CE} = V_{IL}$	Auto.	—	40	—	35	—	30	
		V _{IN} ≥ V _{DD} - 0.3V, or V _{IN} ≤ 0.4V	typ. ⁽²⁾		18					
I _{CC1}	Operating Supply Current	V _{DD} = Max.,	Com.	—	2	—	2	—	2	mA
		I _{OUT} = 0 mA, f = 0	Ind.	—	2	—	2	—	2	
		$\overline{CE} = V_{IL}$	Auto.	—	2	—	2	—	2	
		V _{IN} ≥ V _{DD} - 0.3V, or V _{IN} ≤ 0.4V								
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max.,	Com.	—	40	—	40	—	40	μA
		$\overline{CE} \geq V_{DD} - 0.2V$,	Ind.	—	50	—	50	—	50	
		V _{IN} ≥ V _{DD} - 0.2V, or	Auto.	—	75	—	75	—	75	
		V _{IN} ≤ 0.2V, f = 0	typ. ⁽²⁾		4					

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-8		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	8	—	10	—	12	—	ns
t _{AA}	Address Access Time	—	8	—	10	—	12	ns
t _{OHA}	Output Hold Time	2.0	—	2.0	—	3	—	ns
t _{ACE}	$\overline{\text{CE}}$ Access Time	—	8	—	10	—	12	ns
t _{DOE}	$\overline{\text{OE}}$ Access Time	—	5.5	—	6.0	—	6.0	ns
t _{HZOE} ⁽²⁾	$\overline{\text{OE}}$ to High-Z Output	—	3	—	4	—	6	ns
t _{LZOE} ⁽²⁾	$\overline{\text{OE}}$ to Low-Z Output	0	—	0	—	0	—	ns
t _{HZCE} ⁽²⁾	$\overline{\text{CE}}$ to High-Z Output	0	3	0	4	0	6	ns
t _{LZCE} ⁽²⁾	$\overline{\text{CE}}$ to Low-Z Output	3	—	3	—	3	—	ns
t _{BA}	$\overline{\text{LB}}$, $\overline{\text{UB}}$ Access Time	—	5.5	—	6.5	—	6.5	ns
t _{HZB} ⁽²⁾	$\overline{\text{LB}}$, $\overline{\text{UB}}$ to High-Z Output	0	5.5	0	6.5	0	6.5	ns
t _{LZB} ⁽²⁾	$\overline{\text{LB}}$, $\overline{\text{UB}}$ to Low-Z Output	0	—	0	—	0	—	ns
t _{PU}	Power Up Time	0	—	0	—	0	—	ns
t _{PD}	Power Down Time	—	8	—	10	—	10	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

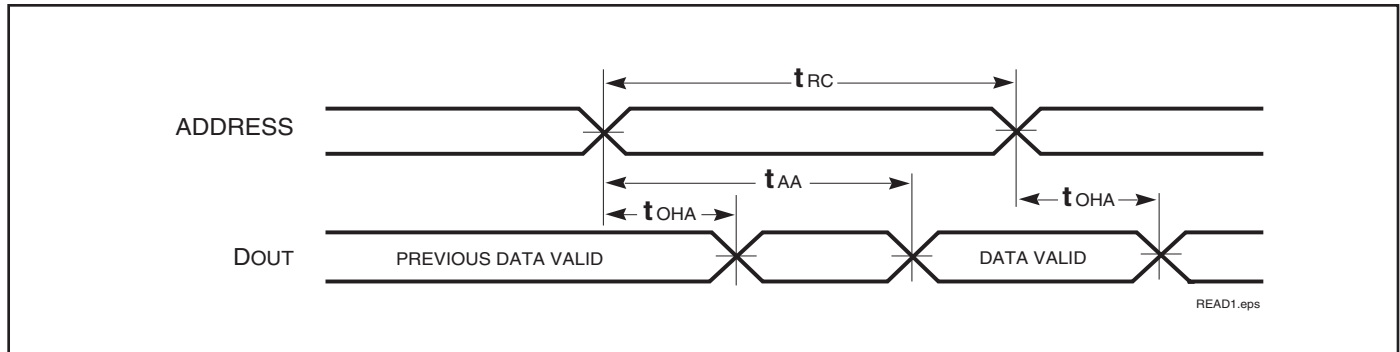
Symbol	Parameter	-20 ns		-25 ns		-35 ns		-45 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	20	—	25	—	35	—	45	—	ns
t _{AA}	Address Access Time	—	20	—	25	—	35	—	45	ns
t _{OHA}	Output Hold Time	2.5	—	6	—	8	—	10	—	ns
t _{ACE}	$\overline{\text{CE}}$ Access Time	—	20	—	25	—	35	—	45	ns
t _{DOE}	$\overline{\text{OE}}$ Access Time	—	8	—	12	—	15	—	20	ns
t _{HZOE⁽²⁾}	$\overline{\text{OE}}$ to High-Z Output	0	8	0	8	0	10	0	15	ns
t _{LZOE⁽²⁾}	$\overline{\text{OE}}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns
t _{HZCE⁽²⁾}	$\overline{\text{CE}}$ to High-Z Output	0	8	0	8	0	10	0	15	ns
t _{LZCE⁽²⁾}	$\overline{\text{CE}}$ to Low-Z Output	3	—	10	—	10	—	10	—	ns
t _{BA}	LB, UB Access Time	—	8	—	25	—	35	—	45	ns
t _{HZB}	LB, UB to High-Z Output	0	8	0	8	0	10	0	15	ns
t _{LZB}	LB, UB to Low-Z Output	0	—	0	—	0	—	0	—	ns

Notes:

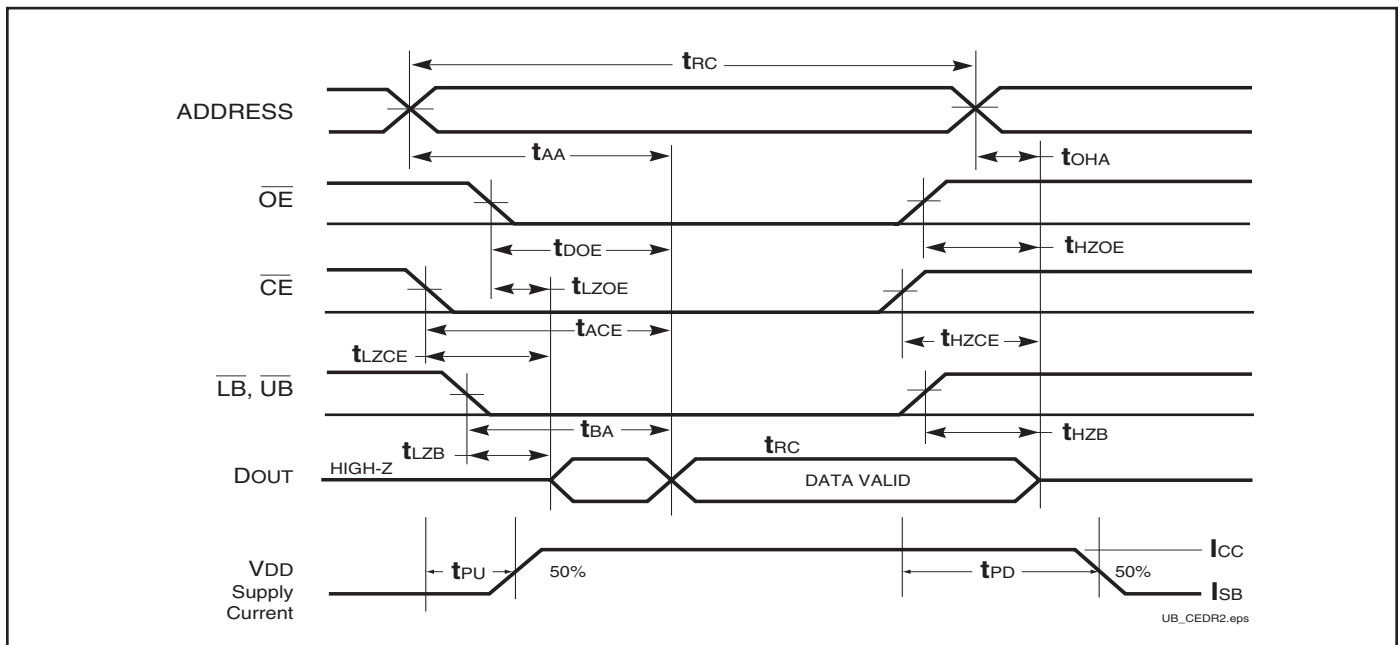
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$, $\overline{UB}$ or $\overline{LB} = V_{IL}$)



READ CYCLE NO. 2^(1,3)



Notes:

1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{UB}$, or $\overline{LB} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

Symbol	Parameter	-8		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	8	—	10	—	12	—	ns
t _{SCE}	$\overline{CE}$ to Write End	6.5	—	8	—	9	—	ns
t _{AW}	Address Setup Time to Write End	6.5	—	8	—	9	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	ns
t _{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	6.5	—	8	—	9	—	ns
t _{PWE1}	$\overline{WE}$ Pulse Width	6.5	—	8	—	9	—	ns
t _{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	8.0	—	10	—	11	—	ns
t _{SD}	Data Setup to Write End	5	—	6	—	9	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t _{HZWE} ⁽²⁾	$\overline{WE}$ LOW to High-Z Output	—	3.5	—	5	—	6	ns
t _{LZWE} ⁽²⁾	$\overline{WE}$ HIGH to Low-Z Output	2	—	2	—	3	—	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

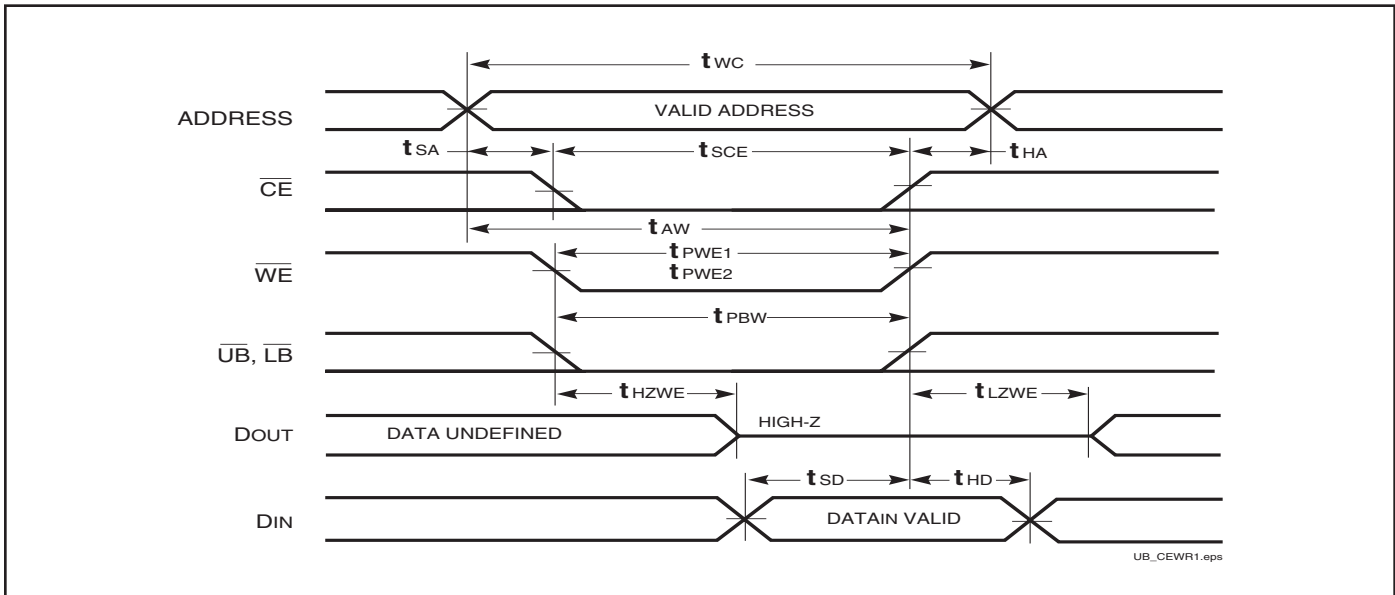
Symbol	Parameter	-20 ns		-25 ns		-35 ns		-45ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	20	—	25	—	35	—	45	—	ns
t _{SCE}	CE to Write End	12	—	18	—	25	—	35	—	ns
t _{AW}	Address Setup Time to Write End	12	—	15	—	25	—	35	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t _{PWB}	LB, UB Valid to End of Write	12	—	18	—	30	—	35	—	ns
t _{PWE1}	WE Pulse Width (OE = HIGH)	12	—	18	—	30	—	35	—	ns
t _{PWE2}	WE Pulse Width (OE = LOW)	17	—	20	—	30	—	35	—	ns
t _{SD}	Data Setup to Write End	9	—	12	—	15	—	20	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{HZWE} ⁽³⁾	WE LOW to High-Z Output	—	9	—	12	—	20	—	20	ns
t _{LZWE} ⁽³⁾	WE HIGH to Low-Z Output	3	—	5	—	5	—	5	—	ns

Notes:

1. Test conditions for IS61WV6416LL assume signal transition times of 1.5ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

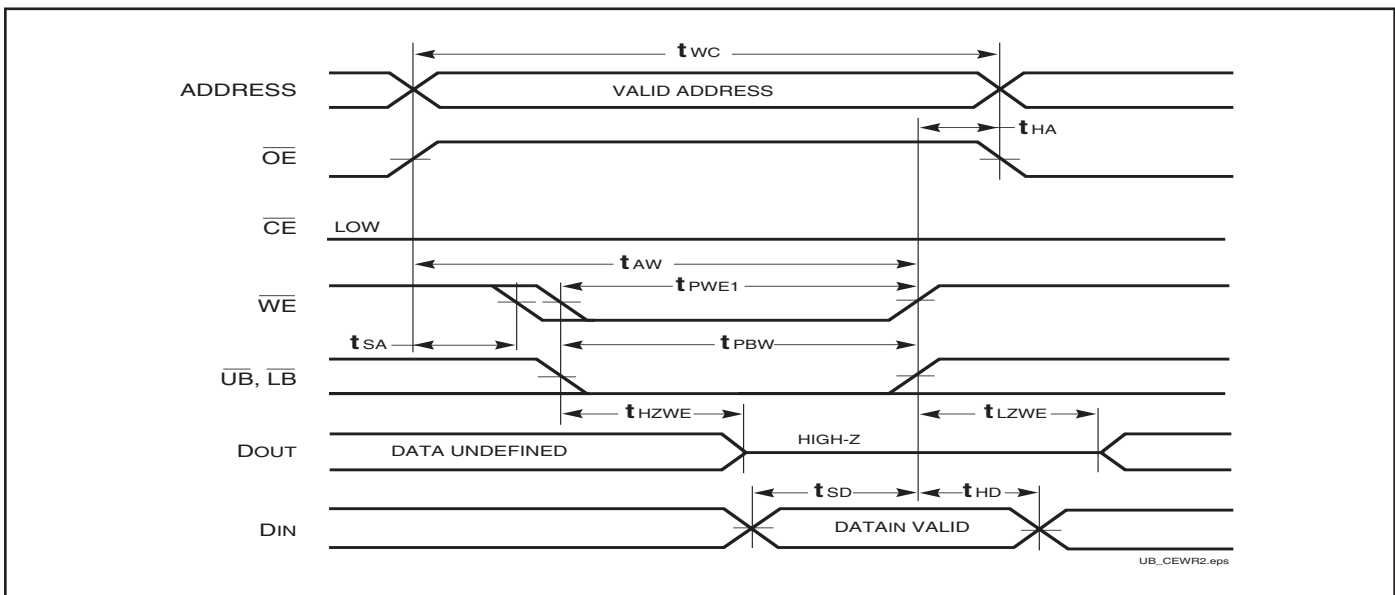
WRITE CYCLE NO. 1 ($\overline{CE}$ Controlled, $\overline{OE}$ is HIGH or LOW) ⁽¹⁾



Notes:

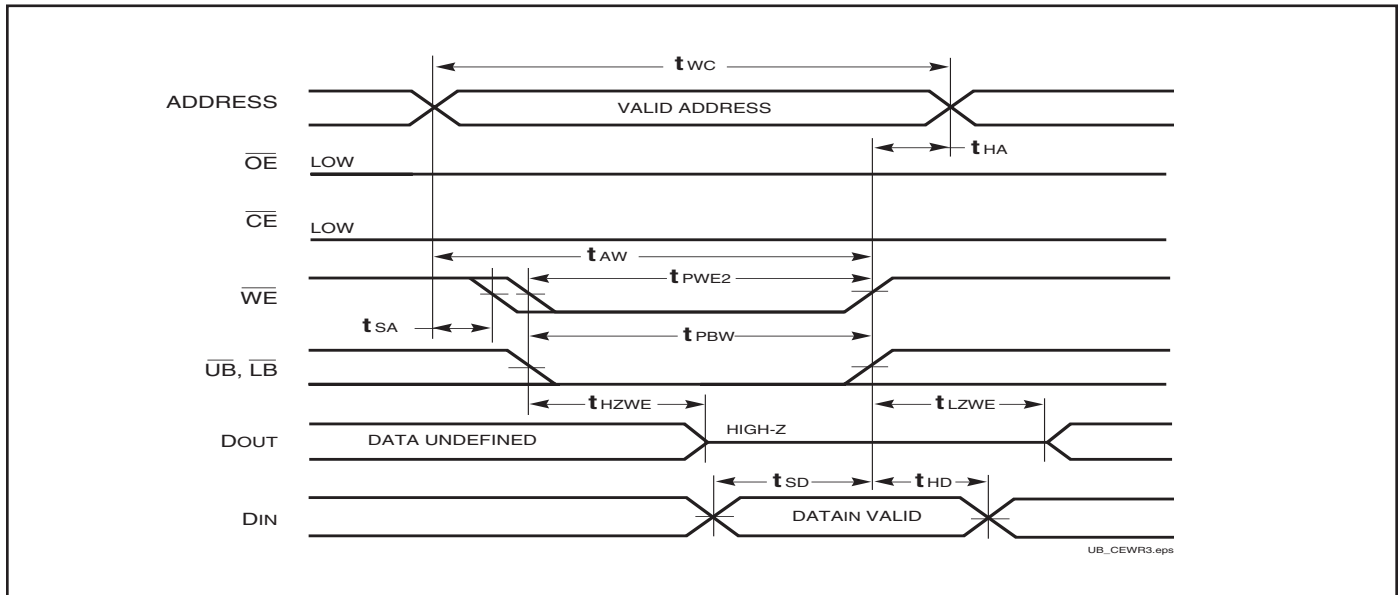
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CE}$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CE}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled. $\overline{OE}$ is HIGH During Write Cycle) ^(1,2)

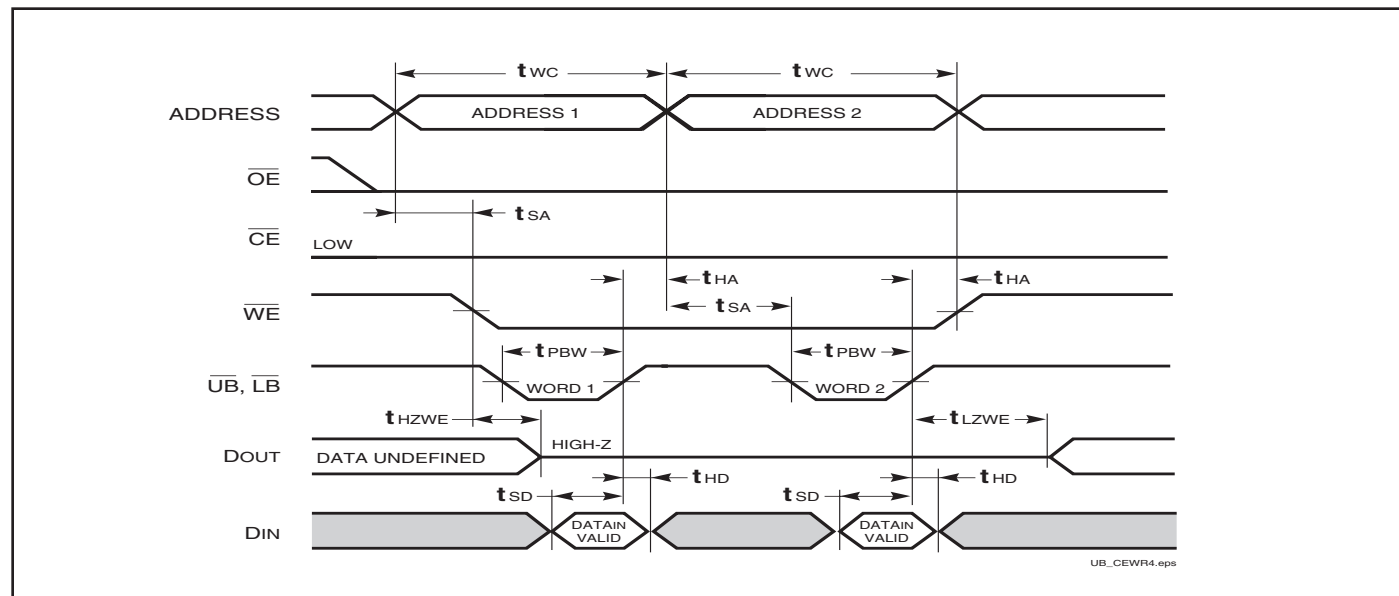


AC WAVEFORMS

WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ is LOW During Write Cycle) ⁽¹⁾



WRITE CYCLE NO. 4 ($\overline{LB}$, $\overline{UB}$ Controlled, Back-to-Back Write) ^(1,3)



Notes:

1. The internal Write time is defined by the overlap of $\overline{CE} = \text{LOW}$, $\overline{UB}$ and/or $\overline{LB} = \text{LOW}$, and $\overline{WE} = \text{LOW}$. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA} , t_{HA} , t_{SD} , and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with $\overline{OE}$ HIGH for a minimum of 4 ns before $\overline{WE} = \text{LOW}$ to place the I/O in a HIGH-Z state.
3. $\overline{WE}$ may be held LOW across many address cycles and the $\overline{LB}$, $\overline{UB}$ pins can be used to control the Write function.

HIGH SPEED (IS61WV12816DALL/DBLL)

DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{DR}	V _{DD} for Data Retention	See Data Retention Waveform		2.0	—	3.6	V
I _{DR}	Data Retention Current	V _{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$	Com. Ind. Auto.	— — —	10 — —	50 70 100	μA
t _{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t _{RDR}	Recovery Time	See Data Retention Waveform		t _{RC}	—	—	ns

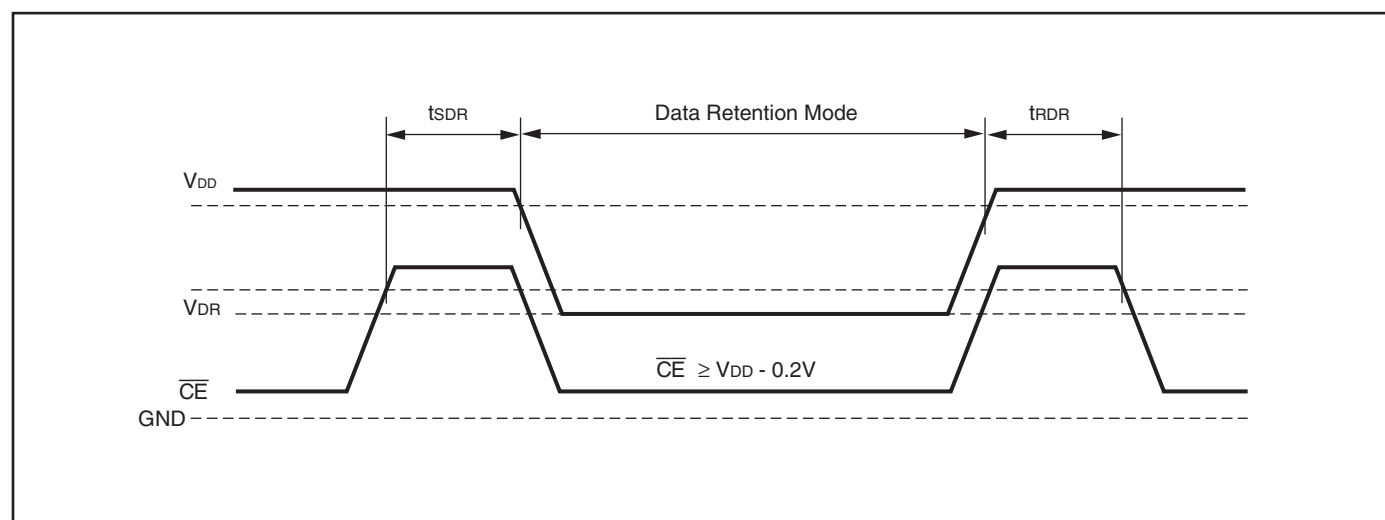
Note 1: Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{DR}	V _{DD} for Data Retention	See Data Retention Waveform		1.2	—	3.6	V
I _{DR}	Data Retention Current	V _{DD} = 1.2V, $\overline{CE} \geq V_{DD} - 0.2V$	Com. Ind. Auto.	— — —	10 — —	50 70 100	μA
t _{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t _{RDR}	Recovery Time	See Data Retention Waveform		t _{RC}	—	—	ns

Note 1: Typical values are measured at V_{DD} = 1.8V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



LOW POWER (IS61WV12816DALS/DBLS)

DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{DR}	V _{DD} for Data Retention	See Data Retention Waveform		2.0	—	3.6	V
I _{DR}	Data Retention Current	V _{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$	Com. Ind. Auto.	— — —	20 — —	40 50 75	μA
t _{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t _{RDR}	Recovery Time	See Data Retention Waveform		t _{RC}	—	—	ns

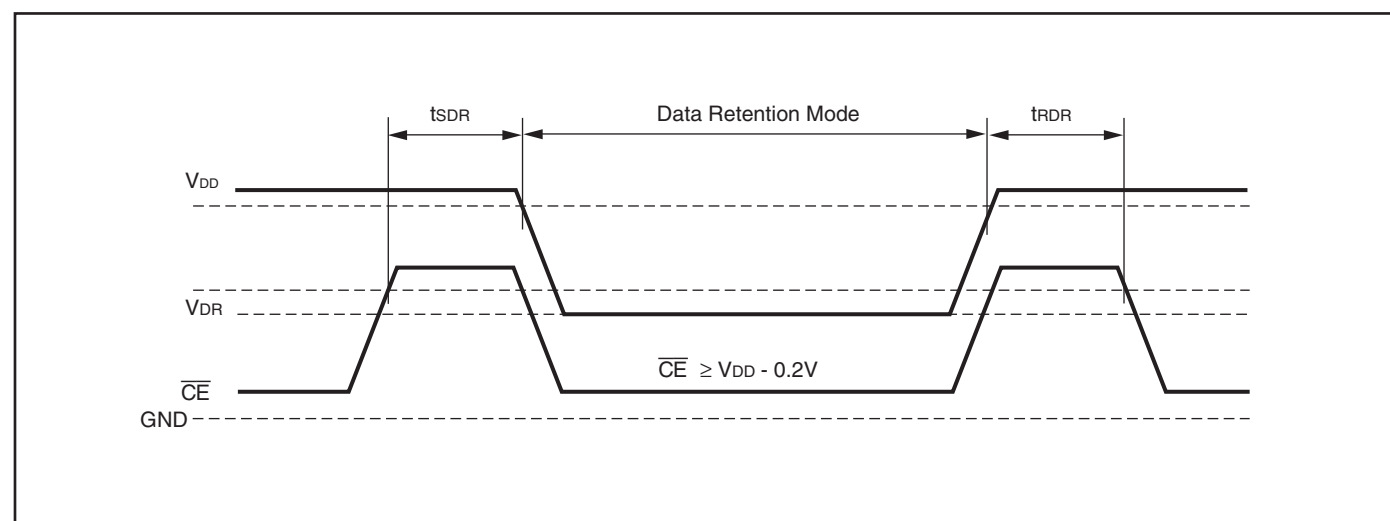
Note 1: Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{DR}	V _{DD} for Data Retention	See Data Retention Waveform		1.2	—	3.6	V
I _{DR}	Data Retention Current	V _{DD} = 1.2V, $\overline{CE} \geq V_{DD} - 0.2V$	Com. Ind. Auto.	— — —	20 — —	40 50 75	μA
t _{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t _{RDR}	Recovery Time	See Data Retention Waveform		t _{RC}	—	—	ns

Note 1: Typical values are measured at V_{DD} = 1.8V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



ORDERING INFORMATION (HIGH SPEED)

Commercial Range: 0°C to +70°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10 (8')	IS61WV12816DBLL-10TL	TSOP (Type II), Lead-free

Note:

1. Speed = 8ns for $V_{DD} = 3.3V \pm 5\%$. Speed = 10ns for $V_{DD} = 2.4V$ to 3.6V.

Industrial Range: -40°C to +85°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10 (8')	IS61WV12816DBLL-10BI	48 mini BGA (6mm x 8mm)
	IS61WV12816DBLL-10BLI	48 mini BGA (6mm x 8mm), Lead-free
	IS61WV12816DBLL-10TI	TSOP (Type II)
	IS61WV12816DBLL-10TLI	TSOP (Type II), Lead-free

Note:

1. Speed = 8ns for $V_{DD} = 3.3V \pm 5\%$. Speed = 10ns for $V_{DD} = 2.4V$ to 3.6V.

Industrial Range: -40°C to +85°C

Voltage Range: 1.65V to 2.2V

Speed (ns)	Order Part No.	Package
20	IS61WV12816DALL-20BI	48 mini BGA (6mm x 8mm)
	IS61WV12816DALL-20TI	TSOP (Type II)

Automotive Range: -40°C to +125°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
12 ($10^{2.3}$)	IS64WV12816DBLL-12BA3	48 mini BGA (6mm x 8mm)
	IS64WV12816DBLL-12BLA3	48 mini BGA (6mm x 8mm), Lead-free
	IS64WV12816DBLL-12CTA3	TSOP (Type II), Copper Leadframe
	IS64WV12816DBLL-12CTLA3	TSOP (Type II), Lead-free, Copper Leadframe

Note:

2. Speed = 10ns for $V_{DD} = 3.3V \pm 5\%$. Speed = 12ns for $V_{DD} = 2.4V$ to 3.6V.

3. Speed = 10ns for $V_{DD} = 2.4V$ to 3.6V and temperature = -40°C to +85°C.

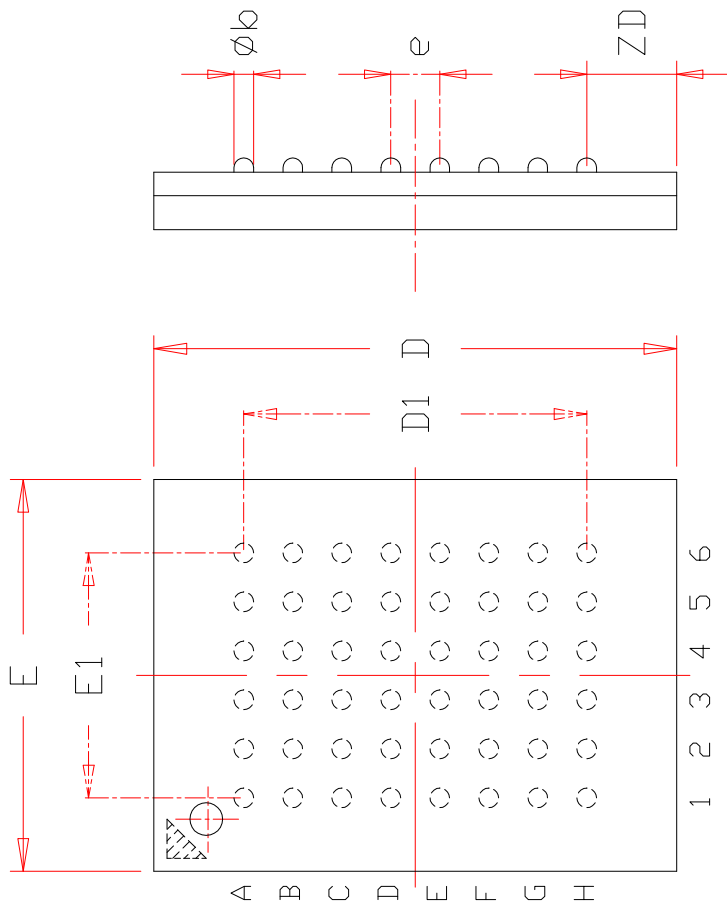
ORDERING INFORMATION (LOW POWER - IN EVALUATION)

Industrial Range: -40°C to +85°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
35	IS61WV12816DBLS-35TLI	TSOP (Type II), Lead-free

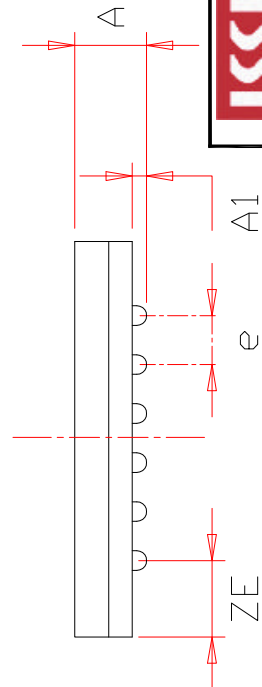
TOP VIEW



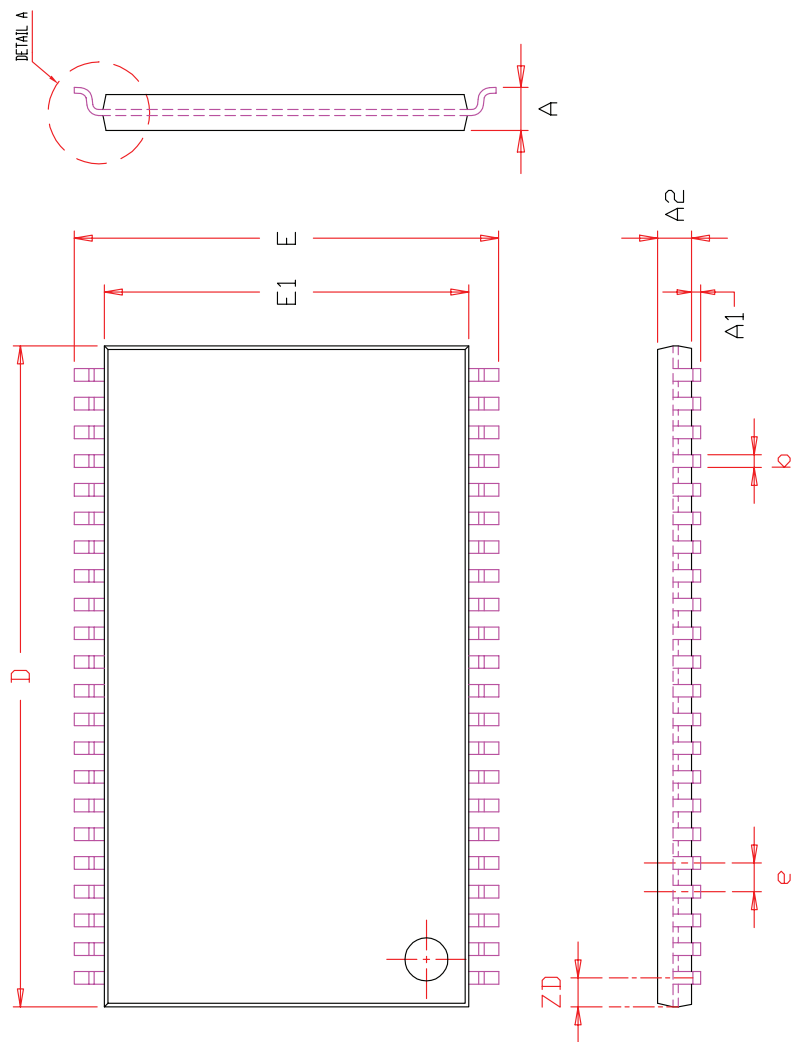
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.20		0.30	0.008		0.012
ϕb	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	5.25	BSC		0.207	BSC	
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.75	BSC		0.148	BSC	
e		0.75	BSC.		0.030	BSC.
ZD		1.375	REF.		0.054	REF.
ZE		1.125	REF.		0.044	REF.

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207



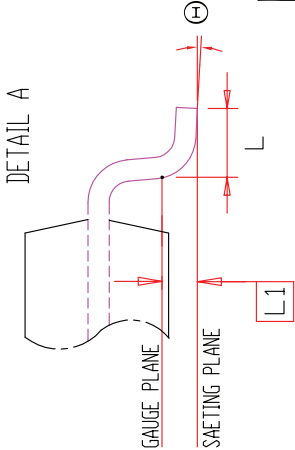
ISSI	TITLE	48L 6x8mm TF-BGA Package Outline	REV.	C	DATE	08/12/2008
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SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00		1.20	0.039		0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.45	0.012		0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e		0.80	BSC.		0.031	BSC.
L	0.40		0.69	0.016		0.027
L1		0.25	BSC.		0.010	BSC.
ZD		0.805	REF.		0.032	REF.
⊖	0		8°	0		8°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.



TITLE

44L 400mil TSOP-2
Package Outline

REV.

F

DATE

06/04/2008