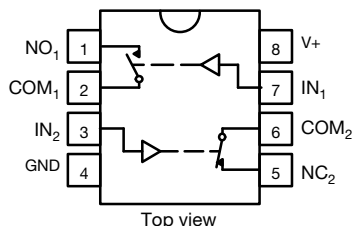
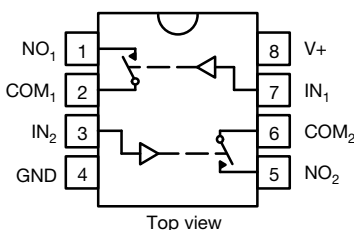
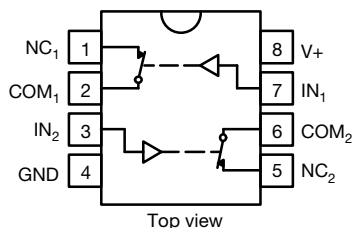


FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

TRUTH TABLE - DG9232E

LOGIC	SWITCH
0	On
1	Off

Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.4 V

TRUTH TABLE - DG9233E

LOGIC	SWITCH
0	Off
1	On

Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.4 V

TRUTH TABLE - DG9234E

LOGIC	SWITCH-1	SWITCH-2
0	Off	On
1	On	Off

Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.4 V

ORDERING INFORMATION

TEMPERATURE RANGE	CONFIGURATION	PACKAGE	PART NUMBER	MINIMUM ORDER / PACKAGE QUANTITY
-40 °C to +85 °C lead (Pb)-free	DG9232E	8-pin MSOP	DG9232EDQ-T1-GE3	Tape and reel 2500 units
		8-pin SOIC	DG9232EDY-T1-GE3	Tape and reel 2500 units
		8-pin SOIC	DG9232EDY-GE3	Tube 500 units
	DG9233E	8-pin MSOP	DG9233EDQ-T1-GE3	Tape and reel 2500 units
		8-pin SOIC	DG9233EDY-T1-GE3	Tape and reel 2500 units
		8-pin SOIC	DG9233EDY-GE3	Tube 500 units
	DG9234E	8-pin MSOP	DG9234EDQ-T1-GE3	Tape and reel 2500 units
		8-pin SOIC	DG9234EDY-T1-GE3	Tape and reel 2500 units
		8-pin SOIC	DG9234EDY-GE3	Tube 500 units

ABSOLUTE MAXIMUM RATINGS

PARAMETER	LIMIT	UNIT
Reference V+ to GND	-0.3 to +6	V
IN, COM, NC, NO ^a	-0.3 to (V+ + 0.3)	
Continuous current (any terminal)	± 20	mA
Peak current (pulsed at 1 ms, 10 % duty cycle)	± 40	
ESD (HBM) (MIL-STD-883, method 3015)	> 8000	V
ESD (CDM) (ANSI / ESDA / JEDEC® JS-002)	> 1000	V
Latch up current, per JESD78	300	mA
Storage temperature	-65 to +125	°C
Power dissipation (packages) ^b	400	mW

Notes

- Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC board.
- Derate 6.5 mW/°C above 70 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



SPECIFICATIONS (V+ = 3 V)							
PARAMETER	SYMBOL	TEST CONDITIONS OTHERWISE UNLESS SPECIFIED V+ = 3 V, ± 10 %, VIN = 0.8 V or 2.4 V e	TEMP. a	D SUFFIX -40 °C to +85 °C			UNIT
				MIN. c	TYP. b	MAX. c	
Analog Switch							
Analog signal range d	VANALOG		Full	0	-	3	V
Drain-source on-resistance	RDS(on)	VNO or VNC = 1.5 V, V+ = 2.7 V ICOM = 5 mA	Room	-	35	50	Ω
			Full	-	35	65	
RDS(on) match d	ΔRDS(on)	VNO or VNC = 1.5 V	Room	-	0.4	2	
RDS(on) flatness d	RDS(on) flatness	VNO or VNC = 1 V and 2 V	Room	-	4	8	
NO or NC off leakage current g	INO/NC(off)	VNO or VNC = 1 V/2 V, VCOM = 2 V/1 V	Room	-100	5	100	pA
			Full	-5000	5	5000	
COM off leakage current g	ICOM(off)	VCOM = 1 V/2 V, VNO or VNC = 2 V/1 V	Room	-100	5	100	
			Full	-5000	5	5000	
Channel-on leakage current g	ICOM(on)	VCOM = VNO or VNC = 1 V/2 V	Room	-200	5	200	
			Full	-10 000	5	10 000	
Digital Control							
Input current	IINL or IINH		Full	-	0.001	-	μA
Dynamic Characteristics							
Turn-on time	tON	VNO or VNC = 1.5 V	Room	-	43	120	ns
			Full	-	-	200	
Turn-off time	tOFF		Room	-	16	50	
			Full	-	-	120	
Charge injection d	QINJ	CL = 1 nF, VGEN = 0 V, RGEN = 0 Ω	Room	-	-0.28	-	pC
Off-isolation	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room	-	-80	-	dB
Crosstalk	XTALK		Room	-	-108	-	
NC and NO capacitance	CS(off)	f = 1 MHz	Room	-	4	-	pF
Channel-on capacitance	CCOM(on)		Room	-	8	-	
COM-off capacitance	CCOM(off)		Room	-	4	-	
Power Supply							
Positive supply range	V+			2.7	-	5.5	V
Power supply current	I+	V+ = 3.3 V, VIN = 0 V or 3.3 V		0.0003	-	1	μA

Notes

- a. Room = 25 °C, full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Difference of min. and max. values.
g. Guaranteed by 5 V leakage tests, not production tested.



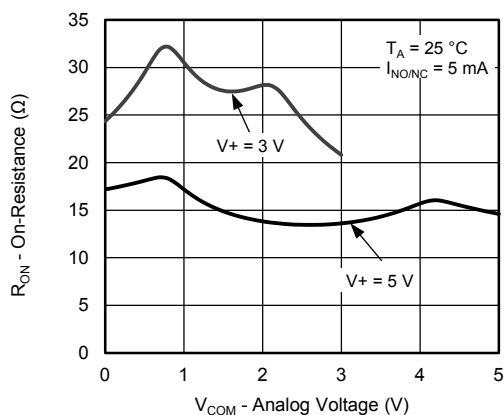
SPECIFICATIONS (V+ = 5 V)							
PARAMETER	SYMBOL	TEST CONDITIONS OTHERWISE UNLESS SPECIFIED V+ = 5 V, ± 10 %, VIN = 0.8 V or 2.4 V ^e	TEMP. ^a	D SUFFIX -40 °C to +85°C			UNIT
				MIN. ^c	TYP. ^b	MAX. ^c	
Analog Switch							
Analog signal range ^d	VANALOG		Full	0	-	5	V
Drain-source on-resistance	RDS(on)	VNO or VNC = 3.5 V, V+ = 4.5 V ICOM = 5 mA	Room	-	17	25	Ω
			Full	-	17	35	
RDS(on) match ^d	ΔRDS(on)	VNO or VNC = 3.5 V	Room	-	0.4	2	
RDS(on) flatness ^d	RDS(on) flatness	VNO or VNC = 1 V, 2 V, and 3 V	Room	-	3.5	6	
NO or NC off leakage current ^g	INO/NC(off)	VNO or VNC = 1 V/4 V, VCOM = 4 V/1 V	Room	-100	10	100	pA
			Full	-5000	10	5000	
COM off leakage current	ICOM(off)	VCOM = 1 V/4 V, VNO or VNC = 4 V/1 V	Room	-100	10	100	
			Full	-5000	10	5000	
Channel-on leakage current	ICOM(on)	VCOM = VNO or VNC = 1 V/4 V	Room	-200	-	200	
			Full	-10 000	-	10 000	
Digital Control							
Input current	IINL or IINH		Full	-	0.001	-	μA
Dynamic Characteristics							
Turn-on time	tON	VNO or VNC = 3 V	Room	-	32	75	ns
			Full	-	-	150	
Turn-off time	tOFF		Room	-	10	50	
			Full	-	-	100	
Charge injection ^d	QINJ	CL = 1 nF, VGEN = 0 V, RGEN = 0 Ω	Room	-	-0.78	-	pC
Off-isolation	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room	-	-80	-	dB
Crosstalk	XTALK		Room	-	-108	-	
NC and NO capacitance	C(off)	f = 1 MHz	Room	-	3.8	-	pF
Channel-on capacitance	CD(on)		Room	-	7.8	-	
COM-off capacitance	CD(off)		Room	-	3.8	-	
Power Supply							
Positive supply range	V+			2.7	-	5.5	V
Power supply current	I+	V+ = 5.5 V, VIN = 0 V or 5.5 V		-	-	1	μA

Notes

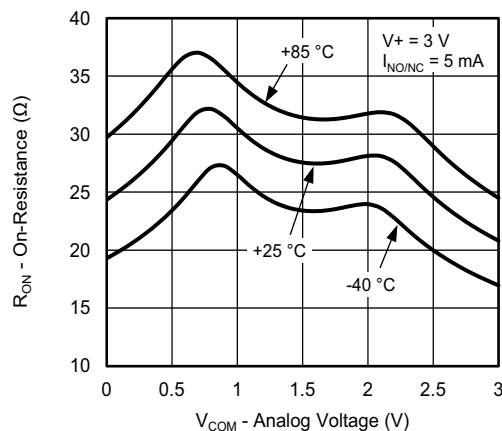
- a. Room = 25 °C, full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Difference of min. and max. values.



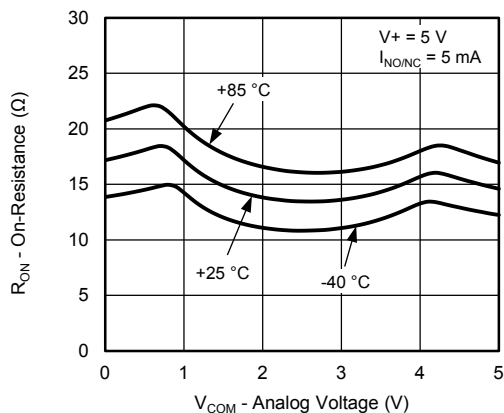
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



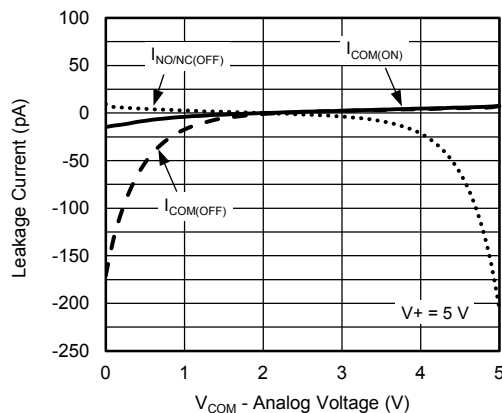
On-Resistance vs. Analog Voltage



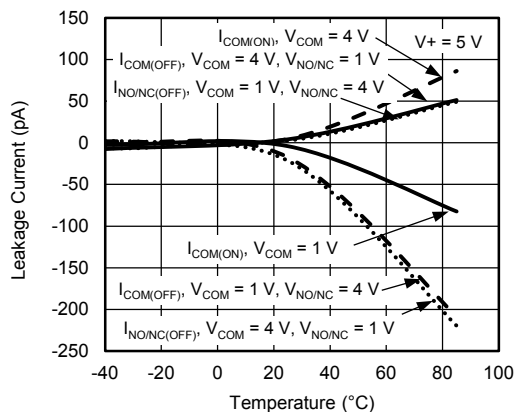
On-Resistance vs. Analog Voltage



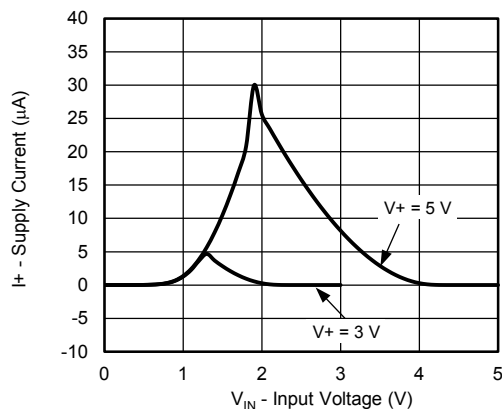
On-Resistance vs. Analog Voltage



Leakage Current vs. Analog Voltage



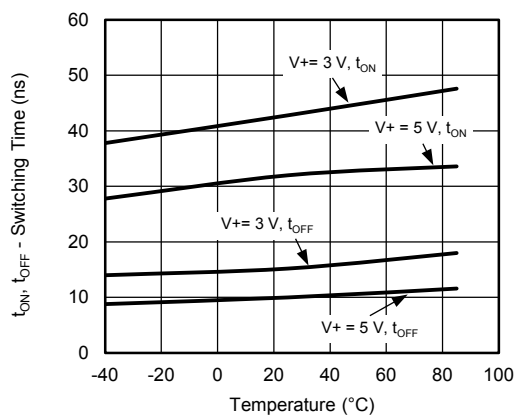
Leakage Current vs. Temperature



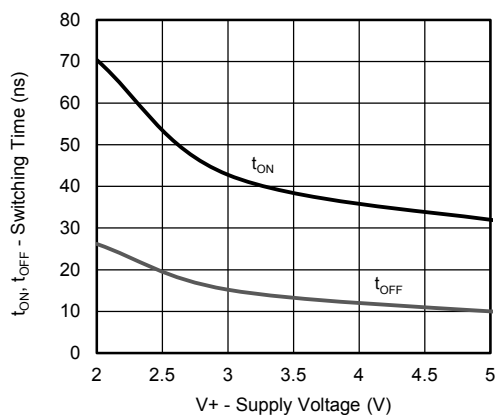
Supply Current vs. Input Voltage



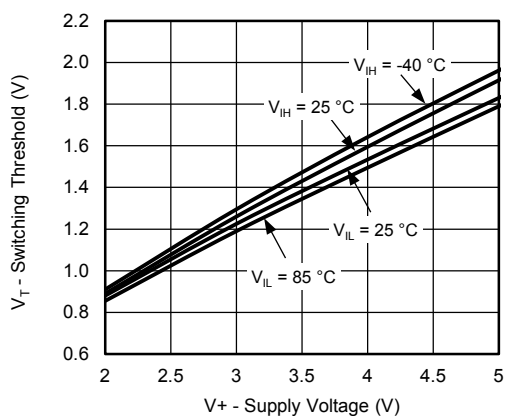
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



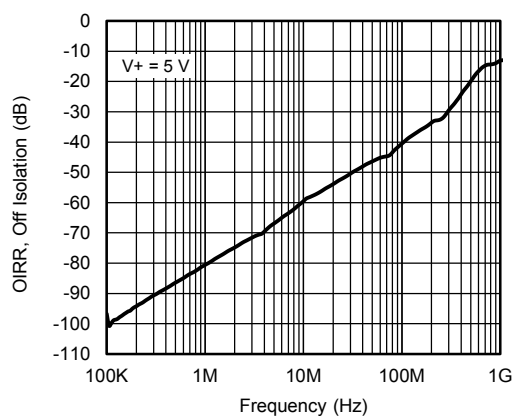
Switching Time vs. Temperature



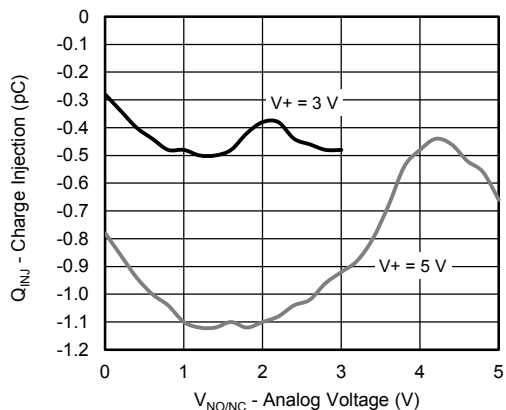
Switching Time vs. Supply Voltage



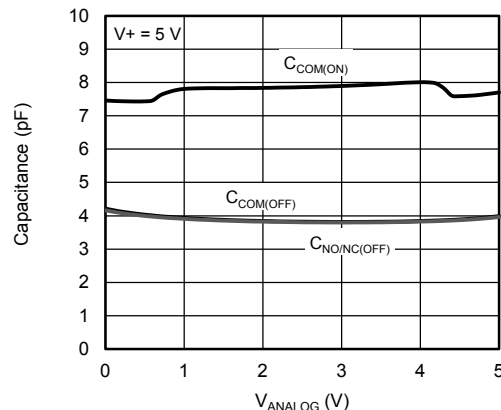
Switching Threshold vs. Supply Voltage



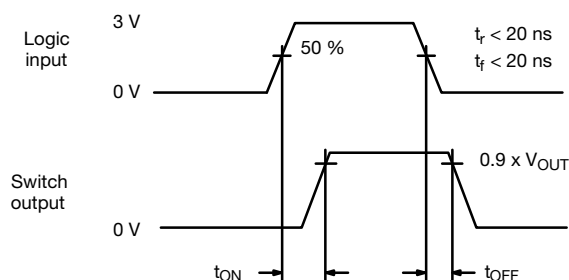
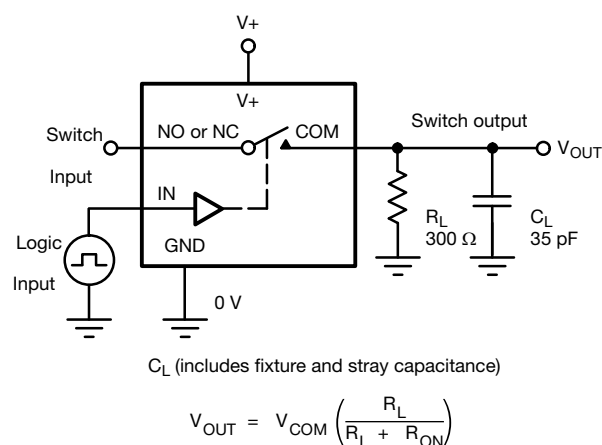
OIRR, Off Isolation vs. Frequency



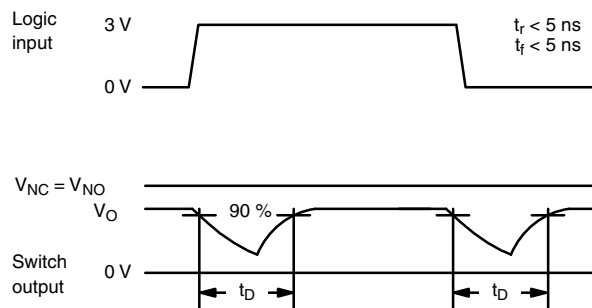
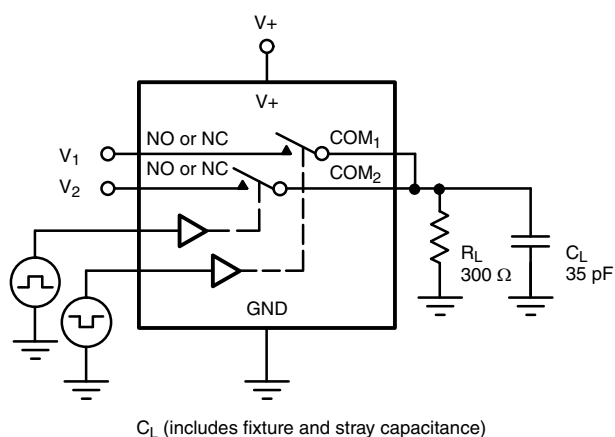
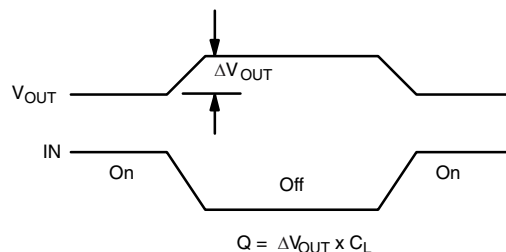
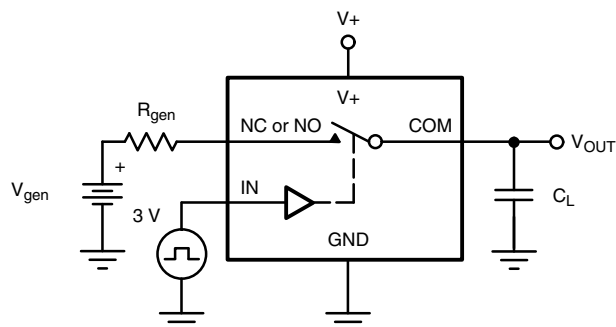
Charge Injection vs. Analog Voltage



Capacitance

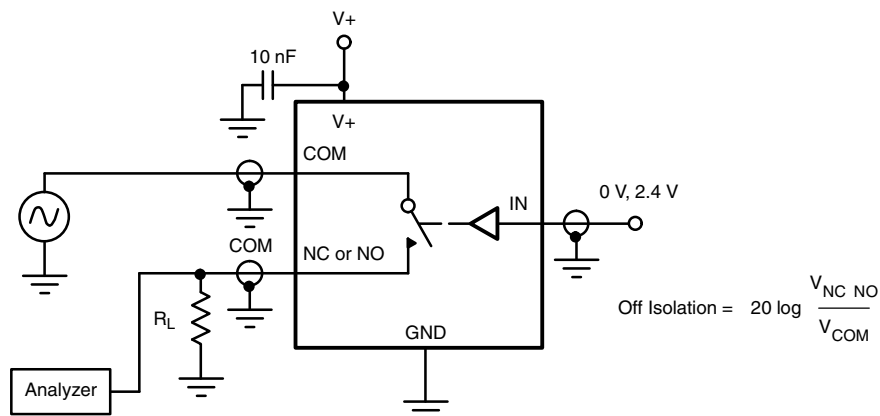
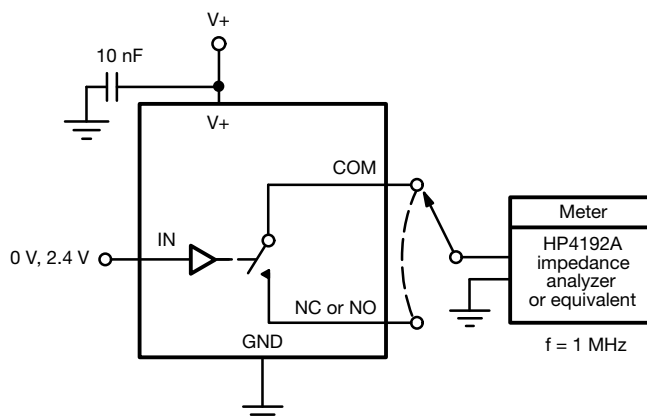
TEST CIRCUITS


Logic "1" = switch on
Logic input waveforms inverted for switches that have the opposite logic sense.

Fig. 1 - Switching Time

Fig. 2 - Break-Before-Make Interval


IN depends on switch configuration: input polarity determined by sense of switch.

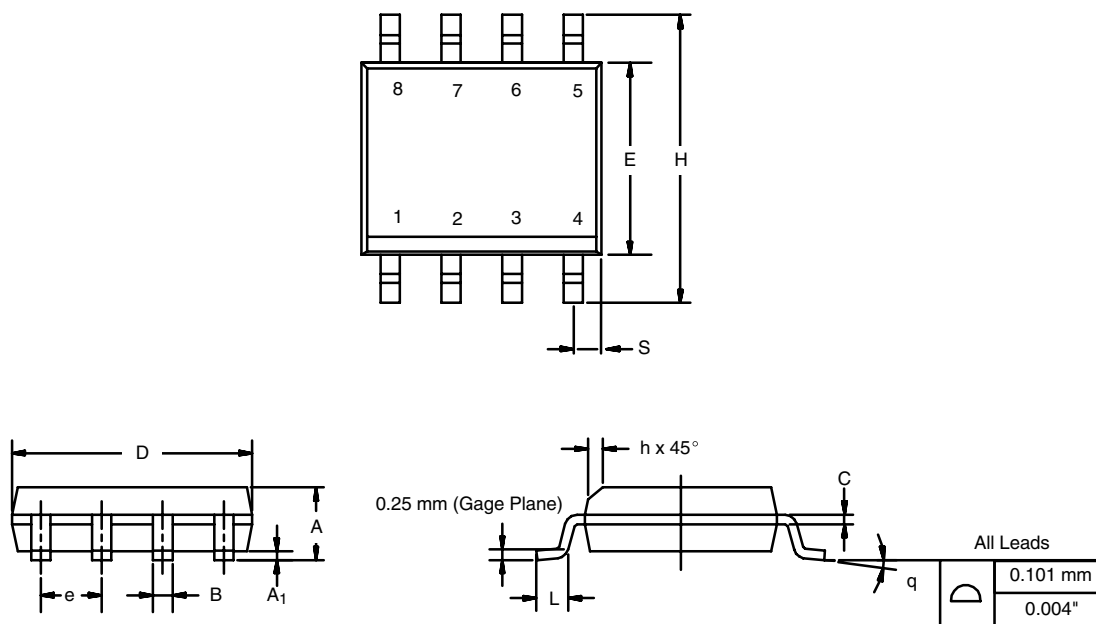
Fig. 3 - Charge Injection

TEST CIRCUITS

Fig. 4 - Off-Isolation

Fig. 5 - Channel Off/On Capacitance

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SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012

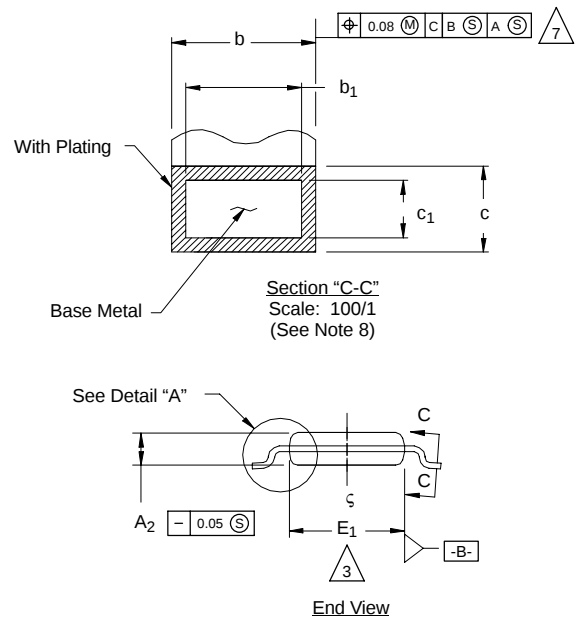
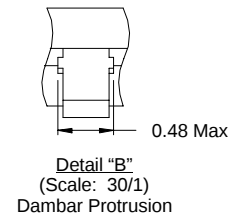
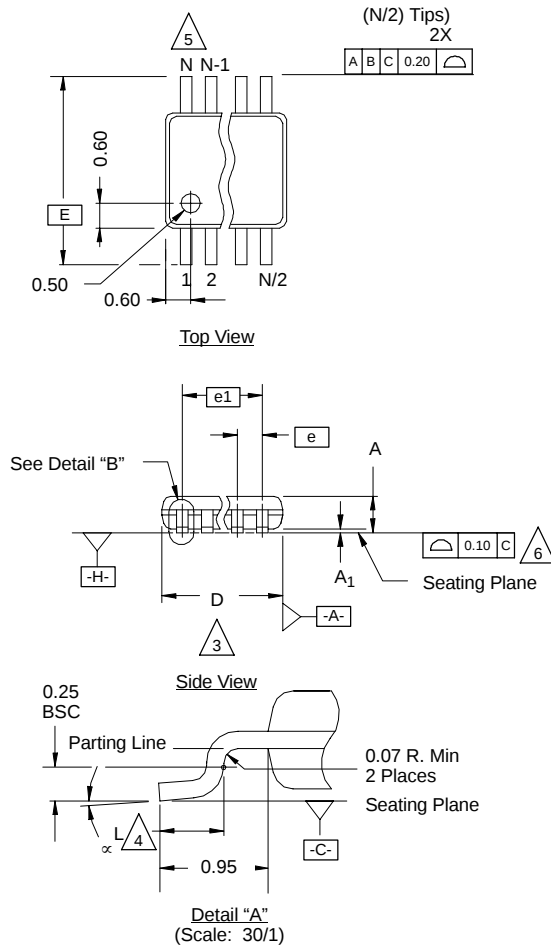


DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				



MSOP: 8-LEADS

JEDEC Part Number: MO-187, (Variation AA and BA)



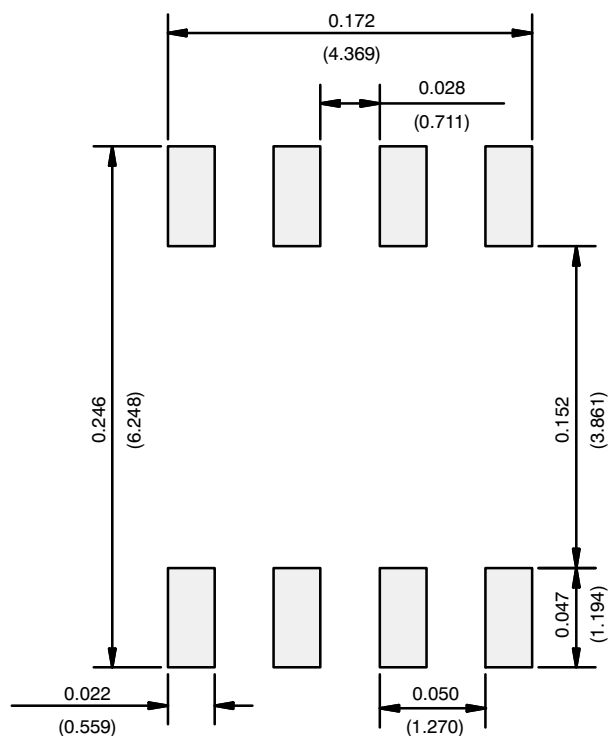
NOTES:

- Die thickness allowable is 0.203 ± 0.0127 .
- Dimensioning and tolerances per ANSI.Y14.5M-1994.
- Dimensions "D" and "E₁" do not include mold flash or protrusions, and are measured at Datum plane $\square\text{H}\square$, mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimension is the length of terminal for soldering to a substrate.
- Terminal positions are shown for reference only.
- Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
- The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
- Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
- Controlling dimension: millimeters.
- This part is compliant with JEDEC registration MO-187, variation AA and BA.
- Datums $\square\text{A}\square$ and $\square\text{B}\square$ to be determined Datum plane $\square\text{H}\square$.
- Exposed pad area in bottom side is the same as the leadframe pad size.

N = 8L

Dim	MILLIMETERS			Note
	Min	Nom	Max	
A	-	-	1.10	
A ₁	0.05	0.10	0.15	
A ₂	0.75	0.85	0.95	
b	0.25	-	0.38	8
b ₁	0.25	0.30	0.33	8
c	0.13	-	0.23	
c ₁	0.13	0.15	0.18	
D	3.00 BSC			3
E	4.90 BSC			
E ₁	2.90	3.00	3.10	3
e	0.65 BSC			
e ₁	1.95 BSC			
L	0.40	0.55	0.70	4
N	8			5
α	0°	4°	6°	
ECN: T-02080—Rev. C, 15-Jul-02				
DWG: 5867				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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