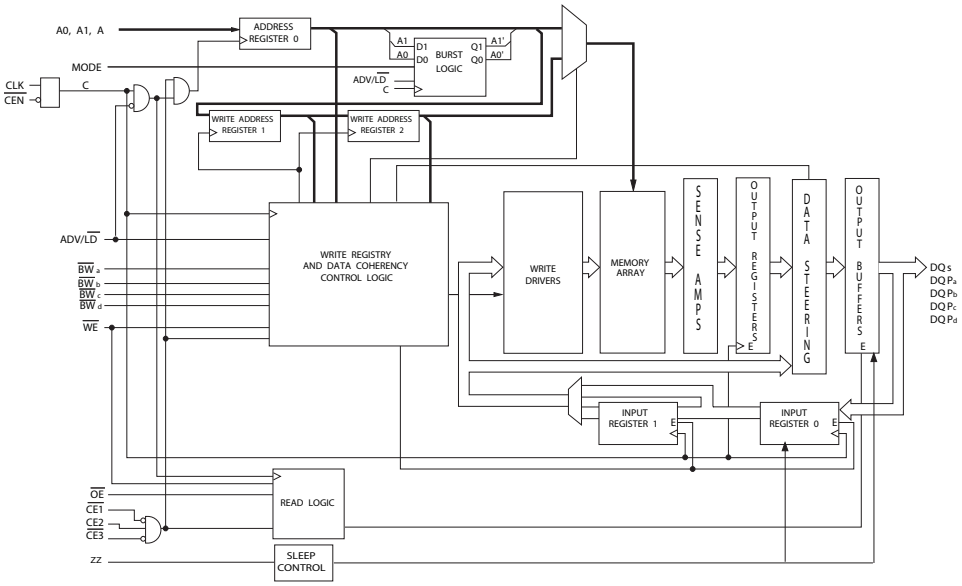
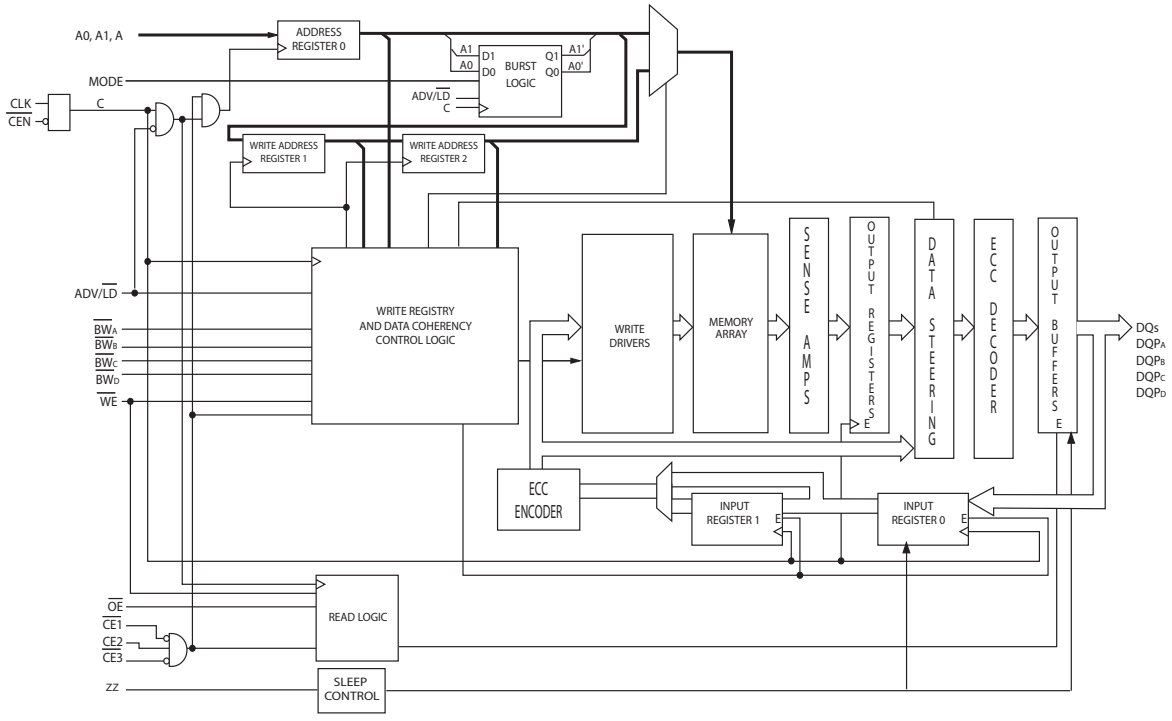
Logic Block Diagram – CY7C1370KV33

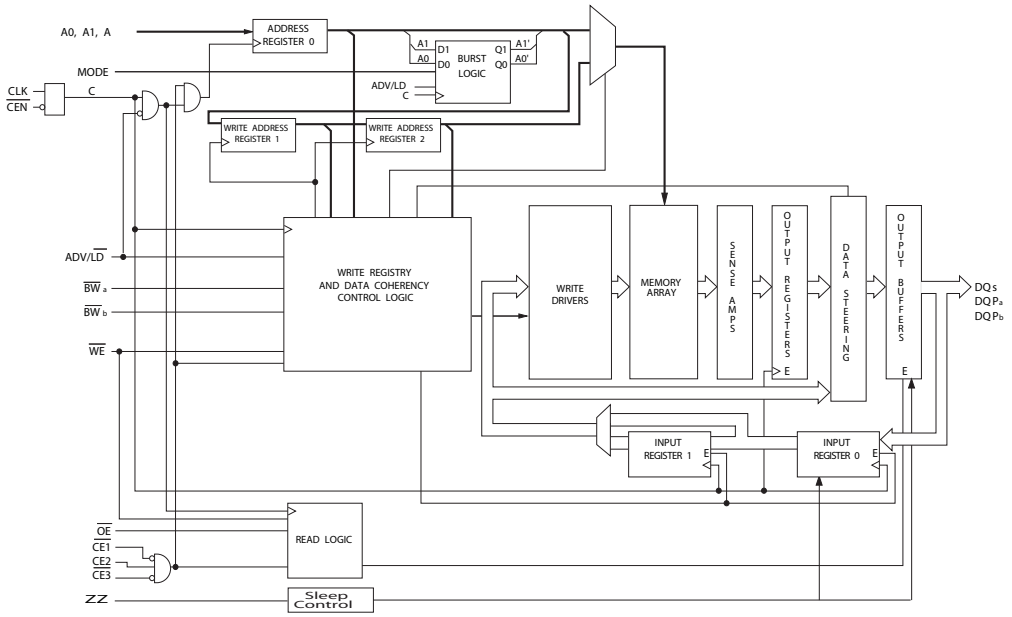


Logic Block Diagram – CY7C1370KVE33

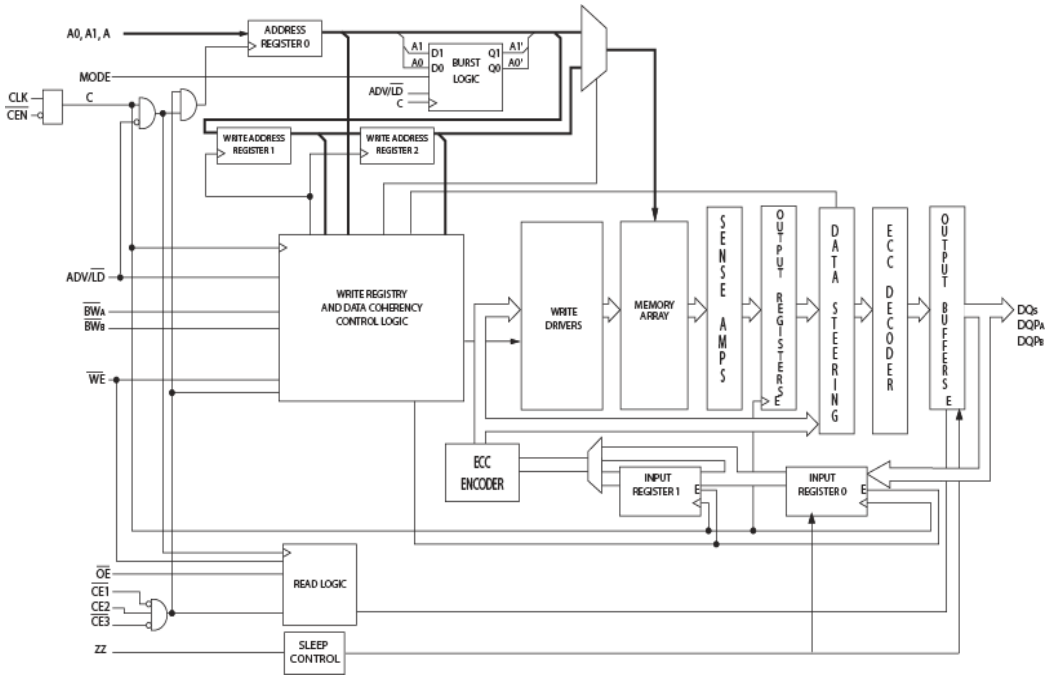


Downloaded from Arrow.com.

Logic Block Diagram – CY7C1372KV33



Logic Block Diagram – CY7C1372KVE33



Downloaded from Arrow.com.

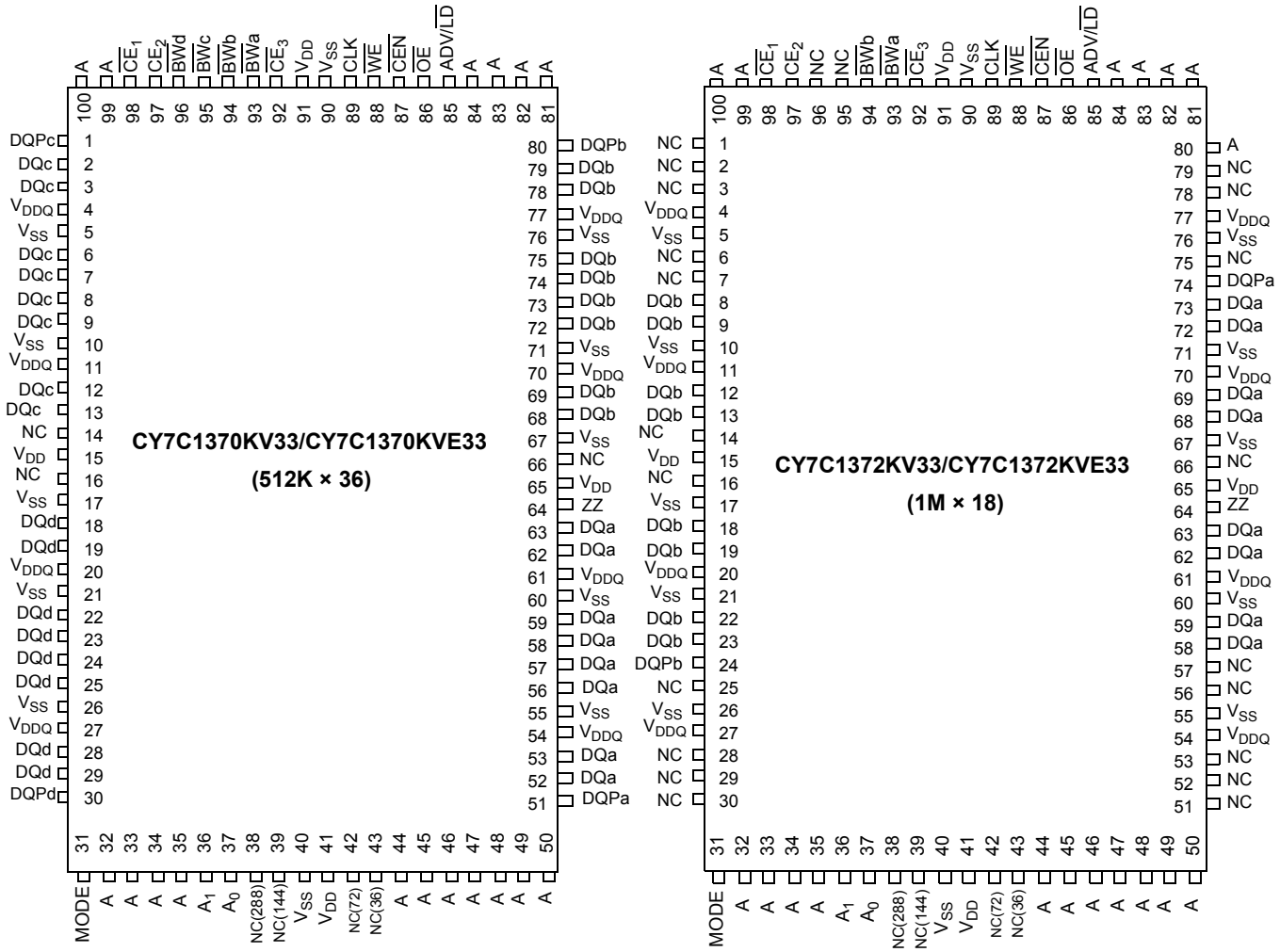
Contents

Pin Configurations **5**
Pin Definitions **7**
Functional Overview **9**
Single Read Accesses 9
Burst Read Accesses 9
Single Write Accesses 9
Burst Write Accesses 10
Sleep Mode 10
Interleaved Burst Address Table 10
Linear Burst Address Table 10
ZZ Mode Electrical Characteristics 10
Truth Table **11**
Partial Write Cycle Description **12**
Partial Write Cycle Description **12**
IEEE 1149.1 Serial Boundary Scan (JTAG) **13**
Disabling the JTAG Feature 13
Test Access Port (TAP) 13
PERFORMING A TAP RESET 13
TAP REGISTERS 13
TAP Instruction Set 14
TAP Controller State Diagram **15**
TAP Controller Block Diagram **16**
TAP Timing **16**
TAP AC Switching Characteristics **17**
3.3 V TAP AC Test Conditions **18**
3.3 V TAP AC Output Load Equivalent **18**
2.5 V TAP AC Test Conditions **18**
2.5 V TAP AC Output Load Equivalent **18**
TAP DC Electrical Characteristics and Operating Conditions **18**
Identification Register Definitions **19**
Scan Register Sizes **19**
Identification Codes **19**
Boundary Scan Order **20**
Maximum Ratings **21**
Operating Range **21**
Neutron Soft Error Immunity **21**
Electrical Characteristics **21**
Capacitance **23**
Thermal Resistance **23**
AC Test Loads and Waveforms **23**
Switching Characteristics **24**
Switching Waveforms **25**
Ordering Information **27**
Ordering Code Definitions 27
Package Diagrams **28**
Acronyms **30**
Document Conventions **30**
Units of Measure 30
Document History Page **31**
Sales, Solutions, and Legal Information **32**
Worldwide Sales and Design Support 32
Products 32
PSoC®Solutions 32
Cypress Developer Community 32
Technical Support 32

Downloaded from Arrow.com.

Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout



Downloaded from Arrow.com.

Pin Configurations (continued)

Figure 2. 165-ball FBGA (13 × 15 × 1.4 mm) pinout

CY7C1370KV33 (512K × 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/576M	A	$\overline{CE}_1$	$\overline{BW}_c$	$\overline{BW}_b$	$\overline{CE}_3$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	NC
B	NC/1G	A	CE2	$\overline{BW}_d$	$\overline{BW}_a$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
C	DQP_c	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_b
D	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
E	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
F	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
G	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
K	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
L	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
M	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
N	DQP_d	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DQP_a
P	NC/144M	NC/72M	A	A	TDI	A1	TDO	A	A	A	NC/288M
R	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

Downloaded from Arrow.com.

Pin Definitions

Pin Name	I/O Type	Pin Description
A_0, A_1, A	Input-synchronous	**Address inputs used to select one of the address locations**. Sampled at the rising edge of the CLK.
$\overline{BW}_a$, $\overline{BW}_b$, $\overline{BW}_c$, $\overline{BW}_d$	Input-synchronous	**Byte write select inputs, active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK. $\overline{BW}_a$ controls DQ_a and DQP_a, $\overline{BW}_b$ controls DQ_b and DQP_b, $\overline{BW}_c$ controls DQ_c and DQP_c, $\overline{BW}_d$ controls DQ_d and DQP_d.
$\overline{WE}$	Input-synchronous	**Write enable input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input-synchronous	**Advance/load input used to advance the on-chip address counter or load a new address**. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should be driven LOW in order to load a new address.
CLK	Input-clock	**Clock input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input-synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device.
CE_2	Input-synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$	Input-synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input-asynchronous	**Output enable, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state and when the device has been deselected.
$\overline{CEN}$	Input-synchronous	**Clock enable input, active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
DQ_S	I/O-synchronous	**Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[17:0]}$ during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQ_a–DQ_d are placed in a tristate condition. The outputs are automatically tristated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	I/O-synchronous	**Bidirectional data parity I/O lines**. Functionally, these signals are identical to DQ_s. During write sequences, DQP_a is controlled by $\overline{BW}_a$, DQP_b is controlled by $\overline{BW}_b$, DQP_c is controlled by $\overline{BW}_c$, and DQP_d is controlled by $\overline{BW}_d$.
MODE	Input strap pin	**Mode input**. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE will default HIGH, to an interleaved burst order.

Downloaded from Arrow.com.

Pin Definitions (continued)

Pin Name	I/O Type	Pin Description
TDO	JTAG serial output synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK.
TDI	JTAG serial input synchronous	**Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK.
TMS	Test mode select synchronous	**This pin controls the test access port state machine**. Sampled on the rising edge of TCK.
TCK	JTAG-clock	**Clock input to the JTAG circuitry**.
V_{DD}	Power supply	**Power supply inputs to the core of the device**.
V_{DDQ}	I/O power supply	**Power supply for the I/O circuitry**.
V_{SS}	Ground	**Ground for the device**. Should be connected to ground of the system.
NC	–	**No connects**. This pin is not connected to the die.
NC/(36M, 72M, 144M, 288M, 576M, 1G)	–	**These pins are not connected**. They will be used for expansion to the 36M, 72M, 144M, 288M, 576M and 1G densities.
ZZ	Input-asynchronous	**ZZ "sleep" input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. During normal operation, this pin can be connected to V_{SS} or left floating. ZZ pin has an internal pull down.

Downloaded from Arrow.com.

Functional Overview

The CY7C1370KV33, CY7C1370KVE33, CY7C1372KVE33 and CY7C1372KV33 are synchronous-pipelined burst NoBL SRAMs designed specifically to eliminate wait states during write/read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 2.5 ns (250-MHz device).

Accesses can be initiated by asserting all three chip enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) active at the rising edge of the clock. If clock enable ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device will be latched. The access can either be a read or write operation, depending on the status of the write enable ($\overline{WE}$). $\overline{BW_X}$ can be used to conduct byte write operations.

Write operations are qualified by the write enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous output enable ($\overline{OE}$) simplify depth expansion. All operations (reads, writes, and deselects) are pipelined. ADV/$\overline{LD}$ should be driven LOW once the device has been deselected in order to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active, (3) the write enable input signal $\overline{WE}$ is deasserted HIGH, and (4) ADV/$\overline{LD}$ is asserted LOW. The address presented to the address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 2.5 ns (250-MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW in order for the device to drive out the requested data. During the second clock, a subsequent operation (read/write/deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output will tristate following the next clock rise.

Burst Read Accesses

The CY7C1370KV33, CY7C1370KVE33, CY7C1372KVE33 and CY7C1372KV33 have an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW in order to load a new address into the SRAM, as described in Single Read Accesses. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and will wrap-around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ will increment the internal burst counter regardless of the state of chip enables inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active, and (3) the write signal $\overline{WE}$ is asserted LOW. The address presented is loaded into the address register. The write signals are latched into the control logic block.

On the subsequent clock rise the data lines are automatically tristated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1370KV33, CY7C1370KVE33, and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1372KV33, CY7C1372KVE33). In addition, the address for the subsequent access (read/write/deselect) is latched into the address register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1370KV33, CY7C1370KVE33 & $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1372KV33, CY7C1372KVE33) (or a subset for byte write operations, see Write Cycle Description table for details) inputs is latched into the device and the write is complete.

The data written during the write operation is controlled by $\overline{BW}$ ($\overline{BW_{a,b,c,d}}$ for CY7C1370KV33, CY7C1370KVE33 and $\overline{BW_{a,b}}$ for CY7C1372KV33, CY7C1372KVE33) signals.

The CY7C1370KV33 / CY7C1370KVE33 / CY7C1372KV33 / CY7C1372KVE33 provides byte write capability that is described in the Write Cycle Description table. Asserting the write enable input ($\overline{WE}$) with the selected byte write select ($\overline{BW}$) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included in order to greatly simplify read/modify/write sequences, which can be reduced to simple byte write operations.

Because the CY7C1370KV33, CY7C1370KVE33 and CY7C1372KV33, CY7C1372KVE33 are common I/O devices, data should not be driven into the device while the outputs are active. The output enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1370KV33, CY7C1370KVE33 and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1372KV33, CY7C1372KVE33) inputs. Doing so will tri-state the output drivers. As a safety precaution, DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1370KV33, CY7C1370KVE33 and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1372KV33, CY7C1372KVE33) are automatically tristated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

Downloaded from Arrow.com.

Burst Write Accesses

The CY7C1370KV33 / CY7C1370KVE33 / CY7C1372KV33 / CY7C1372KVE33 has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four write operations without reasserting the address inputs. ADV/LD must be driven LOW in order to load the initial address, as described in the Single Write Accesses section above. When ADV/LD is driven HIGH on the subsequent clock rise, the chip enables ($\overline{CE}_1$, CE_2, and $\overline{CE}_3$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct $\overline{BW}$ ($\overline{BW}_{a,b,c,d}$ for CY7C1370KV33, CY7C1370KVE33 and $\overline{BW}_{a,b}$ for CY7C1372KV33, CY7C1372KVE33) inputs must be driven in each cycle of the burst write in order to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE}_1$, CE_2, and $\overline{CE}_3$, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2$ V	–	65	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2$ V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2$ V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

Downloaded from Arrow.com.

Truth Table

The Truth Table for CY7C1370KV33/CY7C1370KVE33 and CY7C1372KV33/CY7C1372KVE33 follows. [1, 2, 3, 4, 5, 6, 7]

Operation	Address Used	$\overline{CE}$	ZZ	ADV/$\overline{LD}$	$\overline{WE}$	$\overline{BW_x}$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect cycle	None	H	L	L	X	X	X	L	L–H	Tri-state
Continue deselect cycle	None	X	L	H	X	X	X	L	L–H	Tri-state
Read cycle (begin burst)	External	L	L	L	H	X	L	L	L–H	Data out (Q)
Read cycle (continue burst)	Next	X	L	H	X	X	L	L	L–H	Data out (Q)
NOP/dummy read (begin burst)	External	L	L	L	H	X	H	L	L–H	Tri-state
Dummy read (continue burst)	Next	X	L	H	X	X	H	L	L–H	Tri-state
Write cycle (begin burst)	External	L	L	L	L	L	X	L	L–H	Data in (D)
Write cycle (continue burst)	Next	X	L	H	X	L	X	L	L–H	Data in (D)
NOP/write abort (begin burst)	None	L	L	L	L	H	X	L	L–H	Tri-state
Write abort (continue burst)	Next	X	L	H	X	H	X	L	L–H	Tri-state
Ignore clock edge (stall)	Current	X	L	X	X	X	X	H	L–H	–
Sleep mode	None	X	H	X	X	X	X	X	X	Tri-state

Notes
1. X = “Don't Care”, H = Logic HIGH, L = Logic LOW, $\overline{CE}$ stands for ALL Chip Enables active. $\overline{BW}$x = L signifies at least one Byte Write Select is active, $\overline{BW}$x = Valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
2. Write is defined by $\overline{WE}$ and $\overline{BW_X}$. See Write Cycle Description table for details.
3. When a write cycle is detected, all I/Os are tristated, even during byte writes.
4. The DQ and DQP pins are controlled by the current cycle and the $\overline{OE}$ signal.
5. $\overline{CEN}$ = H inserts wait states.
6. Device will power-up deselected and the I/Os in a tristate condition, regardless of $\overline{OE}$.
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQ_s and DQP_X = Tri-state when $\overline{OE}$ is inactive or when the device is deselected, and DQ_s = data when $\overline{OE}$ is active.

Downloaded from Arrow.com.

Partial Write Cycle Description

The Partial Write Cycle Description for CY7C1370KV33/CY7C1370KVE33 follows. [8, 9, 10, 11]

Function (CY7C1370KV33/CY7C1370KVE33)	$\overline{WE}$	$\overline{BW_d}$	$\overline{BW_c}$	$\overline{BW_b}$	$\overline{BW_a}$
Read	H	X	X	X	X
Write – No bytes written	L	H	H	H	H
Write Byte a – (DQ_a and DQP_a)	L	H	H	H	L
Write Byte b – (DQ_b and DQP_b)	L	H	H	L	H
Write Bytes b, a	L	H	H	L	L
Write Byte c – (DQ_c and DQP_c)	L	H	L	H	H
Write Bytes c, a	L	H	L	H	L
Write Bytes c, b	L	H	L	L	H
Write Bytes c, b, a	L	H	L	L	L
Write Byte d – (DQ_d and DQP_d)	L	L	H	H	H
Write Bytes d, a	L	L	H	H	L
Write Bytes d, b	L	L	H	L	H
Write Bytes d, b, a	L	L	H	L	L
Write Bytes d, c	L	L	L	H	H
Write Bytes d, c, a	L	L	L	H	L
Write Bytes d, c, b	L	L	L	L	H
Write All Bytes	L	L	L	L	L

Partial Write Cycle Description

The Partial Write Cycle Description for CY7C1372KV33/CY7C1372KVE33 follows. [8, 9, 10, 11]

Function (CY7C1372KV33/CY7C1372KVE33)	$\overline{WE}$	$\overline{BW_b}$	$\overline{BW_a}$
Read	H	X	X
Write – No Bytes Written	L	H	H
Write Byte a – (DQ_a and DQP_a)	L	H	L
Write Byte b – (DQ_b and DQP_b)	L	L	H
Write Both Bytes	L	L	L

Notes
8. X = “Don't Care”, H = Logic HIGH, L = Logic LOW, $\overline{CE}$ stands for ALL Chip Enables active. $\overline{BW}$x = L signifies at least one Byte Write Select is active, $\overline{BW}$x = Valid signifies that the desired byte write selects are asserted, see Truth Table on page 11 for details.
9. Write is defined by $\overline{WE}$ and $\overline{BW}_X$. See Write Cycle Description table for details.
10. When a write cycle is detected, all I/Os are tristated, even during byte writes.
11. Table only lists a partial listing of the byte write combinations. Any Combination of $\overline{BW}_X$ is valid Appropriate write will be done based on which byte write is active.

Downloaded from Arrow.com.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1370KV33 incorporates a serial boundary scan test access port (TAP). This part is fully compliant with 1149.1. The TAP operates using JEDEC-standard 3.3 V or 2.5 V I/O logic levels.

The CY7C1370KV33 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This Reset does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the TAP Controller Block Diagram on page 16. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

Downloaded from Arrow.com.

TAP Instruction Set

Overview

Eight different instructions are possible with the three bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the shift-DR controller state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1-mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required – that is, while data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST Output Bus Tristate

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tristate mode.

The boundary scan register has a special bit located at bit #89 (for 165-ball FBGA package). When this scan cell, called the "extest output bus tristate," is latched into the preload register during the "Update-DR" state in the TAP controller, it will directly control the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it will enable the output buffers to drive the output bus. When LOW, this bit will place the output bus into a High Z condition.

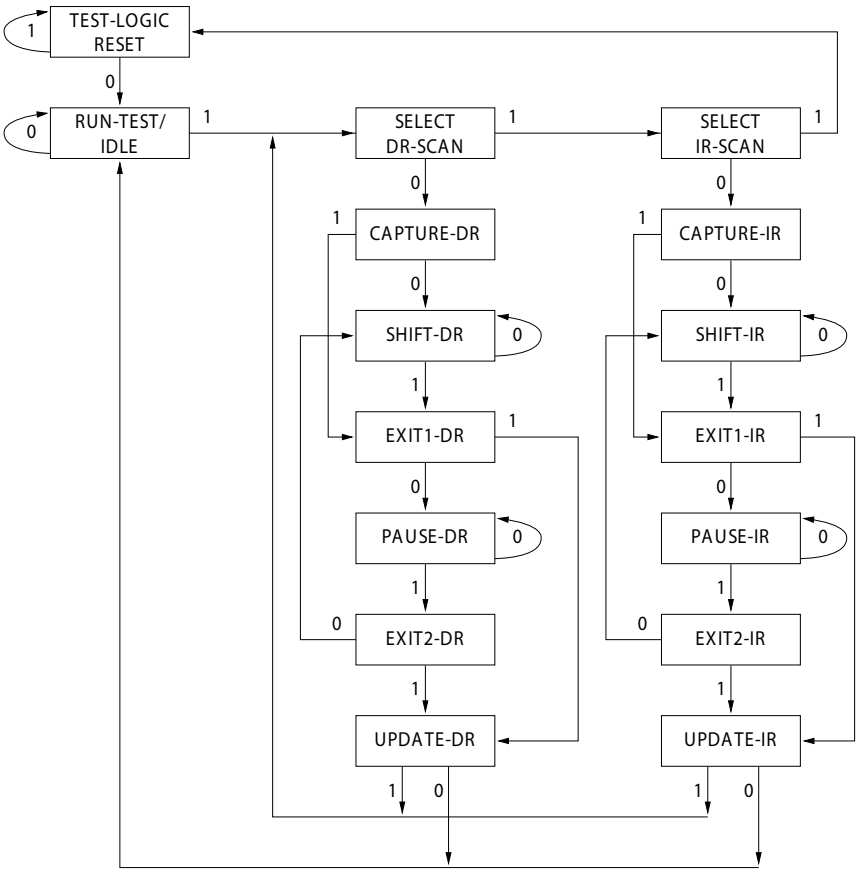
This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the "Shift-DR" state. During "Update-DR," the value loaded into that shift-register cell will latch into the preload register. When the EXTEST instruction is entered, this bit will directly control the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered-up, and also when the TAP controller is in the "Test-Logic-Reset" state.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

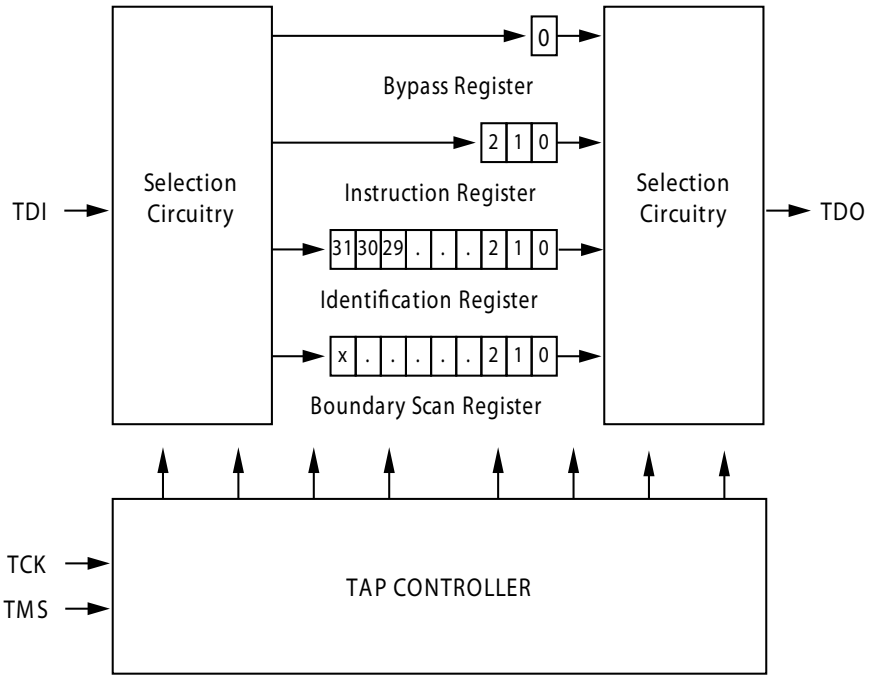
Downloaded from Arrow.com.

TAP Controller State Diagram

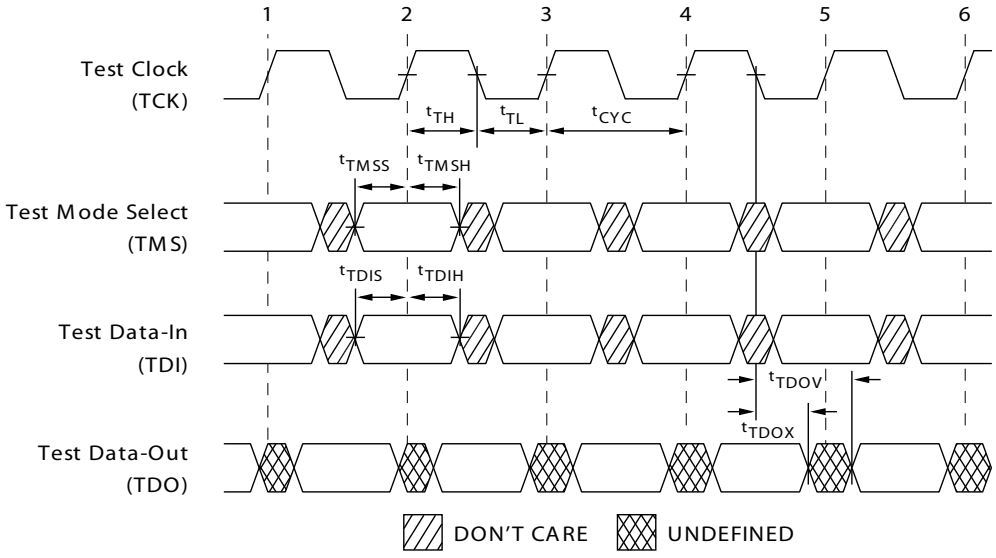


Downloaded from Arrow.com.

TAP Controller Block Diagram



TAP Timing



Downloaded from Arrow.com.

TAP AC Switching Characteristics

Over the Operating Range

Parameter [12, 13]	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50	–	ns
t_{TF}	TCK Clock Frequency	–	20	MHz
t_{TH}	TCK Clock HIGH time	20	–	ns
t_{TL}	TCK Clock LOW time	20	–	ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid	–	10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0	–	ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5	–	ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5	–	ns
t_{CS}	Capture Setup to TCK Rise	5	–	ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5	–	ns
t_{TDIH}	TDI Hold after Clock Rise	5	–	ns
t_{CH}	Capture Hold after Clock Rise	5	–	ns

Notes
12. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
13. Test conditions are specified using the load in TAP AC test Conditions. t_R/t_F = 1 ns.

Downloaded from Arrow.com.

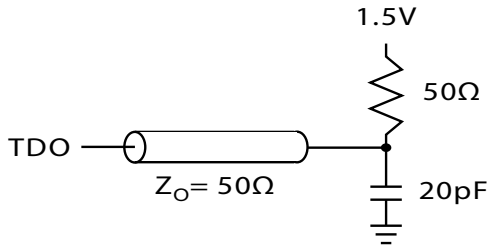
3.3 V TAP AC Test Conditions

Input pulse levels ..... V_{SS} to 3.3 V
Input rise and fall times (Slew Rate) ..... 2 V/ns
Input timing reference levels ..... 1.5 V
Output reference levels ..... 1.5 V
Test load termination supply voltage ..... 1.5 V

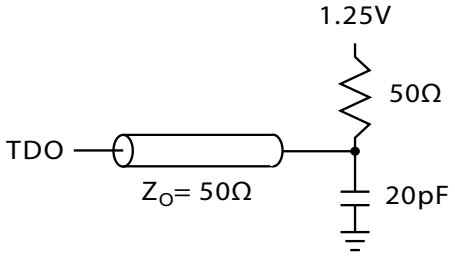
2.5 V TAP AC Test Conditions

Input pulse levels ..... V_{SS} to 2.5 V
Input rise and fall time (Slew Rate) ..... 2 V/ns
Input timing reference levels ..... 1.25 V
Output reference levels ..... 1.25 V
Test load termination supply voltage ..... 1.25 V

3.3 V TAP AC Output Load Equivalent



2.5 V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics and Operating Conditions

(0 °C < T_A < +70 °C; V_{DD} = 3.3 V ± 0.165 V unless otherwise noted)

Parameter [14]	Description	Test Conditions		Min	Max	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –4.0 mA, V_{DDQ} = 3.3 V		2.4	–	V
		I_{OH} = –1.0 mA, V_{DDQ} = 2.5 V		2.0	–	V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	V_{DDQ} = 3.3 V	2.9	–	V
			V_{DDQ} = 2.5 V	2.1	–	V
V_{OL1}	Output LOW Voltage	I_{OL} = 8.0 mA, V_{DDQ} = 3.3 V		–	0.4	V
		I_{OL} = 8.0 mA, V_{DDQ} = 2.5 V		–	0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	V_{DDQ} = 3.3 V	–	0.2	V
			V_{DDQ} = 2.5 V	–	0.2	V
V_{IH}	Input HIGH Voltage	V_{DDQ} = 3.3 V		2.0	V_{DD} + 0.3	V
		V_{DDQ} = 2.5 V		1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	V_{DDQ} = 3.3 V		–0.5	0.7	V
		V_{DDQ} = 2.5 V		–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA

Note
14. All voltages referenced to V_{SS} (GND)

Downloaded from Arrow.com.

Identification Register Definitions

Instruction Field	CY7C1370KV33	Description
Revision Number (31:29)	000	Reserved for version number.
Cypress Device ID (28:12) [15]	01011001000010101	Reserved for future use.
Cypress JEDEC ID (11:1)	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	Indicate the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size (× 36)
Instruction	3
Bypass	1
ID	32
Boundary Scan Order (165-ball FBGA package)	89

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High Z state.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Note
15. Bit #24 is “1” in the Register Definitions for both 2.5 V and 3.3 V versions of this device.

Downloaded from Arrow.com.

Boundary Scan Order

165-ball FBGA [16, 17]

Bit #	Ball ID	Bit #	Ball ID	Bit #	Ball ID
1	N6	31	D10	61	G1
2	N7	32	C11	62	D2
3	N10	33	A11	63	E2
4	P11	34	B11	64	F2
5	P8	35	A10	65	G2
6	R8	36	B10	66	H1
7	R9	37	A9	67	H3
8	P9	38	B9	68	J1
9	P10	39	C10	69	K1
10	R10	40	A8	70	L1
11	R11	41	B8	71	M1
12	H11	42	A7	72	J2
13	N11	43	B7	73	K2
14	M11	44	B6	74	L2
15	L11	45	A6	75	M2
16	K11	46	B5	76	N1
17	J11	47	A5	77	N2
18	M10	48	A4	78	P1
19	L10	49	B4	79	R1
20	K10	50	B3	80	R2
21	J10	51	A3	81	P3
22	H9	52	A2	82	R3
23	H10	53	B2	83	P2
24	G11	54	C2	84	R4
25	F11	55	B1	85	P4
26	E11	56	A1	86	N5
27	D11	57	C1	87	P6
28	G10	58	D1	88	R6
29	F10	59	E1	89	Internal
30	E10	60	F1		

Notes
16. Balls which are NC (No Connect) are pre-set LOW.
17. Bit# 89 is preset HIGH.

Downloaded from Arrow.com.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.5 V to +4.6 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.5 V to +V_{DD}

DC to Outputs in Tristate .....–0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage .....–0.5 V to V_{DD} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) .....> 2001V

Latch up Current .....> 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / +10%	2.5 V – 5% to V_{DD}
Industrial	–40 °C to +85 °C		

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU (Device without ECC)	Logical Single-Bit Upsets	25 °C	<5	5	FIT/Mb
LSBU (Device with ECC)			0	0.01	FIT/Mb
LMBU	Logical Multi-Bit Upsets	25 °C	0	0.01	FIT/Mb
SEL	Single Event Latch up	85 °C	0	0.1	FIT/Dev

** No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to Application Note AN54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates".

Electrical Characteristics

Over the Operating Range

Parameter [18, 19]	Description	Test Conditions	Min	Max	Unit
V_{DD}	Power Supply Voltage		3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	for 3.3 V I/O	3.135	V_{DD}	V
		for 2.5 V I/O	2.375	2.625	V
V_{OH}	Output HIGH Voltage	for 3.3 V I/O, I_{OH} = –4.0 mA	2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA	2.0	–	V
V_{OL}	Output LOW Voltage	for 3.3 V I/O, I_{OL} = 8.0 mA	–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA	–	0.4	V
V_{IH}	Input HIGH Voltage [18]	for 3.3 V I/O	2.0	V_{DD} + 0.3	V
		for 2.5 V I/O	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage [18]	for 3.3 V I/O	–0.3	0.8	V
		for 2.5 V I/O	–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}	–5	5	µA
	Input Current of MODE	Input = V_{SS}	–30	–	
		Input = V_{DD}	–	5	
	Input Current of ZZ	Input = V_{SS}	–5	–	
		Input = V_{DD}	–	30	

Notes

18. Overshoot: $V_{IH(AC)}$ < V_{DD} + 1.5 V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL(AC)}$ > –2 V (Pulse width less than $t_{CYC}/2$).
19. $T_{Power\text{-}up}$: Assumes a linear ramp from 0 V to $V_{DD(min.)}$ of at least 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Downloaded from Arrow.com.

Electrical Characteristics (continued)

Over the Operating Range

Parameter [18, 19]	Description	Test Conditions			Min	Max	Unit
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled			–5	5	µA
I_{DD}	V_{DD} Operating Supply	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	4-ns cycle, 250 MHz	× 18	–	180	mA
				× 36	–	200	
			5-ns cycle, 200 MHz	× 18	–	158	
				× 36	–	178	
			6-ns cycle, 167 MHz	× 18	–	143	
				× 36	–	163	
I_{SB1}	Automatic CE Power-down Current – TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX} = $1/t_{CYC}$	4-ns cycle, 250 MHz	× 18	–	75	mA
				× 36	–	80	
			5-ns cycle, 200 MHz	× 18	–	75	
				× 36	–	80	
			6-ns cycle, 167 MHz	× 18	–	75	
				× 36	–	80	
I_{SB2}	Automatic CE Power-down Current – CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≤ 0.3 V or V_{IN} ≥ V_{DDQ} – 0.3 V, f = 0	All speed grades	× 18	–	65	mA
				× 36	–	70	
I_{SB3}	Automatic CE Power-down Current – CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≤ 0.3 V or V_{IN} ≥ V_{DDQ} – 0.3 V, f = f_{MAX} = $1/t_{CYC}$	4-ns cycle, 250 MHz	× 18	–	75	mA
				× 36	–	80	
			5-ns cycle, 200 MHz	× 18	–	75	
				× 36	–	80	
			6-ns cycle, 167 MHz	× 18	–	75	
				× 36	–	80	
I_{SB4}	Automatic CE Power-down Current – TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0	All speed grades	× 18	–	65	mA
				× 36	–	70	

Downloaded from Arrow.com.

Capacitance

Parameter	Description	Test Conditions	100-pin TQFP Max	165-ball FBGA Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	5	5	pF
C_{CLK}	Clock input capacitance		5	5	pF
$C_{I/O}$	Input/Output capacitance		5	5	pF

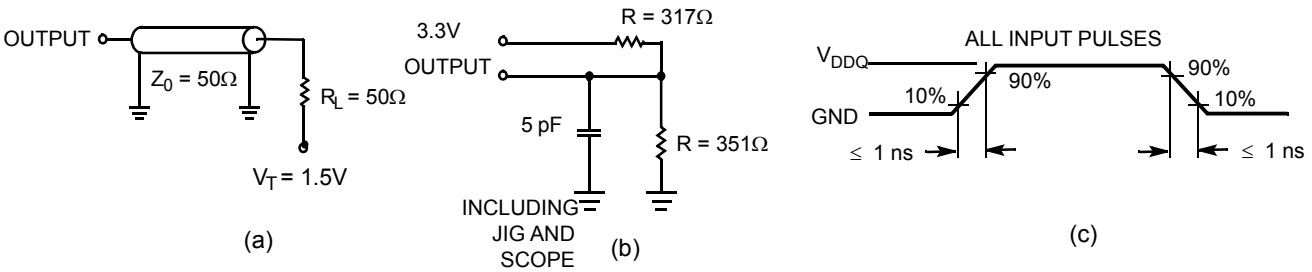
Thermal Resistance

Parameter	Description	Test Conditions		100-pin TQFP Package	165-ball FBGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	With Still Air (0 m/s)	37.95	17.34	°C/W
			With Air Flow (1 m/s)	33.19	14.33	°C/W
			With Air Flow (3 m/s)	30.44	12.63	°C/W
Θ_{JB}	Thermal resistance (junction to board)		--	24.07	8.95	°C/W
Θ_{JC}	Thermal resistance (junction to case)			8.36	3.50	°C/W

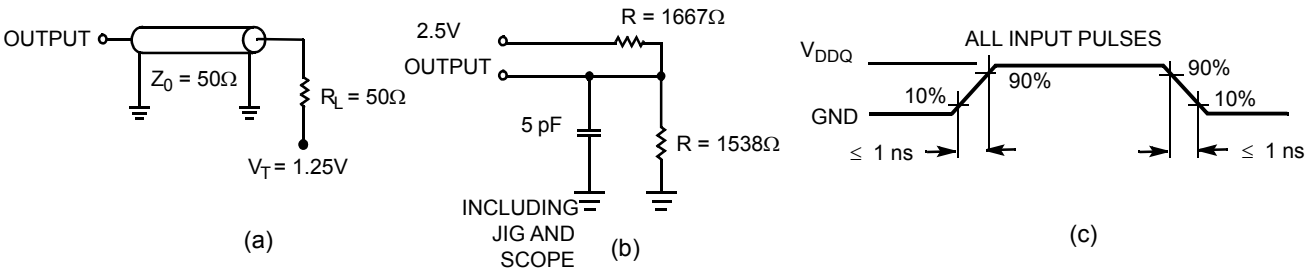
AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms

3.3V I/O Test Load



2.5V I/O Test Load



Downloaded from Arrow.com.

Switching Characteristics

Over the Operating Range

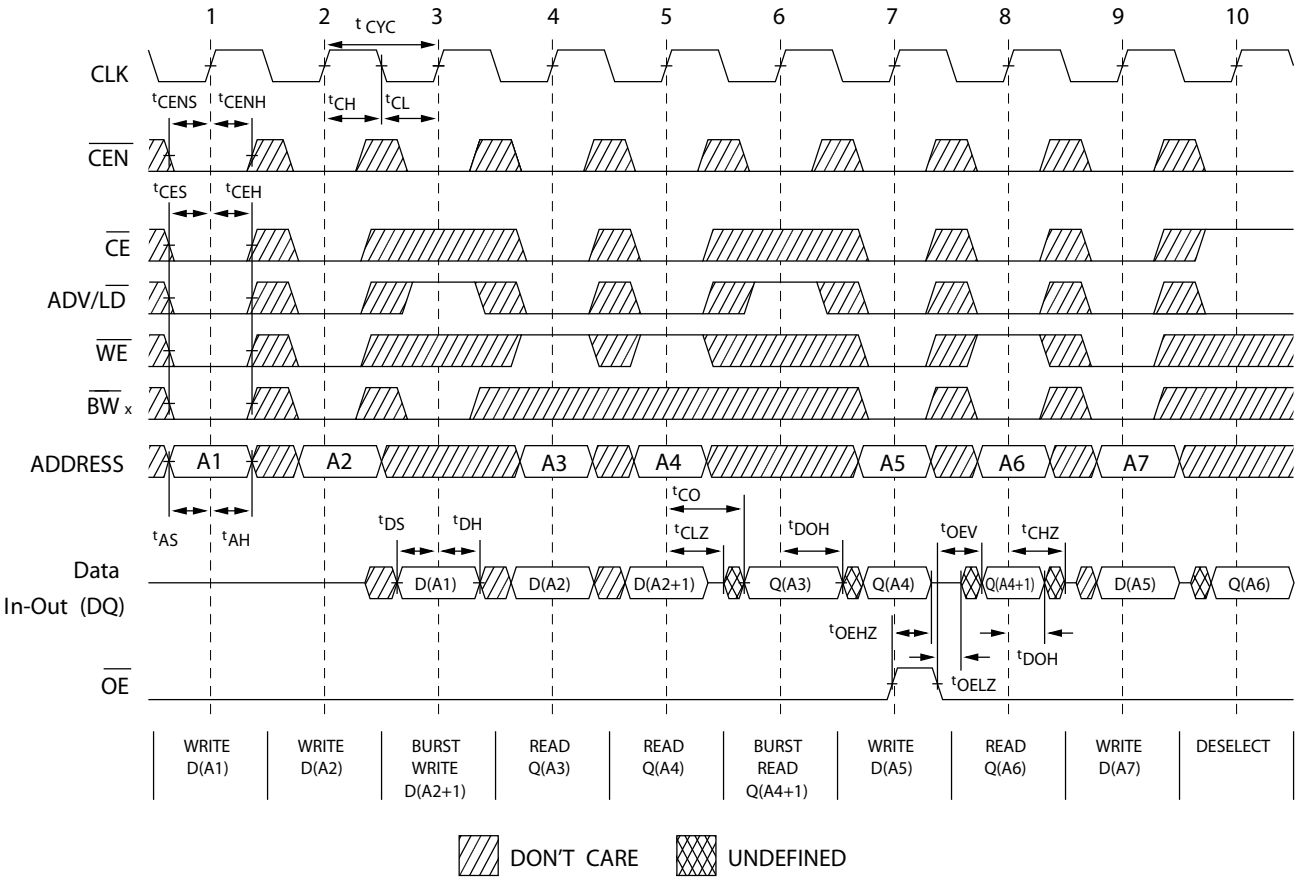
Parameter [20, 21]	Description	-250		-200		-167		Unit
		Min	Max	Min	Max	Min	Max	
t_{Power} [22]	V_{CC}(typical) to the first access read or write	1	–	1	–	1	–	ms
Clock								
t_{CYC}	Clock cycle time	4.0	–	5.0	–	6.0	–	ns
F_{MAX}	Maximum operating frequency	–	250	–	200	–	167	MHz
t_{CH}	Clock HIGH	1.5	–	2.0	–	2.2	–	ns
t_{CL}	Clock LOW	1.5	–	2.0	–	2.2	–	ns
Output Times								
t_{CO}	Data output valid after CLK rise	–	2.5	–	3.0	–	3.4	ns
t_{EOV}	$\overline{OE}$ LOW to output valid	–	2.6	–	3.0	–	3.4	ns
t_{DOH}	Data output hold after CLK rise	1.0	–	1.5	–	1.5	–	ns
t_{CHZ}	Clock to high Z [23, 24, 25]	–	2.6	–	3.0	–	3.4	ns
t_{CLZ}	Clock to low Z [23, 24, 25]	1.0	–	1.3	–	1.5	–	ns
t_{EOHZ}	$\overline{OE}$ HIGH to output high Z [23, 24, 25]	–	2.6	–	3.0	–	3.4	ns
t_{EOLZ}	$\overline{OE}$ LOW to output low Z [23, 24, 25]	0	–	0	–	0	–	ns
Setup Times								
t_{AS}	Address setup before CLK rise	1.2	–	1.4	–	1.5	–	ns
t_{DS}	Data input setup before CLK rise	1.2	–	1.4	–	1.5	–	ns
t_{CENS}	$\overline{CEN}$ setup before CLK rise	1.2	–	1.4	–	1.5	–	ns
t_{WES}	$\overline{WE}$, $\overline{BW}_X$ setup before CLK rise	1.2	–	1.4	–	1.5	–	ns
t_{ALS}	ADV/$\overline{LD}$ setup before CLK rise	1.2	–	1.4	–	1.5	–	ns
t_{CES}	Chip select setup	1.2	–	1.4	–	1.5	–	ns
Hold Times								
t_{AH}	Address hold after CLK rise	0.3	–	0.4	–	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.3	–	0.4	–	0.5	–	ns
t_{CENH}	$\overline{CEN}$ hold after CLK rise	0.3	–	0.4	–	0.5	–	ns
t_{WEH}	$\overline{WE}$, $\overline{BW}_X$ hold after CLK rise	0.3	–	0.4	–	0.5	–	ns
t_{ALH}	ADV/$\overline{LD}$ hold after CLK rise	0.3	–	0.4	–	0.5	–	ns
t_{CEH}	Chip select hold after CLK rise	0.3	–	0.4	–	0.5	–	ns

Notes
20. Timing reference is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
21. Test conditions shown in (a) of Figure 3 on page 23 unless otherwise noted.
22. This part has a voltage regulator internally; t_{Power} is the time power needs to be supplied above V_{DD} minimum initially, before a Read or Write operation can be initiated.
23. t_{CHZ}, t_{CLZ}, t_{EOLZ}, and t_{EOHZ} are specified with AC test conditions shown in (b) of Figure 3 on page 23. Transition is measured ±200 mV from steady-state voltage.
24. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z prior to Low Z under the same system conditions.
25. This parameter is sampled and not 100% tested.

Downloaded from Arrow.com.

Switching Waveforms

Figure 4. Read/Write/Timing [26, 27, 28]



Notes
26. For this waveform ZZ is tied LOW.
27. When $\overline{CE}$ is LOW, $\overline{CE_1}$ is LOW, CE_2 is HIGH and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH,$\overline{CE_1}$ is HIGH or CE_2 is LOW or $\overline{CE_3}$ is HIGH.
28. Order of the Burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved).Burst operations are optional.

Downloaded from Arrow.com.

Switching Waveforms (continued)

Figure 5. NOP, STALL, and DESELECT Cycles [29, 30, 31]

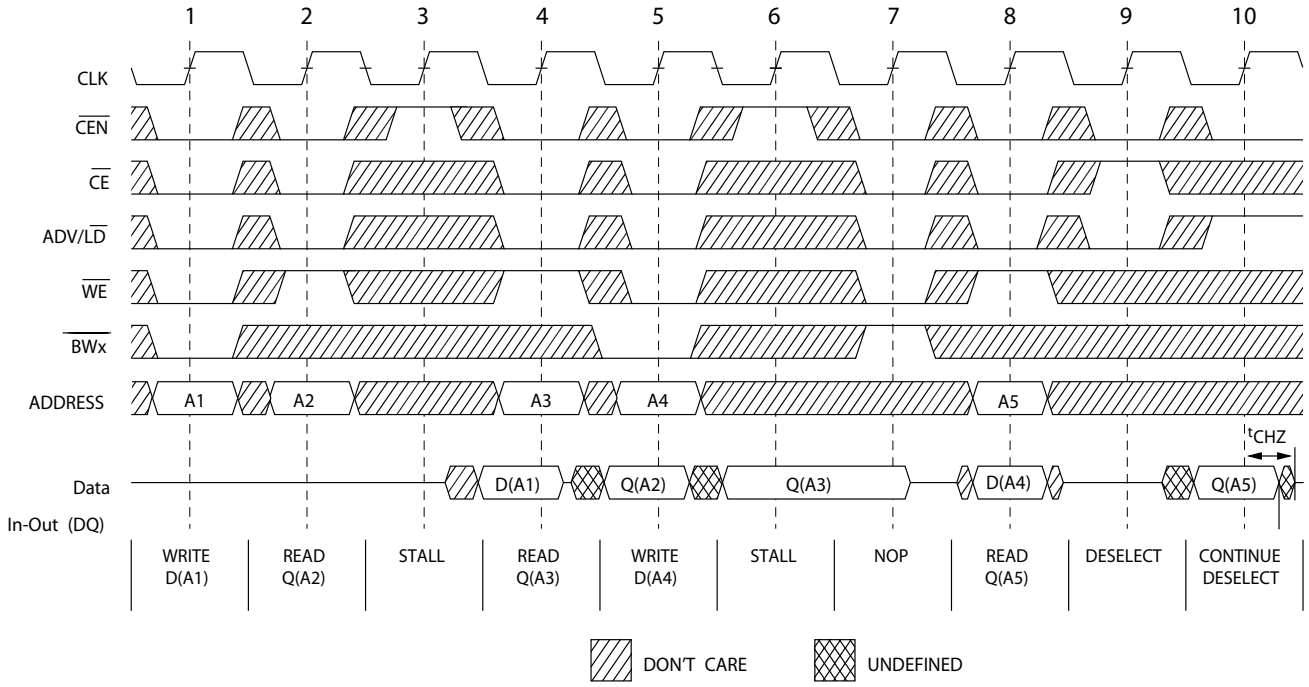
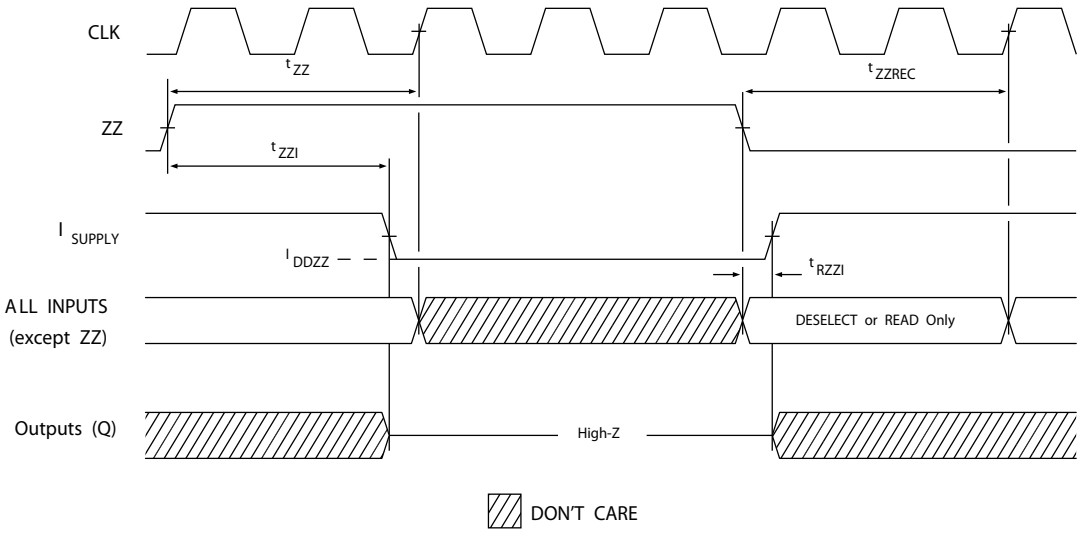


Figure 6. ZZ Mode Timing [32, 33]



Notes
29. For this waveform ZZ is tied LOW.
30. When $\overline{CE}$ is LOW, $\overline{CE_1}$ is LOW, CE_2 is HIGH and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH,$\overline{CE_1}$ is HIGH or CE_2 is LOW or $\overline{CE_3}$ is HIGH.
31. The Ignore Clock Edge or Stall cycle (Clock 3) illustrated $\overline{CEN}$ being used to create a pause. A write is not performed during this cycle.
32. Device must be deselected when entering ZZ mode. See cycle description table for all possible signal conditions to deselect the device.
33. I/Os are in High Z when exiting ZZ sleep mode.

Downloaded from Arrow.com.

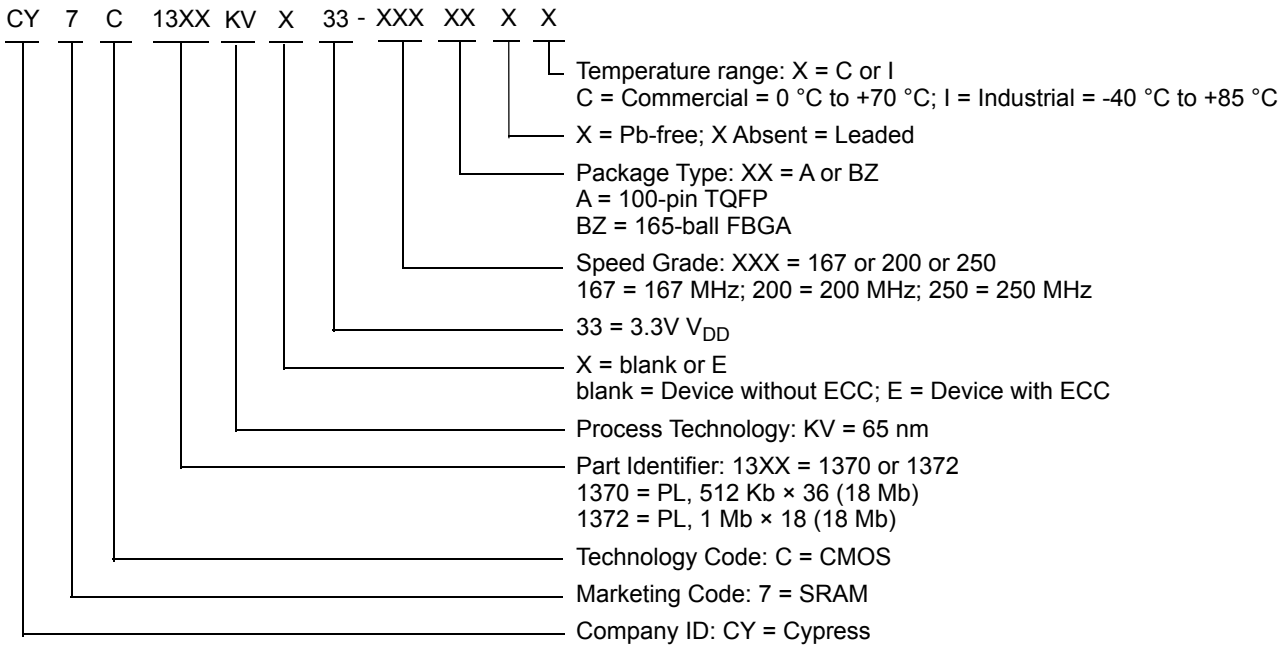
Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available.
For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
167	CY7C1370KV33-167AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1372KV33-167AXC			
	CY7C1370KV33-167BZXC	51-85180	165-ball FBGA (13 × 15 × 1.4 mm) Pb-free	
	CY7C1370KV33-167AXI	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Industrial
	CY7C1370KVE33-167AXI			
	CY7C1372KV33-167AXI			
	CY7C1372KVE33-167AXI			
200	CY7C1370KV33-200AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1372KV33-200AXC			
	CY7C1370KV33-200AXI	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Industrial
	CY7C1370KV33-200BZXI	51-85180	165-ball FBGA (13 × 15 × 1.4 mm) Pb-free	
250	CY7C1370KV33-250AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial

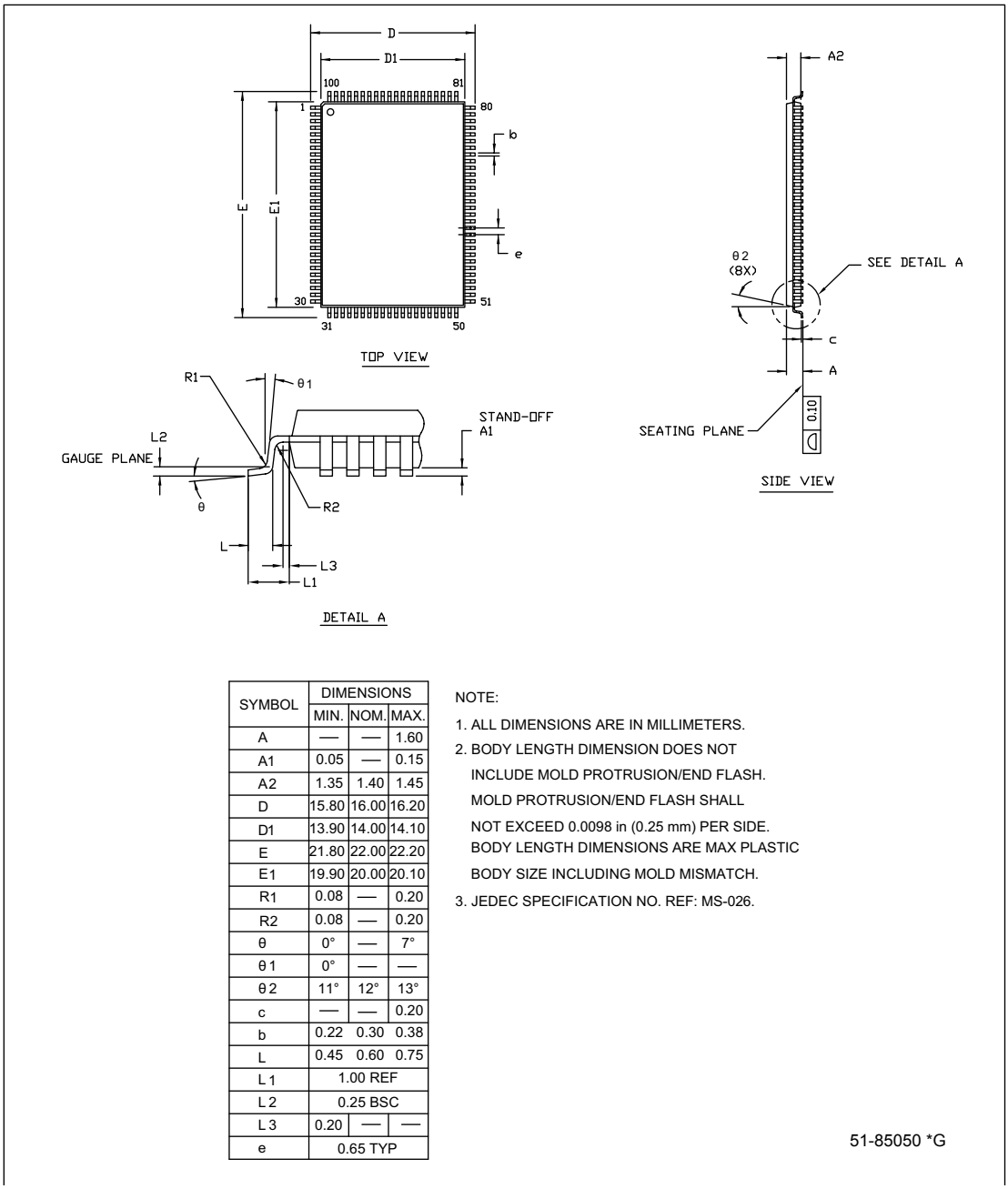
Ordering Code Definitions



Downloaded from Arrow.com.

Package Diagrams

Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
R1	0.08	—	0.20
R2	0.08	—	0.20
θ	0°	—	7°
θ1	0°	—	—
θ2	11°	12°	13°
c	—	—	0.20
b	0.22	0.30	0.38
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
L3	0.20	—	—
e	0.65 TYP		

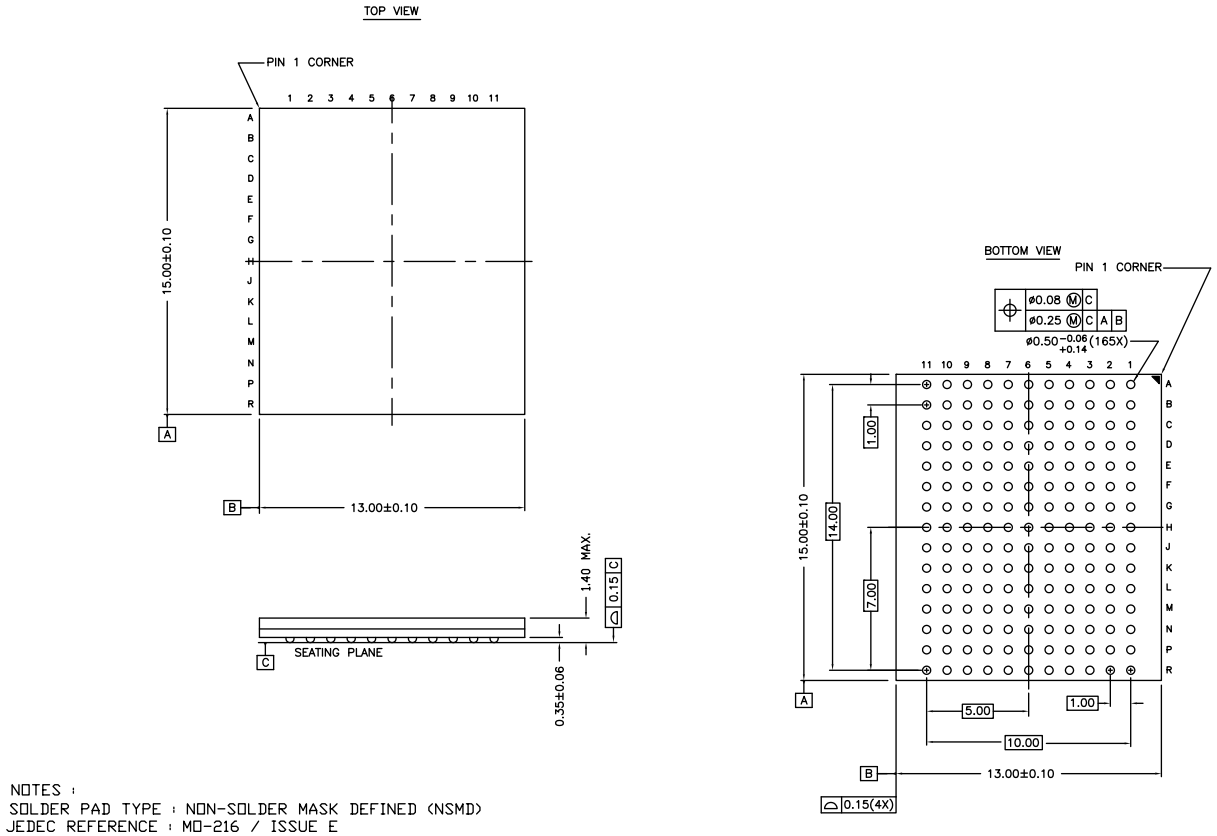
NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE. BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
3. JEDEC SPECIFICATION NO. REF: MS-026.

51-85050 *G

Downloaded from Arrow.com.

Package Diagrams (continued)

Figure 8. 165-ball FBGA (13 × 15 × 1.4 mm) BB165D/BW165D (0.5 Ball Diameter) Package Outline, 51-85180



NOTES :
SOLDER PAD TYPE : NON-SOLDER MASK DEFINED (NSMD)
JEDEC REFERENCE : MO-216 / ISSUE E
PACKAGE CODE : BB0AC/BW0AC
PACKAGE WEIGHT : SEE CYPRESS PACKAGE MATERIAL DECLARATION DATASHEET (PMDD) POSTED ON THE CYPRESS WEB.

51-85180 *G

Downloaded from Arrow.com.

Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
$\overline{CEN}$	Clock Enable
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
JTAG	Joint Test Action Group
LMBU	Logical Multi-Bit Upsets
LSB	Least Significant Bit
LSBU	Logical Single-Bit Upsets
MSB	Most Significant Bit
NoBL	No Bus Latency
$\overline{OE}$	Output Enable
SEL	Single Event Latch-up
SRAM	Static Random Access Memory
TAP	Test Access Port
TCK	Test Clock
TMS	Test Mode Select
TDI	Test Data-In
TDO	Test Data-Out
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mV	millivolt
mm	millimeter
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

Downloaded from Arrow.com.

Document History Page

Document Title: CY7C1370KV33/CY7C1370KVE33/CY7C1372KV33/CY7C1372KVE33, 18-Mbit (512K × 36/1M × 18) Pipelined SRAM with NoBL™ Architecture (With ECC) Document Number: 001-97836				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*F	5083798	DEVM	01/14/2016	Changed status from Preliminary to Final.
*G	5396610	PRIT	08/09/2016	Updated Neutron Soft Error Immunity: Updated values in “Typ” and “Max” columns corresponding to “LSBU (Device without ECC)” parameter. Updated Ordering Information: Updated part numbers. Updated to new template.
*H	5734193	PRIT	05/12/2017	Updated Package Diagrams Changed Spec 51-85050 from *E to *G. Updated Cypress Logo and Copyright.

Downloaded from Arrow.com.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC®Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IoT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2015-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Downloaded from Arrow.com.