

# 16-Mbit (1M words × 16-bit) Static RAM with Error-Correcting Code (ECC)

## Features

- High speed
  - $t_{AA} = 10 \text{ ns}/15 \text{ ns}$
- Embedded error-correcting code (ECC) for single-bit error correction<sup>[1, 2]</sup>
- Low active and standby currents
  - $I_{CC} = 90 \text{ mA}$  typical at 100 MHz
  - $I_{SB2} = 20 \text{ mA}$  typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0 V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Available in Pb-free 48-pin TSOP I, 54-pin TSOP II, and 48-ball VFBGA packages

## Functional Description

CY7C1061G and CY7C1061GE are high-performance CMOS fast static RAM devices with embedded ECC<sup>[1]</sup>. Both devices are offered in single and dual chip enable options and in multiple pin configurations. The CY7C1061GE device includes an ERR pin that signals a single-bit error-detection and correction event during a read cycle.

To access devices with a single chip enable input, assert the chip enable (CE) input LOW. To access dual chip enable devices, assert both chip enable inputs – CE<sub>1</sub> as LOW and CE<sub>2</sub> as HIGH.

To perform data writes, assert the Write Enable (WE) input LOW, and provide the data and address on the device data pins (I/O<sub>0</sub> through I/O<sub>15</sub>) and address pins (A<sub>0</sub> through A<sub>19</sub>) respectively. The Byte High Enable (BHE) and Byte Low Enable (BLE) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified. BHE controls I/O<sub>8</sub> through I/O<sub>15</sub> and BLE controls I/O<sub>0</sub> through I/O<sub>7</sub>.

To perform data reads, assert the Output Enable (OE) input and provide the required address on the address lines. Read data is accessible on I/O lines (I/O<sub>0</sub> through I/O<sub>15</sub>). You can perform byte accesses by asserting the required byte enable signal (BHE or BLE) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when the device is deselected (CE HIGH for a single chip enable device and CE<sub>1</sub> HIGH / CE<sub>2</sub> LOW for a dual chip enable device), or control signals are de-asserted (OE, BLE, BHE).

On the CY7C1061GE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = High). See the [Truth Table on page 16](#) for a complete description of read and write modes.

The logic block diagrams are on page 2.

The CY7C1061G and CY7C1061GE devices are available in 48-pin TSOP I, 54-pin TSOP II, and 48-ball VFBGA packages.

For a complete list of related documentation, click [here](#).

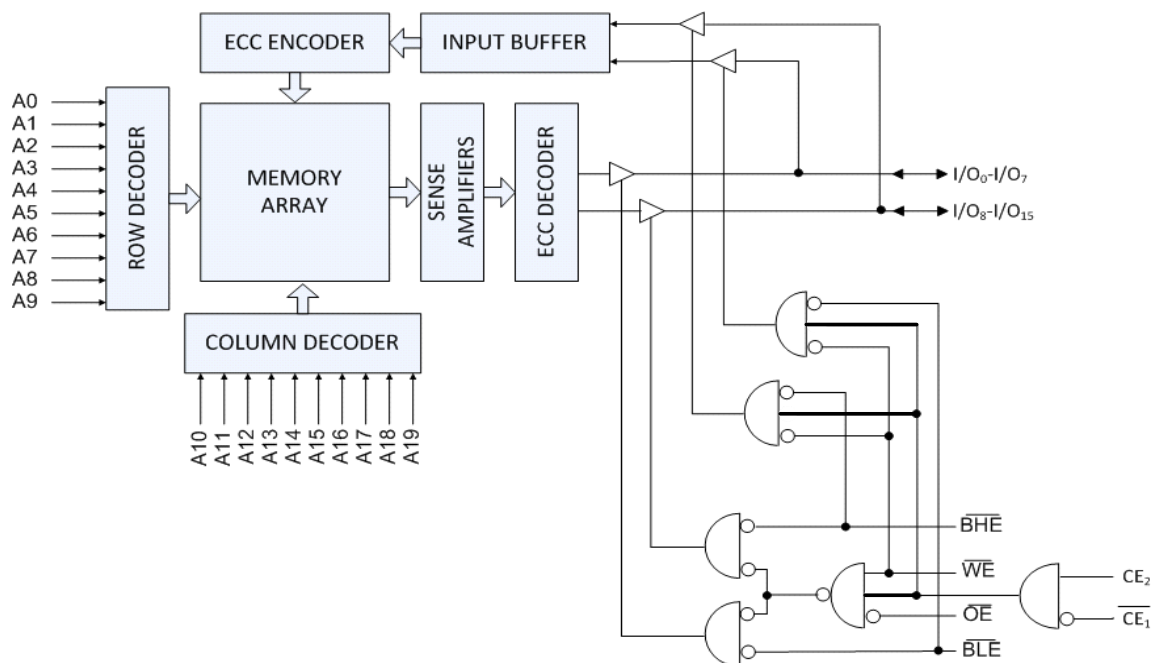
## Product Portfolio

Product	Features and Options (see <a href="#">Pin Configurations on page 4</a> )	Range	V <sub>CC</sub> Range (V)	Speed (ns) 10/15	Current Consumption			
					Operating I <sub>CC</sub> , (mA)		Standby, I <sub>SB2</sub> (mA)	
					f = f <sub>max</sub>			
					Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max
CY7C1061G18	Single or dual chip enables	Industrial	1.65 V–2.2 V	15	70	80	20	30
CY7C1061G(E)30	Optional ERR pins		2.2 V–3.6 V	10	90	110		
CY7C1061G			4.5 V–5.5 V	10	90	110		
	Address MSB A <sub>19</sub> pin placement options compatible with Cypress and other vendors							

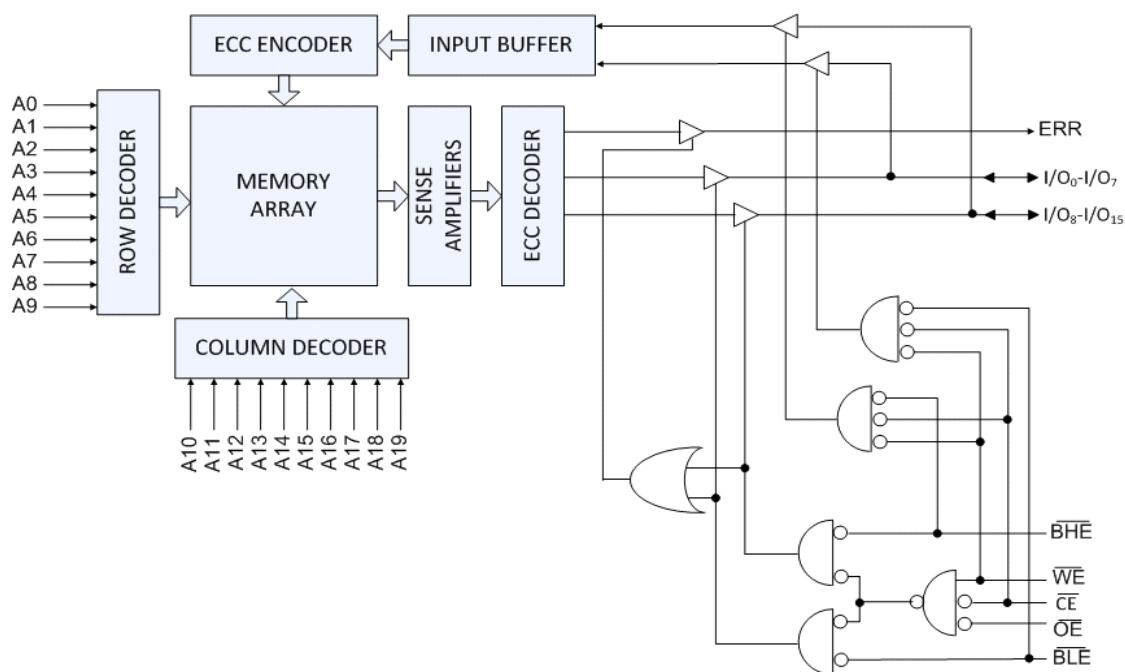
### Notes

- This device does not support automatic write-back on error detection.
- SER FIT Rate <0.1 FIT/Mb. Refer [AN88889](#) for details.
- Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 1.8 V (for a V<sub>CC</sub> range of 1.65 V–2.2 V), V<sub>CC</sub> = 3 V (for a V<sub>CC</sub> range of 2.2 V–3.6 V), and V<sub>CC</sub> = 5 V (for a V<sub>CC</sub> range of 4.5 V–5.5 V), T<sub>A</sub> = 25 °C.

## Logic Block Diagram – CY7C1061G



## Logic Block Diagram – CY7C1061GE

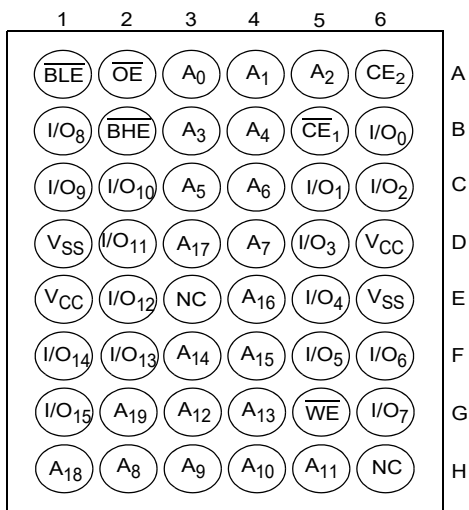


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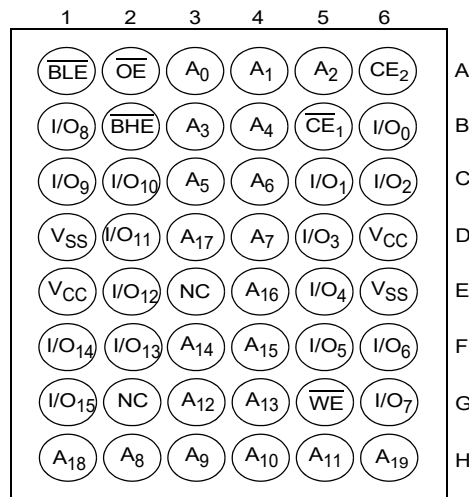
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## Pin Configurations

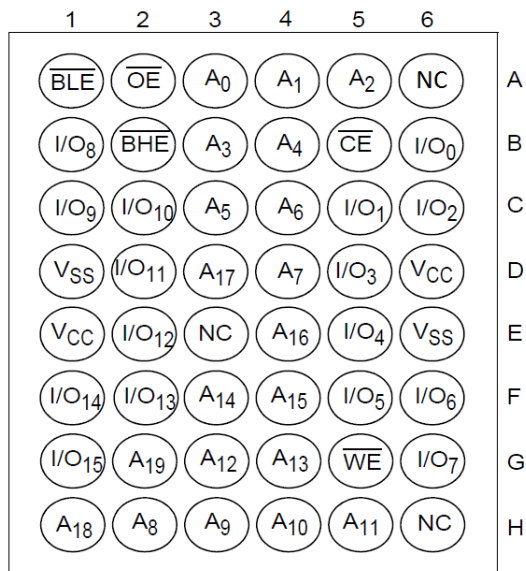
**Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Dual Chip Enable without ERR, Address MSB A19 at Ball G2, CY7C1061G<sup>[4]</sup> Package/Grade ID: BVJXI**



**Figure 2. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Dual Chip Enable without ERR, Address MSB A19 at Ball H6, CY7C1061G<sup>[4]</sup> Package/Grade ID: BVXI**



**Figure 3. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Single Chip Enable without ERR, Address MSB A19 at Ball G2, CY7C1061G<sup>[4]</sup> Package/Grade ID: BV1XI**

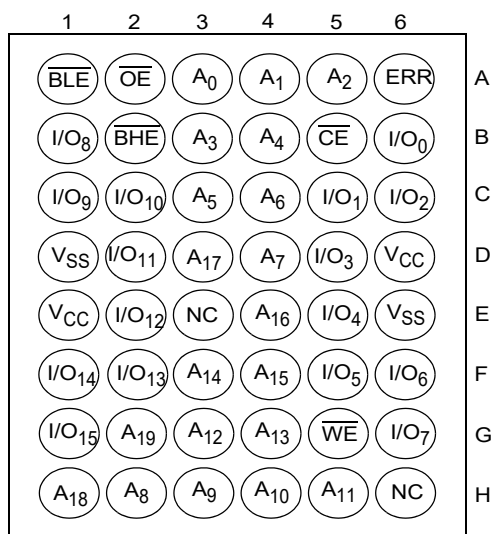


### Note

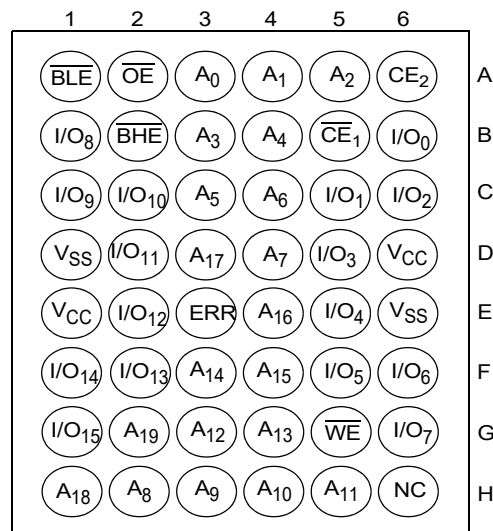
4. NC pins are not connected internally to the die.

## Pin Configurations (continued)

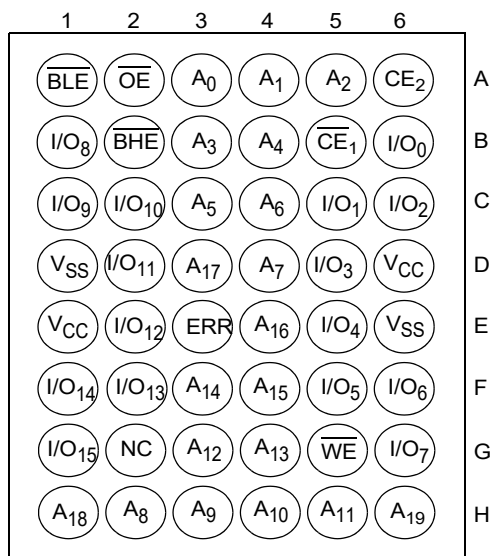
**Figure 4. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Single Chip Enable with ERR, Address MSB A19 at Ball G2, CY7C1061GE<sup>[5, 6]</sup> Package/Grade ID: BV1XI**



**Figure 5. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Dual Chip Enable with ERR, Address MSB A19 at Ball G2, CY7C1061GE<sup>[5, 6]</sup> Package/Grade ID: BVJXI**



**Figure 6. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Dual Chip Enable with ERR, Address MSB A19 at Ball H6, CY7C1061GE<sup>[5, 6]</sup> Package/Grade ID: BVXI**

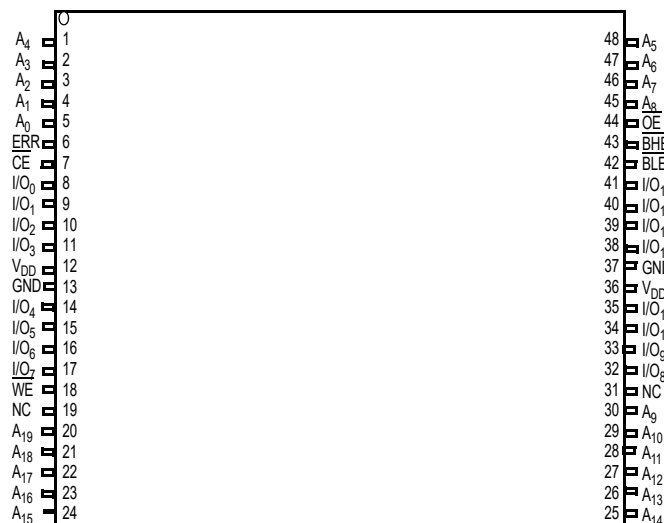


### Notes

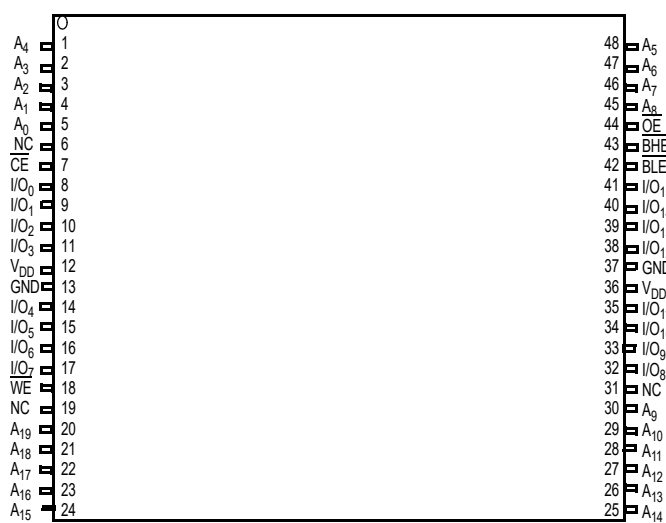
5. NC pins are not connected internally to the die.
6. ERR is an Output pin. If not used, this pin should be left floating.

## Pin Configurations (continued)

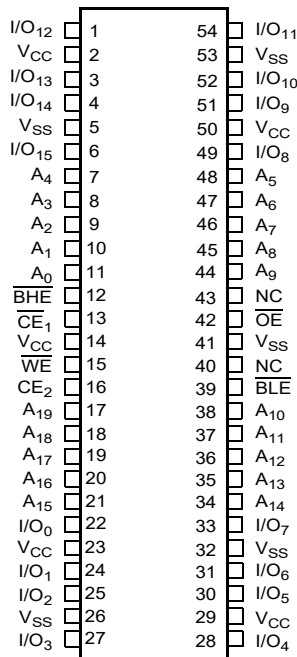
**Figure 7. 48-pin TSOP I (12 × 18.4 × 1 mm) Pinout, Single Chip Enable with ERR, CY7C1061GE<sup>[7, 8]</sup>**  
 Package/Grade ID: ZXI



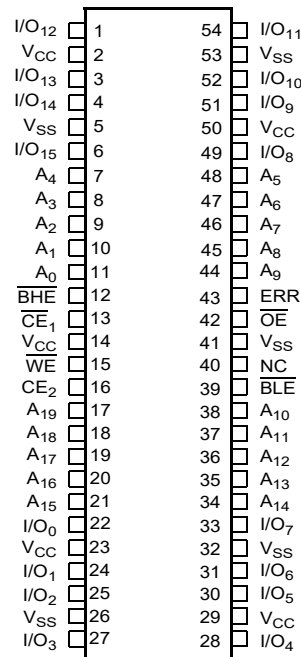
**Figure 8. 48-pin TSOP I (12 × 18.4 × 1 mm) Pinout, Single Chip Enable without ERR, CY7C1061G<sup>[7]</sup>**  
 Package/Grade ID: ZXI



**Figure 9. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) pinout, Dual Chip Enable without ERR, CY7C1061G<sup>[7]</sup>**  
 Package/Grade ID: ZSXI



**Figure 10. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) pinout, Dual Chip Enable with ERR, CY7C1061GE<sup>[7, 8]</sup>**  
 Package/Grade ID: ZSXI



### Notes

7. NC pins are not connected internally to the die.
8. ERR is an Output pin. If not used, this pin should be left floating.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature  
with power applied ..... -55 °C to +125 °C

Supply voltage  
on  $V_{CC}$  relative to GND ..... -0.5 V to  $V_{CC} + 0.5$  V

DC voltage applied to outputs  
in High Z State <sup>[9]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage<sup>[9]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage  
(MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

## Operating Range

Grade	Ambient Temperature	$V_{CC}$
Industrial	-40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

## DC Electrical Characteristics

Over the operating range of -40 °C to 85 °C

Parameter	Description	Test Conditions	10 ns / 15 ns			Unit
			Min	Typ <sup>[10]</sup>	Max	
$V_{OH}$	Output HIGH voltage	1.65 V to 2.2 V $V_{CC} = \text{Min}, I_{OH} = -0.1$ mA	1.4	—	—	V
		2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OH} = -1.0$ mA	2.0	—	—	
		2.7 V to 3.0 V $V_{CC} = \text{Min}, I_{OH} = -4.0$ mA	2.2	—	—	
		3.0 V to 3.6 V $V_{CC} = \text{Min}, I_{OH} = -4.0$ mA	2.4	—	—	
		4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OH} = -4.0$ mA	2.4	—	—	
		4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OH} = -0.1$ mA	$V_{CC} - 0.4$ <sup>[11]</sup>	—	—	
$V_{OL}$	Output LOW voltage	1.65 V to 2.2 V $V_{CC} = \text{Min}, I_{OL} = 0.1$ mA	—	—	0.2	V
		2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OL} = 2$ mA	—	—	0.4	
		2.7 V to 3.6 V $V_{CC} = \text{Min}, I_{OL} = 8$ mA	—	—	0.4	
		4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OL} = 8$ mA	—	—	0.4	
$V_{IH}$ <sup>[9]</sup>	Input HIGH voltage	1.65 V to 2.2 V	1.4	—	$V_{CC} + 0.2$	V
		2.2 V to 2.7 V	2.0	—	$V_{CC} + 0.3$	
		2.7 V to 3.6 V	2.0	—	$V_{CC} + 0.3$	
		4.5 V to 5.5 V	2.0	—	$V_{CC} + 0.5$	
$V_{IL}$ <sup>[9]</sup>	Input LOW voltage	1.65 V to 2.2 V	-0.2	—	0.4	V
		2.2 V to 2.7 V	-0.3	—	0.6	
		2.7 V to 3.6 V	-0.3	—	0.8	
		4.5 V to 5.5 V	-0.5	—	0.8	
$I_{IX}$	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	-1.0	—	+1.0	μA
$I_{OZ}$	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$ , Output disabled	-1.0	—	+1.0	μA
$I_{CC}$	Operating supply current	$V_{CC} = \text{Max}, I_{OUT} = 0$ mA, CMOS levels	—	90.0	110.0	mA
		$f = 100$ MHz	—	70.0	80.0	
$I_{SB1}$	Automatic CE power down current – TTL inputs	$\text{Max } V_{CC}, \overline{CE} \geq V_{IH}$ <sup>[12]</sup> , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	—	—	40.0	mA
$I_{SB2}$	Automatic CE power down current – CMOS inputs	$\text{Max } V_{CC}, \overline{CE} \geq V_{CC} - 0.2$ V <sup>[12]</sup> , $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$	—	20.0	30.0	mA

### Notes

9.  $V_{IL(\text{min})} = -2.0$  V and  $V_{IH(\text{max})} = V_{CC} + 2$  V for pulse durations of less than 20 ns.

10. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8$  V (for a  $V_{CC}$  range of 1.65 V–2.2 V),  $V_{CC} = 3$  V (for a  $V_{CC}$  range of 2.2 V–3.6 V), and  $V_{CC} = 5$  V (for a  $V_{CC}$  range of 4.5 V–5.5 V),  $T_A = 25$  °C.

11. This parameter is guaranteed by design and is not tested.

12. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

## Capacitance

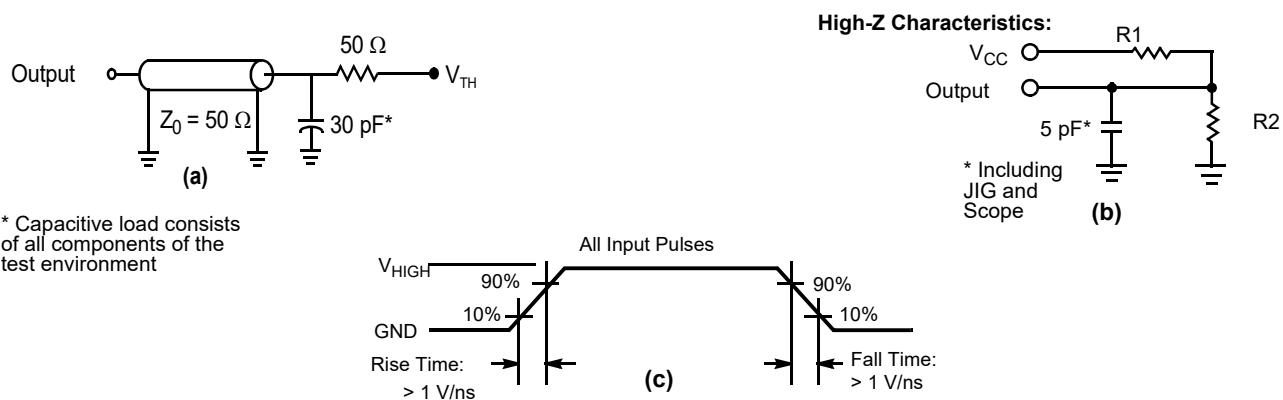
Parameter <sup>[13]</sup>	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	48-pin TSOP I	Unit
$C_{IN}$	Input capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC(\text{typ})}$	10	10	10	pF
$C_{OUT}$	I/O capacitance		10	10	10	pF

## Thermal Resistance

Parameter <sup>[13]</sup>	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	48-pin TSOP I	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a $3 \times 4.5$ inch, four-layer printed circuit board	93.63	31.50	57.99	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		21.58	15.75	13.42	$^\circ\text{C/W}$

## AC Test Loads and Waveforms

Figure 11. AC Test Loads and Waveforms<sup>[14]</sup>



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	$\Omega$
R2	1538	351	351	$\Omega$
$V_{TH}$	0.9	1.5	1.5	V
$V_{HIGH}$	1.8	3	3	V

### Notes

13. Tested initially and after any design or process changes that may affect these parameters.

14. Full-device AC operation assumes a 100- $\mu\text{s}$  ramp time from 0 to  $V_{CC}$  (min) and 100- $\mu\text{s}$  wait time after  $V_{CC}$  stabilizes to its operational value.



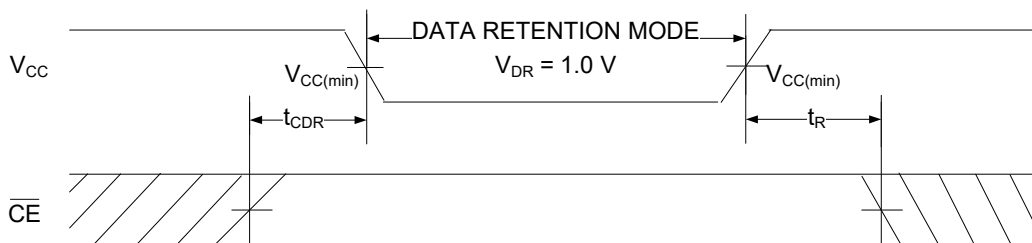
## Data Retention Characteristics

Over the operating range of  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.0	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = V_{DR}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}^{[15]}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	30.0	mA
$t_{CDR}^{[16]}$	Chip deselect to data retention time		0	–	ns
$t_R^{[16, 17]}$	Operation recovery time	$V_{CC} \geq 2.2\text{ V}$	10.0	–	ns
		$V_{CC} < 2.2\text{ V}$	15.0	–	ns

## Data Retention Waveform

**Figure 12. Data Retention Waveform** <sup>[15]</sup>



### Notes

15. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
16. This parameter is guaranteed by design and is not tested
17. Full-device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC}(\text{min}) \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC}(\text{min}) \geq 100\text{ }\mu\text{s}$ .

## AC Switching Characteristics

Over the operating range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

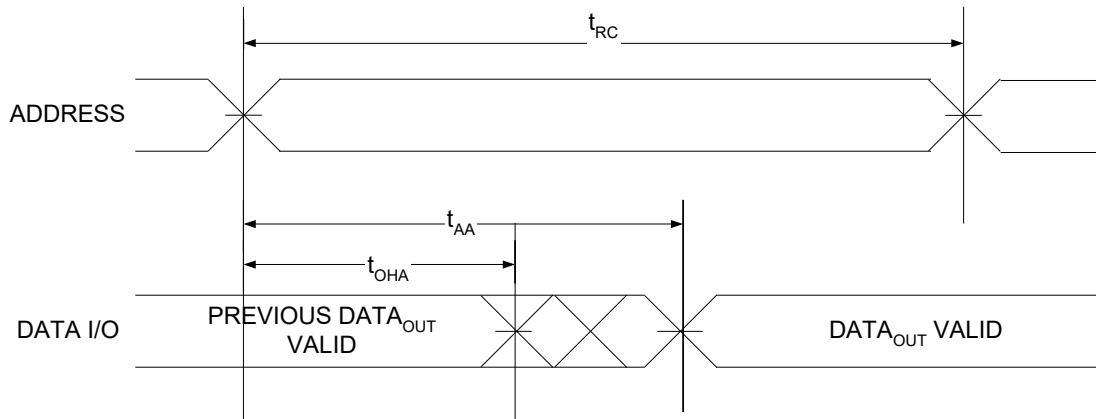
Parameter <sup>[18]</sup>	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t <sub>POWER</sub>	V <sub>CC</sub> (stable) to the first access <sup>[19, 20]</sup>	100.0	–	100.0	–	μs
t <sub>RC</sub>	Read cycle time	10.0	–	15.0	–	ns
t <sub>AA</sub>	Address to data / ERR valid	–	10.0	–	15.0	ns
t <sub>OHA</sub>	Data / ERR hold from address change	3.0	–	3.0	–	ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ LOW to data / ERR valid <sup>[21]</sup>	–	10.0	–	15.0	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to data / ERR valid	–	5.0	–	8.0	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to low Z <sup>[22, 23, 24]</sup>	0	–	1.0	–	ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to high Z <sup>[22, 23, 24]</sup>	–	5.0	–	8.0	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}$ LOW to low Z <sup>[21, 22, 23, 24]</sup>	3.0	–	3.0	–	ns
t <sub>HZCE</sub>	$\overline{\text{CE}}$ HIGH to high Z <sup>[21, 22, 23, 24]</sup>	–	5.0	–	8.0	ns
t <sub>PU</sub>	$\overline{\text{CE}}$ LOW to power-up <sup>[20, 21]</sup>	0	–	0	–	ns
t <sub>PD</sub>	$\overline{\text{CE}}$ HIGH to power-down <sup>[20, 21]</sup>	–	10.0	–	15.0	ns
t <sub>DBE</sub>	Byte enable to data valid	–	5.0	–	8.0	ns
t <sub>LZBE</sub>	Byte enable to low Z <sup>[22, 23]</sup>	0	–	1.0	–	ns
t <sub>HZBE</sub>	Byte disable to high Z <sup>[22, 23]</sup>	–	6.0	–	8.0	ns
Write Cycle <sup>[25, 26]</sup>						
t <sub>WC</sub>	Write cycle time	10.0	–	15.0	–	ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ LOW to write end <sup>[21]</sup>	7.0	–	12.0	–	ns
t <sub>AW</sub>	Address setup to write end	7.0	–	12.0	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	0	–	ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ pulse width	7.0	–	12.0	–	ns
t <sub>SD</sub>	Data setup to write end	5.0	–	8.0	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	0	–	ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to low Z <sup>[22, 23, 24]</sup>	3.0	–	3.0	–	ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to high Z <sup>[22, 23, 24]</sup>	–	5.0	–	8.0	ns
t <sub>BW</sub>	Byte Enable to write end	7.0	–	12.0	–	ns

### Notes

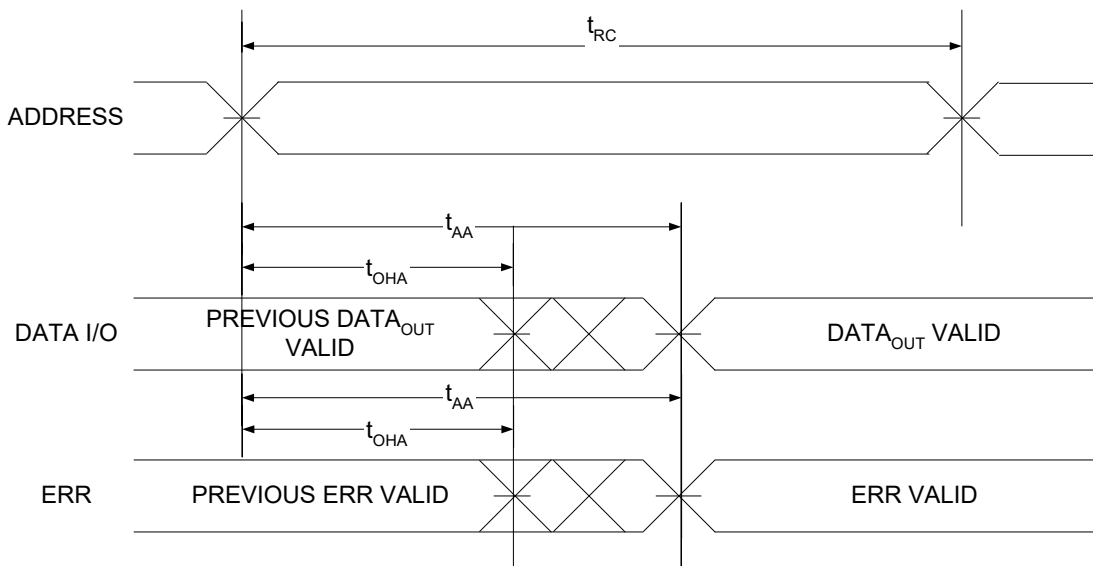
18. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{\text{CC}} \geq 3\text{ V}$ ) and  $V_{\text{CC}}/2$  (for  $V_{\text{CC}} < 3\text{ V}$ ), and input pulse levels of 0 to 3 V (for  $V_{\text{CC}} \geq 3\text{ V}$ ) and 0 to  $V_{\text{CC}}$  (for  $V_{\text{CC}} < 3\text{ V}$ ). Test conditions for the read cycle use the output loading, shown in part (a) of [Figure 11 on page 8](#), unless specified otherwise.
19.  $t_{\text{POWER}}$  gives the minimum amount of time that the power supply is at stable  $V_{\text{CC}}$  until the first memory access is performed.
20. These parameters are guaranteed by design and are not tested.
21. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
22.  $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ ,  $t_{\text{HZWE}}$ , and  $t_{\text{HZBE}}$  are specified with a load capacitance of 5 pF, as shown in part (b) of [Figure 11 on page 8](#). Hi-Z, Lo-Z transition is measured  $\pm 200\text{ mV}$  from steady state voltage.
23. At any temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZBE}}$  is less than  $t_{\text{LZBE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any device.
24. Tested initially and after any design or process changes that may affect these parameters.
25. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ , and  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}} = V_{\text{IL}}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
26. The minimum write pulse width for Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) should be sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

## Switching Waveforms

**Figure 13. Read Cycle No. 1 of CY7C1061G (Address Transition Controlled)** [27, 28]



**Figure 14. Read Cycle No. 2 of CY7C1061GE (Address Transition Controlled)** [27, 28]

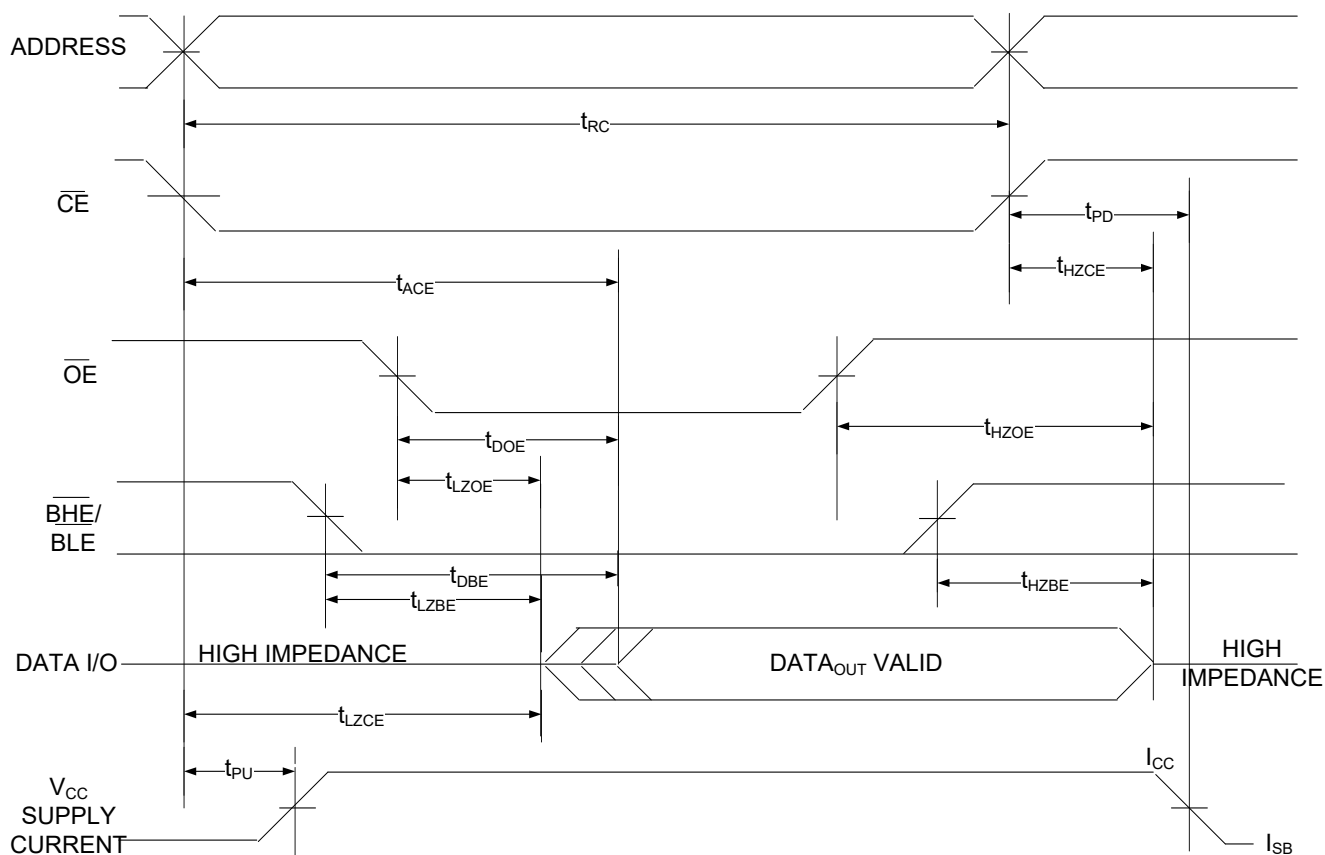


### Notes

27. The device is continuously selected,  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IL}$ .  
 28.  $\overline{WE}$  is HIGH for read cycle.

## Switching Waveforms (continued)

Figure 15. Read Cycle No. 3 ( $\overline{\text{OE}}$  Controlled) [29, 30, 31]

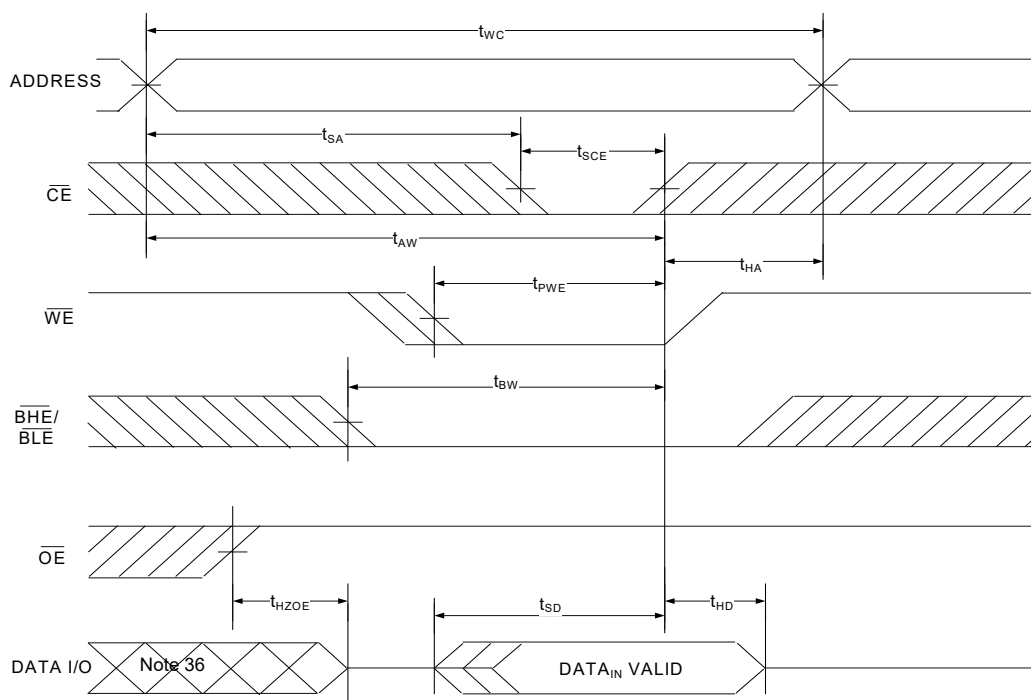


### Notes

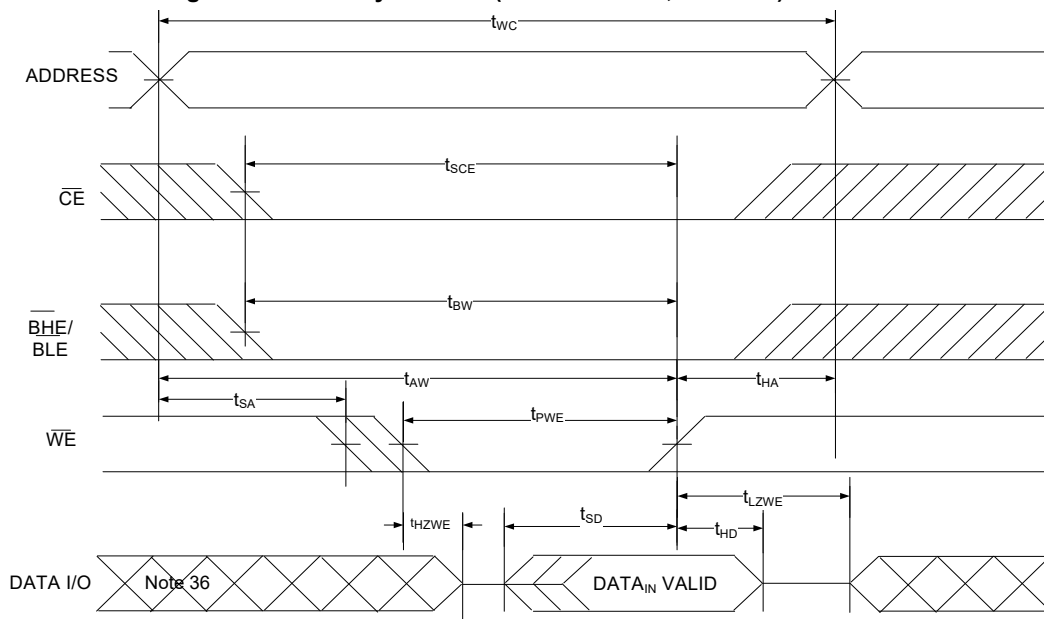
29. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
30.  $\overline{\text{WE}}$  is HIGH for read cycle.
31. Address valid prior to or coincident with  $\overline{\text{CE}}$  LOW transition.

## Switching Waveforms (continued)

**Figure 16. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)** [32, 33, 34]



**Figure 17. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)** [32, 33, 34, 35]

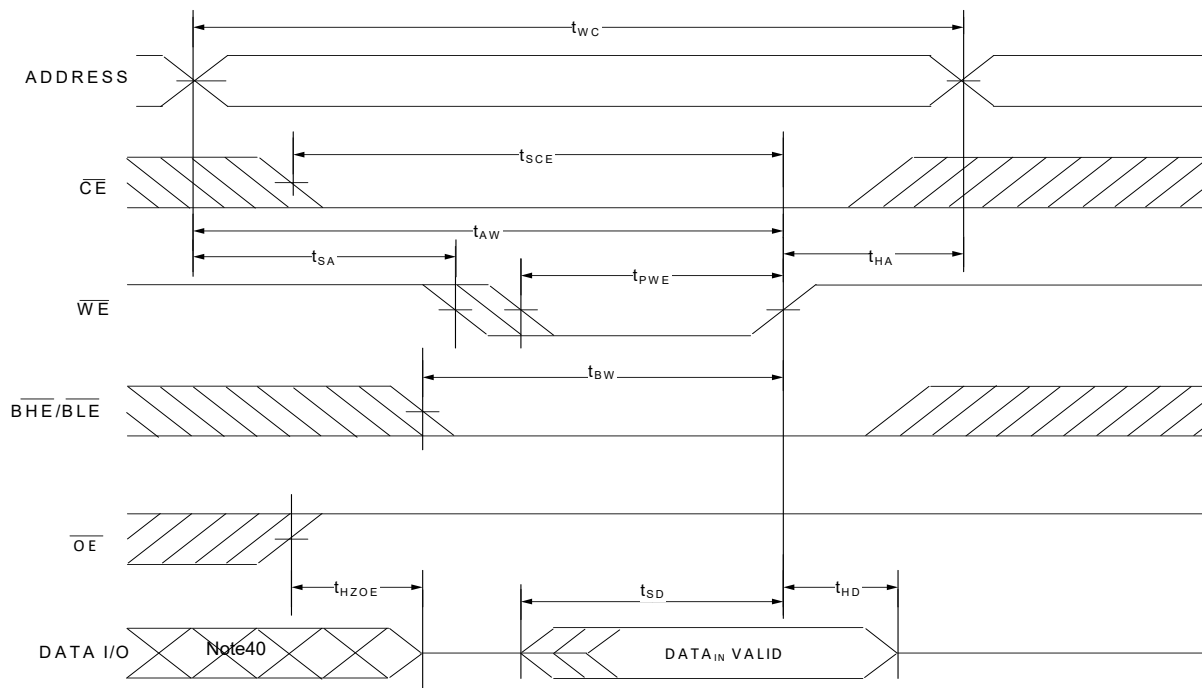


### Notes

32. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
33. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$  and  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}} = V_{\text{IL}}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
34. Data I/O is in high-impedance state if  $\overline{\text{CE}} = V_{\text{IH}}$ , or  $\overline{\text{OE}} = V_{\text{IH}}$  or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .
35. The minimum write cycle pulse width should be equal to sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .
36. During this period the I/Os are in output state. Do not apply input signals.

## Switching Waveforms (continued)

**Figure 18. Write Cycle No. 3 ( $\overline{WE}$  Controlled)** [37, 38, 39]



### Notes

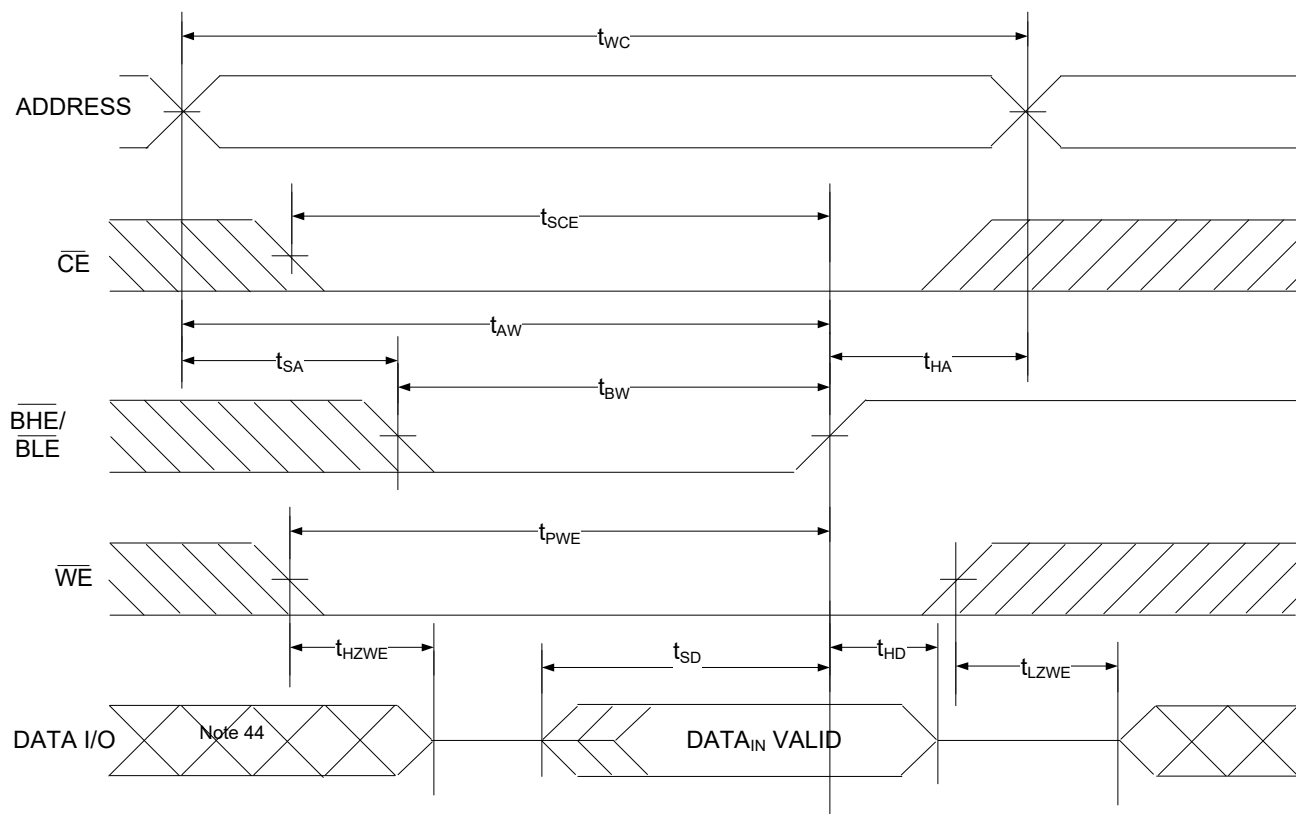
37. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

38. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$  and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

39. Data I/O is in high-impedance state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$  or  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ .

40. During this period, the I/Os are in output state. Do not apply input signals.

**Switching Waveforms** (continued)

**Figure 19. Write Cycle No. 4 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)** [41, 42, 43]

**Notes**

41. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
42. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$  and  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}} = V_{\text{IL}}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
43. Data I/O is in high-impedance state if  $\overline{\text{CE}} = V_{\text{IH}}$ , or  $\overline{\text{OE}} = V_{\text{IH}}$  or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .
44. During this period, the I/Os are in output state. Do not apply input signals.

## Truth Table

$\overline{CE}^{[45]}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X <sup>[46]</sup>	X <sup>[46]</sup>	X <sup>[46]</sup>	X <sup>[46]</sup>	High-Z	High-Z	Power down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data out	Data out	Read all bits	Active (I <sub>CC</sub> )
L	L	H	L	H	Data out	High-Z	Read lower bits only	Active (I <sub>CC</sub> )
L	L	H	H	L	High-Z	Data out	Read upper bits only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data in	Data in	Write all bits	Active (I <sub>CC</sub> )
L	X	L	L	H	Data in	High-Z	Write lower bits only	Active (I <sub>CC</sub> )
L	X	L	H	L	High-Z	Data in	Write upper bits only	Active (I <sub>CC</sub> )
L	H	H	X	X	High-Z	High-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )
L	X	X	H	H	High-Z	High-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

## ERR Output – CY7C1061GE

Output <sup>[47]</sup>	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
High-Z	Device deselected or outputs disabled or Write operation

### Notes

45. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

46. The input voltage levels on these pins should be either at  $V_{IH}$  or  $V_{IL}$ .

47. ERR is an Output pin. If not used, this pin should be left floating.



## Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Key Features / Differentiators	ERR Pin / Ball	Operating Range
10	4.5 V–5.5 V	CY7C1061G-10BV1XI	51-85150	48-ball VFBGA	Single Chip Enable, Address MSB A19 at ball G2	No	Industrial
		CY7C1061GE-10BV1XI				Yes	
		CY7C1061G-10BVJXI			Dual Chip Enable, Address MSB A19 at ball G2	No	
		CY7C1061GE-10BVJXI				Yes	
		CY7C1061G-10BVXI			Dual Chip Enable, Address MSB A19 at ball H6	No	
		CY7C1061GE-10BVXI				Yes	
		CY7C1061G-10ZSXI	51-85160	54-pin TSOP II	Dual Chip Enable	No	
		CY7C1061GE-10ZSXI				Yes	
		CY7C1061G-10ZXI	51-85183	48-pin TSOP I	Single Chip Enable	No	
		CY7C1061GE-10ZXI				Yes	
	2.2 V–3.6 V	CY7C1061G30-10BV1XI	51-85150	48-ball VFBGA	Single Chip Enable, Address MSB A19 at ball G2	No	
		CY7C1061GE30-10BV1XI				Yes	
		CY7C1061G30-10BVJXI			Dual Chip Enable, Address MSB A19 at ball G2	No	
		CY7C1061GE30-10BVJXI				Yes	
		CY7C1061G30-10BVXI			Dual Chip Enable, Address MSB A19 at ball H6	No	
		CY7C1061GE30-10BVXI				Yes	
		CY7C1061G30-10ZSXI	51-85160	54-pin TSOP II	Dual Chip Enable	No	
		CY7C1061GE30-10ZSXI				Yes	
		CY7C1061G30-10ZXI	51-85183	48-pin TSOP I	Single Chip Enable	No	
		CY7C1061GE30-10ZXI				Yes	
15	1.65 V–2.2 V	CY7C1061GE18-15BV1XI	51-85150	48-ball VFBGA	Single Chip Enable, Address MSB A19 at ball G2	Yes	
		CY7C1061G18-15BV1XI				No	
		CY7C1061GE18-15BVJXI			Dual Chip Enable, Address MSB A19 at ball G2	Yes	
		CY7C1061G18-15BVJXI				No	
		CY7C1061GE18-15BVXI			Dual Chip Enable, Address MSB A19 at ball H6	Yes	
		CY7C1061G18-15BVXI				No	
		CY7C1061GE18-15ZSXI	51-85160	54-pin TSOP II	Dual Chip Enable	Yes	
		CY7C1061G18-15ZSXI				No	
		CY7C1061GE18-15ZXI	51-85183	48-pin TSOP I	Single Chip Enable	Yes	
		CY7C1061G18-15ZXI				No	

**Ordering Information** (continued)

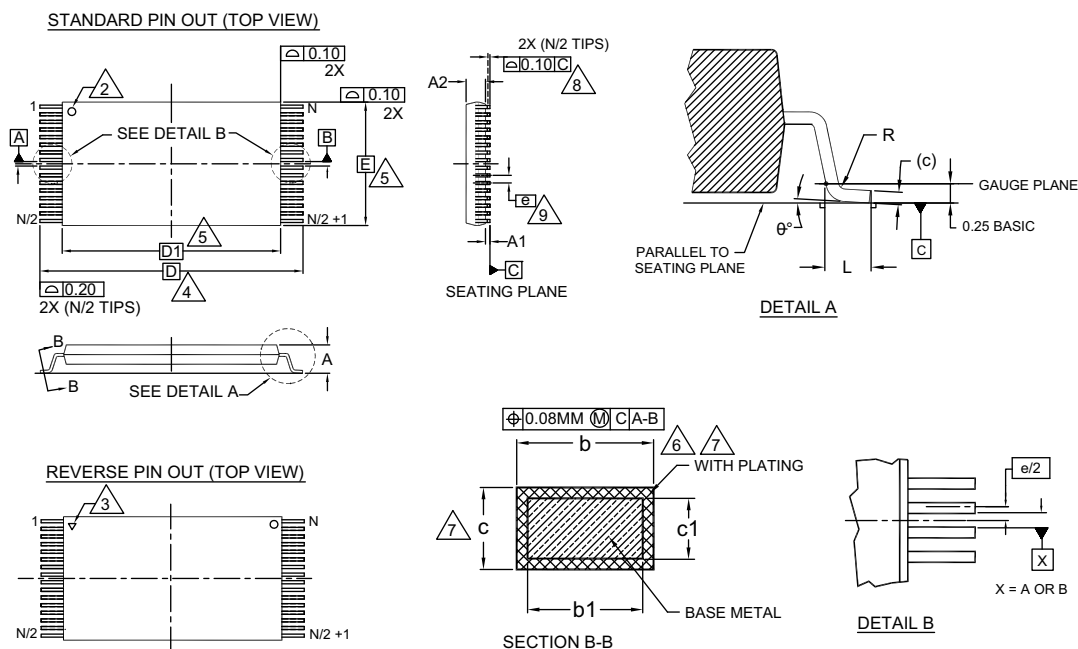
Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Key Features / Differentiators	ERR Pin / Ball	Operating Range
10	4.5 V–5.5 V	CY7C1061G-10BV1XIT	51-85150	48-ball VFBGA	Single Chip Enable, Address MSB A19 at ball G2, Tape and Reel	No	Industrial
		CY7C1061GE-10BV1XIT				Yes	
		CY7C1061G-10BVJXIT			Dual Chip Enable, Address MSB A19 at ball G2, Tape and Reel	No	
		CY7C1061GE-10BVJXIT				Yes	
		CY7C1061G-10BVXIT			Dual Chip Enable, Address MSB A19 at ball H6, Tape and Reel	No	
		CY7C1061GE-10BVXIT				Yes	
		CY7C1061G-10ZSXIT	51-85160	54-pin TSOP II	Dual Chip Enable, Tape and Reel	No	
		CY7C1061GE-10ZSXIT				Yes	
		CY7C1061G-10ZXIT	51-85183	48-pin TSOP I	Single Chip Enable, Tape and Reel	No	
		CY7C1061GE-10ZXIT				Yes	
	2.2 V–3.6 V	CY7C1061G30-10BV1XIT	51-85150	48-ball VFBGA	Single Chip Enable, Address MSB A19 at ball G2, Tape and Reel	No	Industrial
		CY7C1061GE30-10BV1XIT				Yes	
		CY7C1061G30-10BVJXIT			Dual Chip Enable, Address MSB A19 at ball G2, Tape and Reel	No	
		CY7C1061GE30-10BVJXIT				Yes	
		CY7C1061G30-10BVXIT			Dual Chip Enable, Address MSB A19 at ball H6, Tape and Reel	No	
		CY7C1061GE30-10BVXIT				Yes	
		CY7C1061G30-10ZSXIT	51-85160	54-pin TSOP II	Dual Chip Enable, Tape and Reel	No	
		CY7C1061GE30-10ZSXIT				Yes	
		CY7C1061G30-10ZXIT	51-85183	48-pin TSOP I	Single Chip Enable, Tape and Reel	No	
		CY7C1061GE30-10ZXIT				Yes	
15	1.65 V–2.2 V	CY7C1061GE18-15BV1XIT	51-85150	48-ball VFBGA	Single Chip Enable, Address MSB A19 at ball G2, Tape and Reel	Yes	Industrial
		CY7C1061G18-15BV1XIT				No	
		CY7C1061GE18-15BVJXIT			Dual Chip Enable, Address MSB A19 at ball G2, Tape and Reel	Yes	
		CY7C1061G18-15BVJXIT				No	
		CY7C1061GE18-15BVXIT			Dual Chip Enable, Address MSB A19 at ball H6, Tape and Reel	Yes	
		CY7C1061G18-15BVXIT				No	
		CY7C1061GE18-15ZSXIT	51-85160	54-pin TSOP II	Dual Chip Enable, Tape and Reel	Yes	
		CY7C1061G18-15ZSXIT				No	
		CY7C1061GE18-15ZXIT	51-85183	48-pin TSOP I	Single Chip Enable, Tape and Reel	Yes	
		CY7C1061G18-15ZXIT				No	

**Ordering Code Definitions**

CY	7	C	1	06	1	G	E	XX	-	XX	XX	X	I	X	
															X = blank or T blank = Bulk; T = Tape and Reel
															Temperature Range: I = Industrial
															Pb-free
															Package Type: XX = BV or ZS or Z BV = 48-ball VFBGA; ZS = 54-pin TSOP II; Z = 48-pin TSOP I
															Speed: XX = 10 ns or 15 ns
															Voltage Range: XX = no character or 30 or 18 no character = 4.5 V–5.5 V; 30 = 2.2 V–3.6 V; 18 = 1.65 V–2.2 V
															X = blank or E blank = without ERR output; E = with ERR output, Single bit error correction indicator
															Process Technology: Revision Code "G" = 65 nm
															Data Width: 1 = × 16-bits
															Density: 06 = 16-Mbit
															Family Code: 1 = Fast Asynchronous SRAM family
															Technology Code: C = CMOS
															Marketing Code: 7 = SRAM
															Company ID: CY = Cypress

## Package Diagrams

**Figure 20. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Z48A Package Outline, 51-85183**



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	12.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

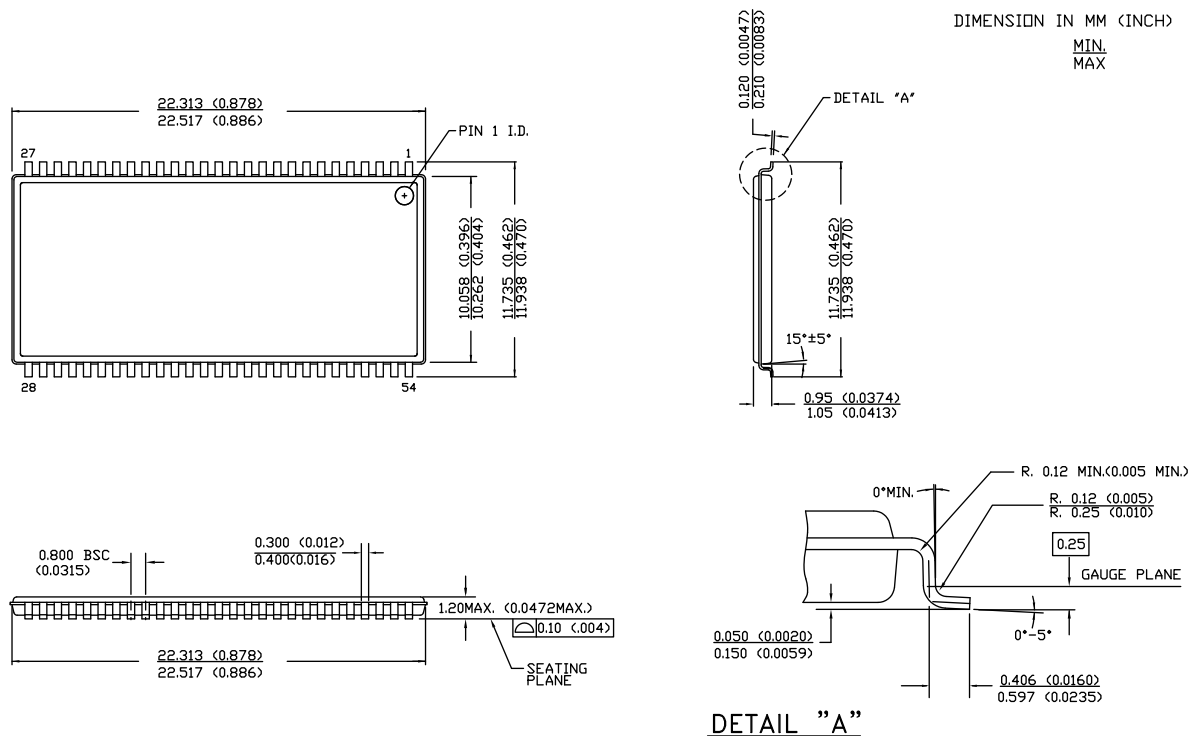
### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE [C]. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm.
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 \*F

## Package Diagrams (continued)

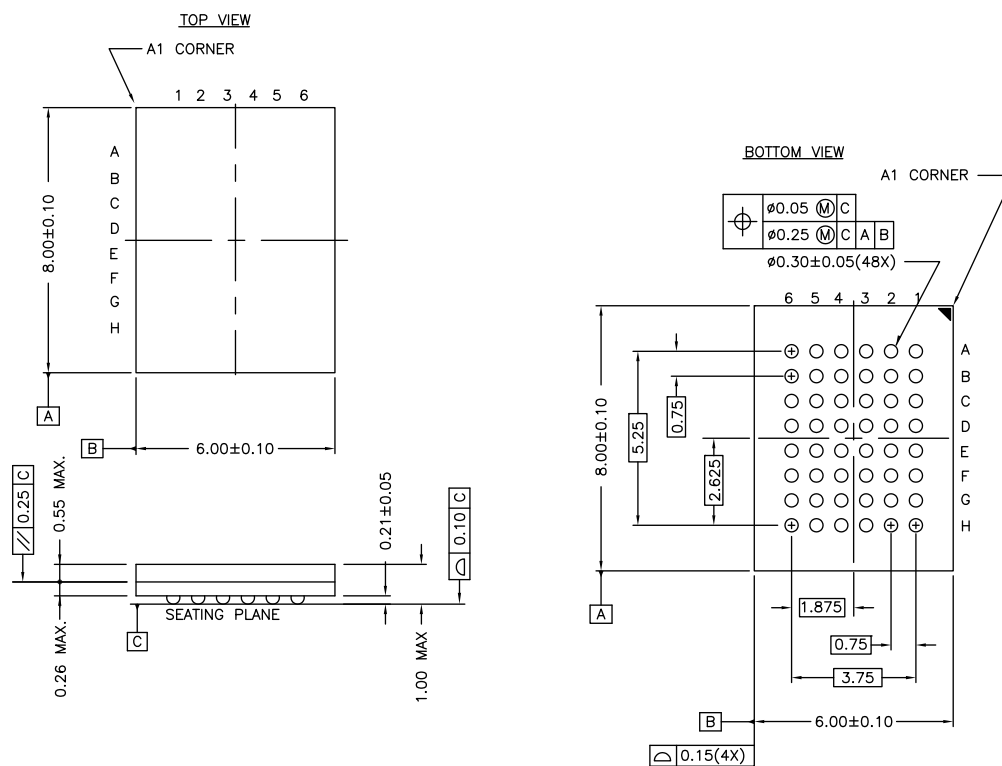
**Figure 21. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160**



51-85160 \*E

## Package Diagrams (continued)

**Figure 22. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150**



NOTE:

PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 \*H

## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C1061G/CY7C1061GE, 16-Mbit (1M words × 16-bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81540				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*P	4791835	NILE	06/09/2015	Changed status from Preliminary to Final.
*Q	5436639	NILE	09/14/2016	Updated <a href="#">Maximum Ratings</a> : Updated Note 9 (Replaced “2 ns” with “20 ns”). Updated <a href="#">DC Electrical Characteristics</a> : Removed Operating Range “2.7 V to 3.6 V” and all values corresponding to V <sub>OH</sub> parameter. Included Operating Ranges “2.7 V to 3.0 V” and “3.0 V to 3.6 V” and all values corresponding to V <sub>OH</sub> parameter. Changed minimum value of V <sub>IH</sub> parameter from 2.2 V to 2 V corresponding to Operating Range “4.5 V to 5.5 V”. Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated to new template.
*R	5580947	NILE	01/10/2017	Updated <a href="#">Logic Block Diagram – CY7C1061G</a> . Updated <a href="#">Package Diagrams</a> : spec 51-85183 – Changed revision from *D to *F. Updated to new template.
*S	5775815	AESATMP9	06/16/2017	Updated logo and copyright.
*T	6245720	NILE	07/13/2018	Updated <a href="#">Features</a> : Added Note 2 and referred the same note in “Embedded error-correcting code (ECC) for single-bit error correction”. Updated to new template. Completing Sunset Review.



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