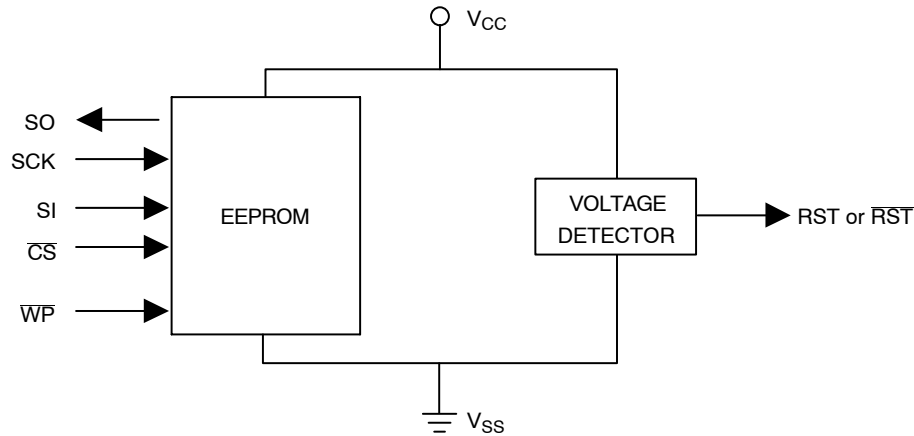


CAT15008, CAT15016

BLOCK DIAGRAM



SPECIFICATIONS

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Storage Temperature	-65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	-0.5 to +6.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The DC input voltage on any pin should not be lower than -0.5 V or higher than $V_{CC} + 0.5$ V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than $V_{CC} + 1.5$ V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
NEND (Note 3)	Endurance	1,000,000	Program/ Erase Cycles
TDR	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
3. Page Mode, $V_{CC} = 5$ V, 25°C

Table 3. D.C. OPERATING CHARACTERISTICS

$V_{CC} = +2.5$ V to +5.5 V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current	Read or Write at 10 MHz, SO open			2	mA
I_{SB}	Standby Current	$V_{CC} < 5.5$ V; $V_{IN} = V_{SS}$ or V_{CC} , $\overline{CS} = V_{CC}$		12	25	μ A
		$V_{CC} < 3.6$ V; $V_{IN} = V_{SS}$ or V_{CC} , $\overline{CS} = V_{CC}$		10	20	
I_L	I/O Pin Leakage	Pin at GND or V_{CC}			2	μ A
V_{IL}	Input Low Voltage		-0.5		$0.3 V_{CC}$	V
V_{IH}	Input High Voltage		$0.7 V_{CC}$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	$V_{CC} \geq 2.5$ V, $I_{OL} = 3.0$ mA			0.4	V
V_{OH}	Output High Voltage	$V_{CC} \geq 2.5$ V, $I_{OH} = -1.6$ mA	$V_{CC} - 0.8$			V

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Table 4. A.C. CHARACTERISTICS (MEMORY) (Note 1)

$V_{CC} = 2.5\text{ V to }5.5\text{ V}$, $T_A = -40^{\circ}\text{C to }85^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Min	Max	Units
f_{SCK}	Clock Frequency	DC	10	MHz
t_{SU}	Data Setup Time	20		ns
t_H	Data Hold Time	20		ns
t_{WH}	SCK High Time	40		ns
t_{WL}	SCK Low Time	40		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z		25	ns
t_{RI} (Note 2)	Input Rise Time		2	μs
t_{FI} (Note 2)	Input Fall Time		2	μs
t_{HD}	$\overline{HOLD}$ Setup Time	0		ns
t_{CD}	$\overline{HOLD}$ Hold Time	10		ns
t_V	Output Valid from Clock Low		40	ns
t_{HO}	Output Hold Time	0		ns
t_{DIS}	Output Disable Time		20	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z		25	ns
t_{CS}	$\overline{CS}$ High Time	15		ns
t_{CSS}	$\overline{CS}$ Setup Time	15		ns
t_{CSH}	$\overline{CS}$ Hold Time	15		ns
t_{WPS}	$\overline{WP}$ Setup Time	10		ns
t_{WPH}	$\overline{WP}$ Hold Time	10		ns
t_{WC} (Note 4)	Write Cycle Time		5	ms
t_{PU} (Notes 2 & 3)	Power-up to Ready Mode		1	ms

1. Test conditions according to "A.C. Test Conditions" table.
2. Tested initially and after a design or process change that affects this parameter.
3. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.
4. t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence to the end of the internal write cycle.

Table 5. A.C. TEST CONDITIONS

Parameter	Test Conditions
Input Rise and Fall Times	$\leq 10\text{ ns}$
Input Levels	$0.3\text{ }V_{CC}\text{ to }0.7\text{ }V_{CC}$
Timing Reference Levels	$0.5\text{ }V_{CC}$
Output Load	Current Source: $I_{OL}\text{ max/ }I_{OH}\text{ max}$; $C_L = 50\text{ pF}$

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Table 6. ELECTRICAL CHARACTERISTICS (SUPERVISORY FUNCTION)

V_{CC} = Full range, T_A = -40°C to $+85^{\circ}\text{C}$ unless otherwise noted. Typical values at T_A = $+25^{\circ}\text{C}$ and V_{CC} = 5 V for L/M/J versions, V_{CC} = 3.3 V for T/S versions, V_{CC} = 3 V for R version and V_{CC} = 2.5 V for Z version.

Symbol	Parameter	Threshold	Conditions	Min	Typ	Max	Units
V_{TH}	Reset Threshold Voltage	L	$T_A = +25^{\circ}\text{C}$	4.56	4.63	4.70	V
			$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	4.50		4.75	
		M	$T_A = +25^{\circ}\text{C}$	4.31	4.38	4.45	
			$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	4.25		4.50	
		J	$T_A = +25^{\circ}\text{C}$	3.93	4.00	4.06	
			$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	3.89		4.10	
		T	$T_A = +25^{\circ}\text{C}$	3.04	3.08	3.11	
			$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	3.00		3.15	
		S	$T_A = +25^{\circ}\text{C}$	2.89	2.93	2.96	
			$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	2.85		3.00	
		R	$T_A = +25^{\circ}\text{C}$	2.59	2.63	2.66	
			$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	2.55		2.70	
		Z	$T_A = +25^{\circ}\text{C}$	2.28	2.32	2.35	
			$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	2.25		2.38	
Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
	Reset Threshold Tempco				30		ppm/ $^{\circ}\text{C}$
t_{RPD}	V_{CC} to Reset Delay (Note 2)	$V_{CC} = V_{TH}$ to $(V_{TH} - 100 \text{ mV})$			20		μs
t_{PURST}	Reset Active Timeout Period	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		140	240	460	ms
V_{OL}	RESET Output Voltage Low (Push-pull, Active LOW, CAT150xx9)	$V_{CC} = V_{TH} \text{ min, } I_{SINK} = 1.2 \text{ mA}$ R/S/T/Z				0.3	V
		$V_{CC} = V_{TH} \text{ min, } I_{SINK} = 3.2 \text{ mA}$ J/L/M				0.4	
		$V_{CC} > 1.0 \text{ V, } I_{SINK} = 50 \mu\text{A}$				0.3	
V_{OH}	RESET Output Voltage High (Push-pull, Active LOW, CAT150xx9)	$V_{CC} = V_{TH} \text{ max, } I_{SOURCE} = -500 \mu\text{A}$ R/S/T/Z		$0.8 V_{CC}$			V
		$V_{CC} = V_{TH} \text{ max, } I_{SOURCE} = -800 \mu\text{A}$ J/L/M		$V_{CC} - 1.5$			
V_{OL}	RESET Output Voltage Low (Push-pull, Active HIGH, CAT150xx1)	$V_{CC} > V_{TH} \text{ max, } I_{SINK} = 1.2 \text{ mA}$ R/S/T/Z				0.3	V
		$V_{CC} > V_{TH} \text{ max, } I_{SINK} = 3.2 \text{ mA}$ J/L/M				0.4	
V_{OH}	RESET Output Voltage High (Push-pull, Active HIGH, CAT150xx1)	$1.8 \text{ V} < V_{CC} \leq V_{TH} \text{ min,}$ $I_{SOURCE} = -150 \mu\text{A}$		$0.8 V_{CC}$			V

1. Production testing done at $T_A = +25^{\circ}\text{C}$; limits over temperature guaranteed by design only.
2. RESET output for the CAT150xx9; RESET output for the CAT150xx1.

PIN DESCRIPTION

RESET/RESET: Reset output is available in two versions: CMOS Active Low (CAT150xx9) and CMOS Active High (CAT150xx1). Both versions are push-pull outputs for high efficiency.

SI: The serial data input pin accepts op-codes, addresses and data. In SPI modes (0,0) and (1,1) input data is latched on the rising edge of the SCK clock input.

SO: The serial data output pin is used to transfer data out of the device. In SPI modes (0,0) and (1,1) data is shifted out on the falling edge of the SCK clock.

SCK: The serial clock input pin accepts the clock provided by the host and used for synchronizing communication between host and CAT15008/16.

$\overline{CS}$: The chip select input pin is used to enable/disable the CAT15008/16. When $\overline{CS}$ is high, the SO output is tri-stated (high impedance) and the device is in Standby Mode (unless an internal write operation is in progress). Every communication session between host and CAT15008/16 must be preceded by a high to low transition and concluded with a low to high transition of the $\overline{CS}$ input.

$\overline{WP}$: The write protect input pin will allow all write operations to the device when held high. When $\overline{WP}$ pin is tied low and the WPEN bit in the Status Register (refer to Status Register description, later in this Data Sheet) is set to “1”, writing to the Status Register is disabled.

DEVICE OPERATION

The CAT15008/16 products combine the accurate voltage monitoring capabilities of a standalone voltage supervisor

with the high quality and reliability of standard EEPROMs from ON Semiconductor.

RESET CONTROLLER DESCRIPTION

The reset signal is asserted LOW for the CAT150xx9 and HIGH for the CAT150xx1 when the power supply voltage falls below the threshold trip voltage and remains asserted for at least 140 ms (t_{PURST}) after the power supply voltage has risen above the threshold. Reset output timing is shown in Figure 2.

The CAT15008/16 devices protect μ Ps against brown-out failure. Short duration V_{CC} transients of 4 μ sec or less and 100 mV amplitude typically do not generate a Reset pulse.

Figure 1 shows the maximum pulse duration of negative-going V_{CC} transients that do not cause a reset condition. As the amplitude of the transient goes further below the threshold (increasing $V_{TH} - V_{CC}$), the maximum pulse duration decreases. In this test, the V_{CC} starts from an initial voltage of 0.5 V above the threshold and drops below it by the amplitude of the overdrive voltage ($V_{TH} - V_{CC}$).

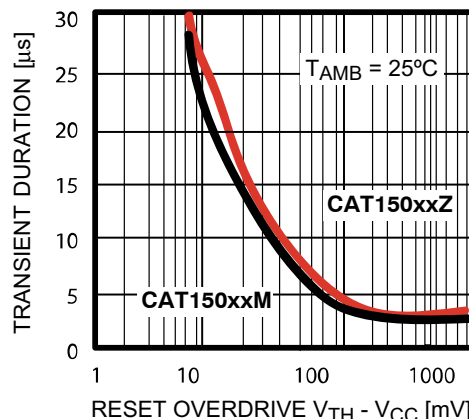


Figure 1. Maximum Transient Duration without Causing a Reset Pulse vs. Overdrive Voltage

CAT15008, CAT15016

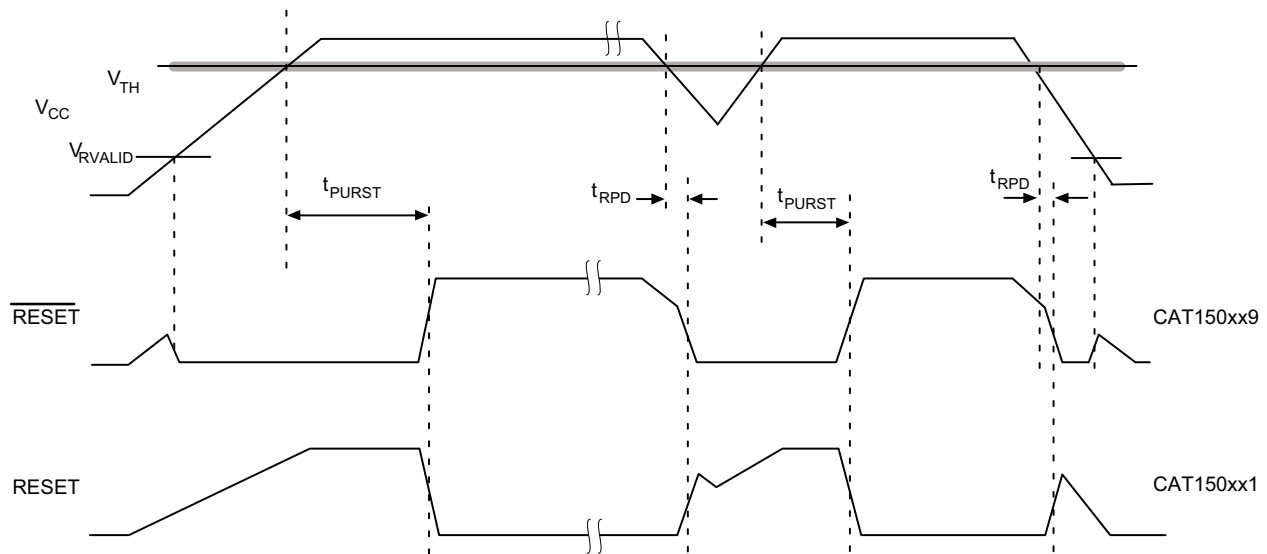


Figure 2. RESET Output Timing

EMBEDDED EEPROM DESCRIPTION

The CAT15008/16 devices support the Serial Peripheral Interface (SPI) bus protocol, modes (0,0) and (1,1). The device contains an 8-bit instruction register. The instruction set and associated op-codes are listed in Table 7.

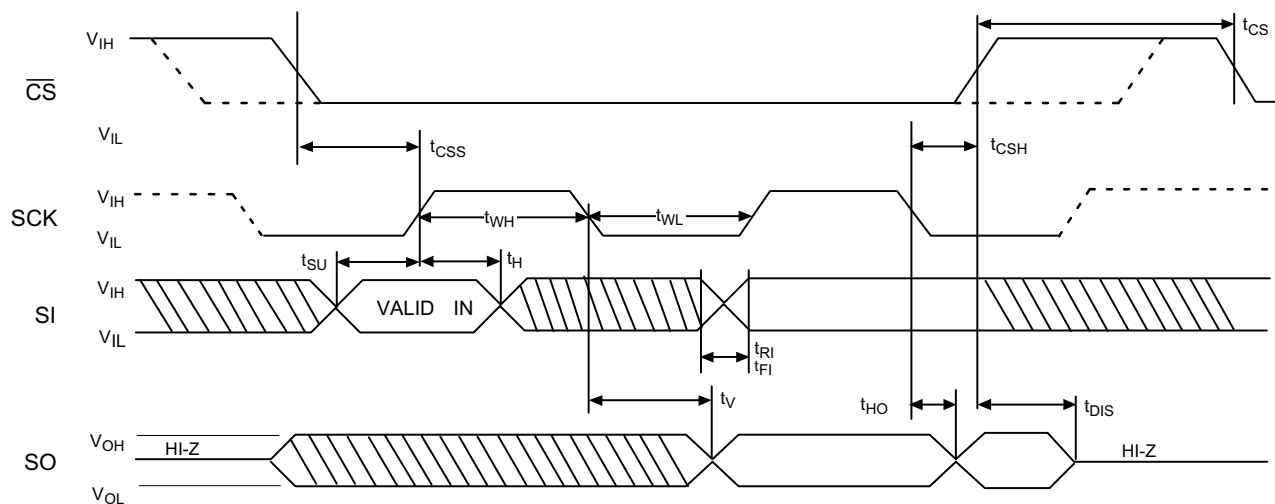
Reading data stored in the CAT15008/16 is accomplished by simply providing the READ command and an address. Writing to the CAT15008/16, in addition to a WRITE command, address and data, also requires enabling the device for writing by first setting certain bits in a Status Register, as will be explained later.

After a high to low transition on the $\overline{CS}$ input pin, the CAT15008/16 will accept any one of the six instruction op-codes listed in Table 7 and will ignore all other possible

8-bit combinations. The communication protocol follows the timing from Figure 3.

Table 7. INSTRUCTION SET

Instruction	Opcode	Operation
WREN	0000 0110	Enable Write Operations
WRDI	0000 0100	Disable Write Operations
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory
WRITE	0000 0010	Write Data to Memory



Note: Dashed Line = mode (1, 1)-----

Figure 3. Synchronous Data Timing

STATUS REGISTER

The Status Register, as shown in Table 8, contains a number of status and control bits.

The **RDY** (Ready) bit indicates whether the device is busy with a write operation. This bit is automatically set to 1 during an internal write cycle, and reset to 0 when the device is ready to accept commands. For the host, this bit is read only.

The **WEL** (Write Enable Latch) bit is set/reset by the **WREN/WRDI** commands. When set to 1, the device is in a Write Enable state and when set to 0, the device is in a Write Disable state.

The **BP0** and **BP1** (Block Protect) bits determine which blocks are currently write protected. They are set by the user with the **WRSR** command and are non-volatile. The user is

allowed to protect a quarter, one half or the entire memory, by setting these bits according to Table 9. The protected blocks then become read-only.

The **WPEN** (Write Protect Enable) bit acts as an enable for the **WP** pin. Hardware write protection is enabled when the **WP** pin is low and the **WPEN** bit is 1. This condition prevents writing to the status register and to the block protected sections of memory. While hardware write protection is active, only the non-block protected memory can be written. Hardware write protection is disabled when the **WP** pin is high or the **WPEN** bit is 0. The **WPEN** bit, **WP** pin and **WEL** bit combine to either permit or inhibit Write operations, as detailed in Table 10.

Table 8. STATUS REGISTER

7	6	5	4	3	2	1	0
WPEN	0	0	0	BP1	BP0	WEL	RDY

Table 9. BLOCK PROTECTION BITS

Status Register Bits		Array Address Protected	Protection
BP1	BP0		
0	0	None	No Protection
0	1	15008: 0300–03FF	Quarter Array Protection
		15016: 0600–07FF	
1	0	15008: 0200–03FF	Half Array Protection
		15016: 0400–07FF	
1	1	15008: 0000–03FF	Full Array Protection
		15016: 0000–07FF	

Table 10. WRITE PROTECT ENABLE OPERATION

WPEN	WP	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

WRITE OPERATIONS

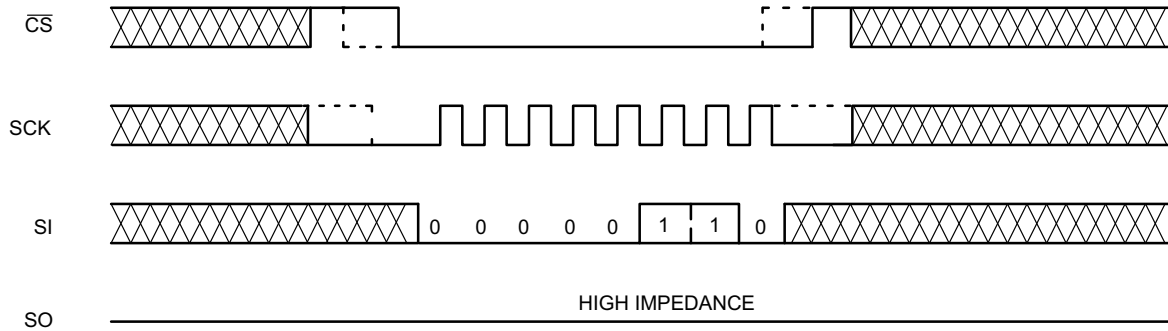
The CAT15008/16 device powers up into a write disable state. The device contains a Write Enable Latch (WEL) which must be set before attempting to write to the memory array or to the status register. In addition, the address of the memory location(s) to be written must be outside the protected area, as defined by BP0 and BP1 bits from the status register.

Write Enable and Write Disable

The internal Write Enable Latch and the corresponding Status Register WEL bit are set by sending the WREN

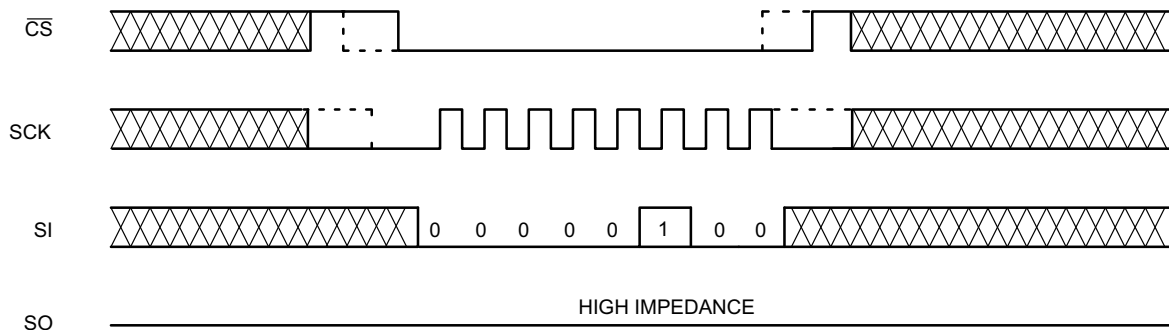
instruction to the CAT15008/16. Care must be taken to take the $\overline{CS}$ input high after the WREN instruction, as otherwise the Write Enable Latch will not be properly set. WREN timing is illustrated in Figure 4. The WREN instruction must be sent prior any WRITE or WRSR instruction.

The internal write enable latch is reset by sending the WRDI instruction as shown in Figure 5. Disabling write operations by resetting the WEL bit, will protect the device against inadvertent writes.



Note: Dashed Line = mode (1, 1)-----

Figure 4. WREN Timing



Note: Dashed Line = mode (1, 1)-----

Figure 5. WRDI Timing

Byte Write

Once the WEL bit is set, the user may execute a write sequence, by sending a WRITE instruction, a 16-bit address and data as shown in Figure 6. Only 10 significant address bits are used by the CAT15008 and 11 by the CAT15016. The rest are don't care bits, as shown in Table 11. Internal programming will start after the low to high $\overline{CS}$ transition. During an internal write cycle, all commands, except for RDSR (Read Status Register) will be ignored. The $\overline{RDY}$ bit will indicate if the internal write cycle is in progress ($\overline{RDY}$ high), or the device is ready to accept commands ($\overline{RDY}$ low).

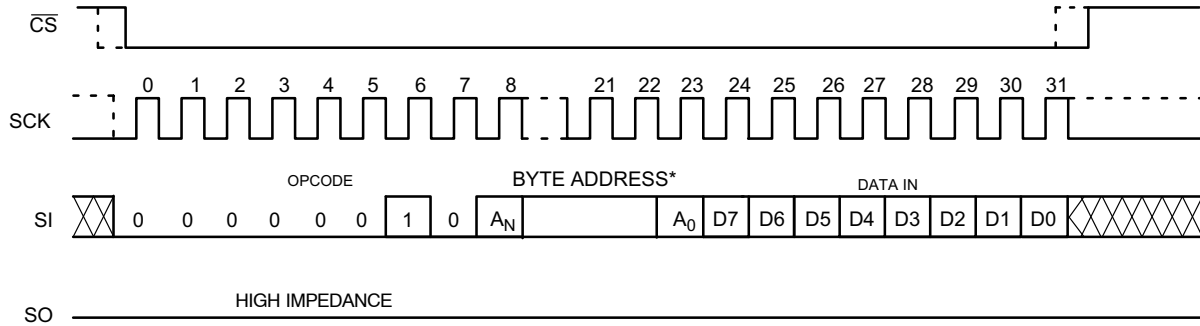
Page Write

After sending the first data byte to the CAT15008/16, the host may continue sending data, up to a total of 32 bytes, according to timing shown in Figure 7. After each data byte, the lower order address bits are automatically incremented, while the higher order address bits (page address) remain unchanged. If during this process the end of page is exceeded, then loading will "roll over" to the first byte in the page, thus possibly overwriting previously loaded data. Following completion of the write cycle, the CAT15008/16 is automatically returned to the write disable state.

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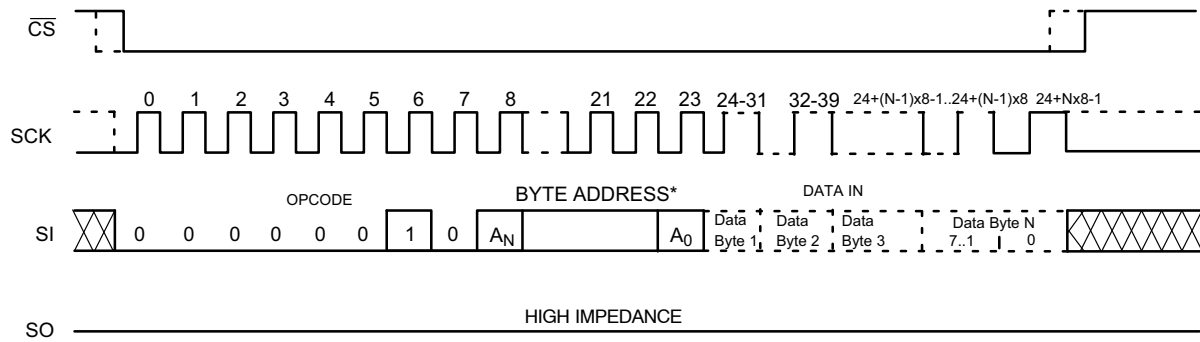
Table 11. BYTE ADDRESS

Device	Address Significant Bits	Address Don't Care Bits	# Address Clock Pulse
CAT15008	A9 – A0	A15 – A10	16
CAT15016	A10 – A0	A15 – A11	16



Notes: * Please check the Byte Address Table (Table 11)
Dashed Line = mode (1, 1)-----

Figure 6. Byte WRITE Timing



Notes: * Please check the Byte Address Table (Table 11)
Dashed Line = mode (1, 1)-----

Figure 7. Page WRITE Timing

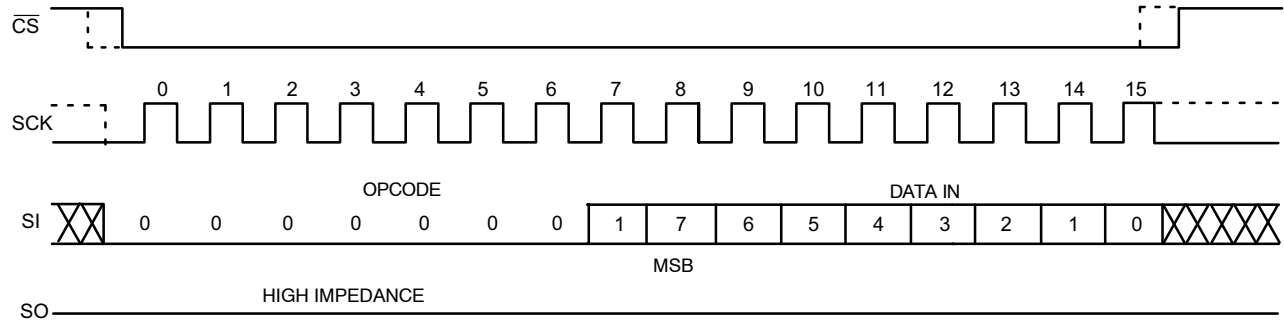
CAT15008, CAT15016

Write Status Register

The Status Register is written by sending a WRSR instruction according to timing shown in Figure 8. Only bits 2, 3 and 7 can be written using the WRSR command.

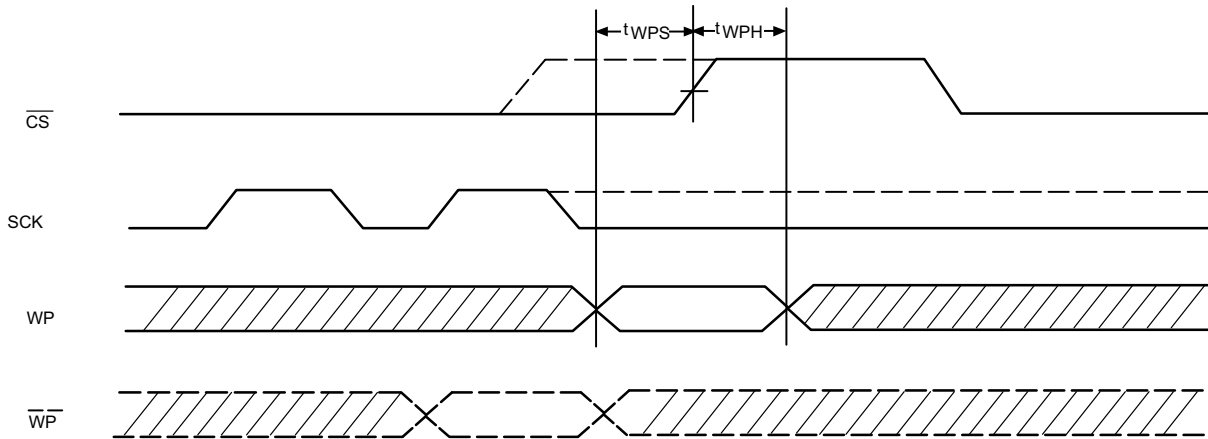
Write Protection

The Write Protect ($\overline{WP}$) pin can be used to protect the Block Protect bits BP0 and BP1 against being inadvertently altered. When $\overline{WP}$ is low and the WPEN bit is set to "1", write operations to the Status Register are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the Status Register. The $\overline{WP}$ pin function is blocked when the WPEN bit is set to "0". The $\overline{WP}$ input timing is shown in Figure 9.



Note: Dashed Line = mode (1, 1)-----

Figure 8. WRSR Timing



Note: Dashed Line = mode (1, 1)-----

Figure 9. WP Timing

READ OPERATIONS

Read from Memory Array

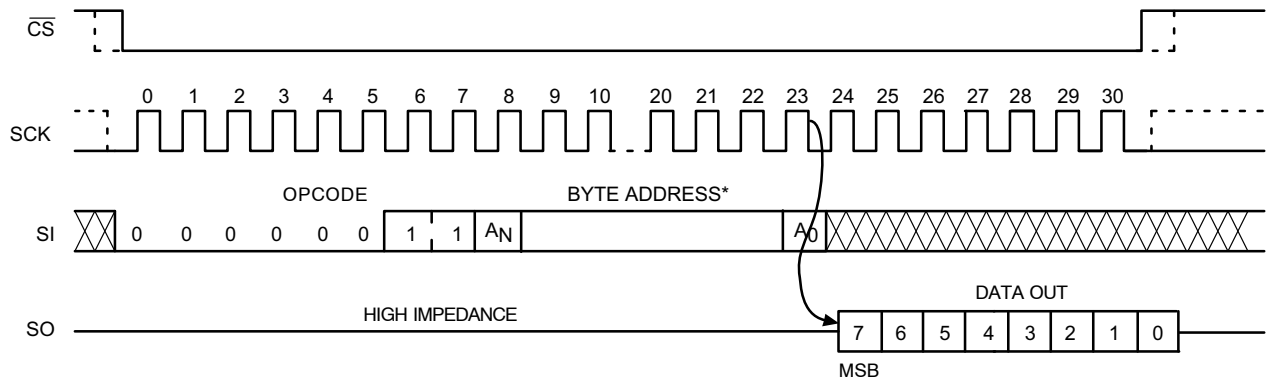
To read from memory, the host sends a READ instruction followed by an 16-bit address (see Table 11 for the number of significant address bits).

After receiving the last address bit, the CAT15008/16 will respond by shifting out data on the SO pin (as shown in Figure 10). Sequentially stored data can be read out by simply continuing to run the clock. The internal address pointer is automatically incremented to the next higher address as data is shifted out. After reaching the highest memory address, the address counter “rolls over” to the

lowest memory address, and the read cycle can be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ high.

Read Status Register

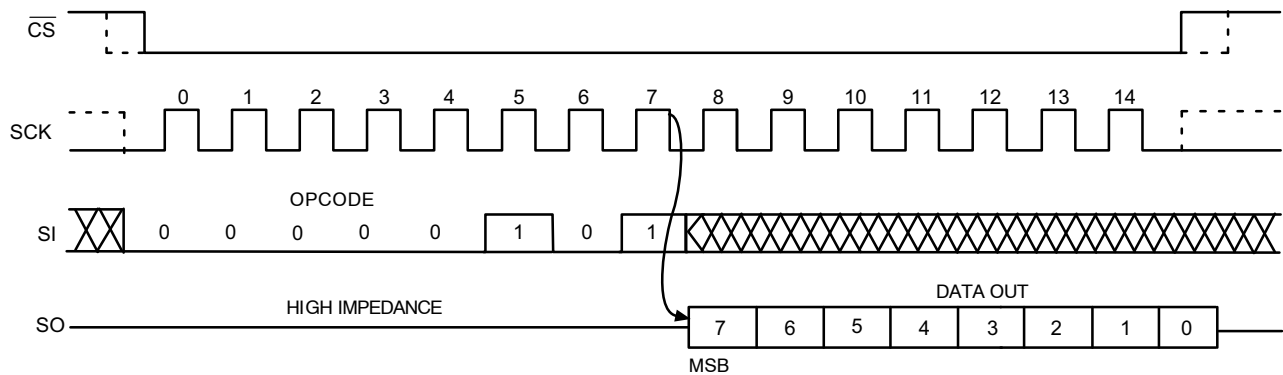
To read the status register, the host simply sends a RDSR command. After receiving the last bit of the command, the CAT15008/16 will shift out the contents of the status register on the SO pin (Figure 11). The status register may be read at any time, including during an internal write cycle.



Notes: * Please check the Byte Address Table (Table 11)

Dashed Line = mode (1, 1)-----

Figure 10. READ Timing



Note: Dashed Line = mode (1, 1)-----

Figure 11. RDSR Timing

CAT15008, CAT15016

ORDERING INFORMATION

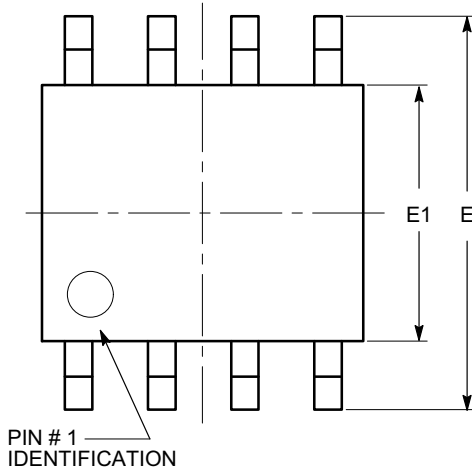
Orderable Part Numbers – CAT150xx Series (See Notes 1 – 4)			
Device	Reset Threshold Voltage	Package–Pins	Shipping
CAT150089SWI–GT3	2.85 to 3.00 V	SOIC–8	3000 Tape & Reel
CAT150089SWI–G	2.85 to 3.00 V		100 Tube
CAT150161MWI–GT3	4.25 to 4.50 V		3000 Tape & Reel
CAT150169MWI–GT3	4.25 to 4.50 V		
CAT150169SWI–GT3	2.85 to 3.00 V		

1. All packages are RoHS–compliant (Lead–free, Halogen–free).
2. The standard lead finish is NiPdAu pre–plated (PPF) lead frames.
3. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
4. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

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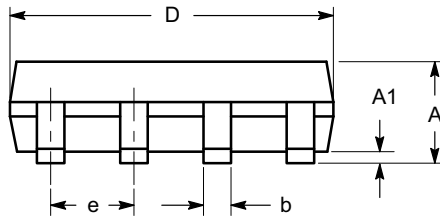
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD-01
ISSUE O

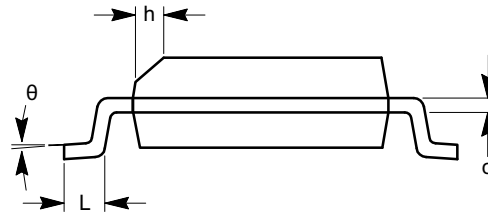


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW



END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

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