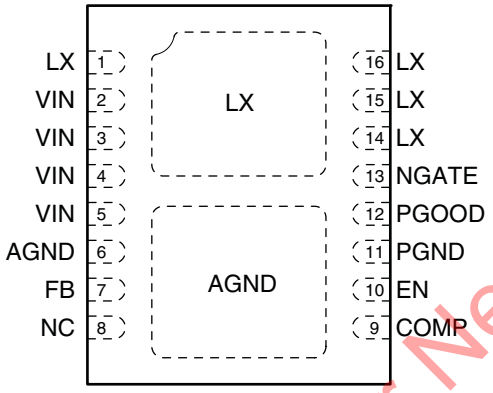
Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ1025DIL	-40°C to +85°C	5 x 4 DFN-16	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

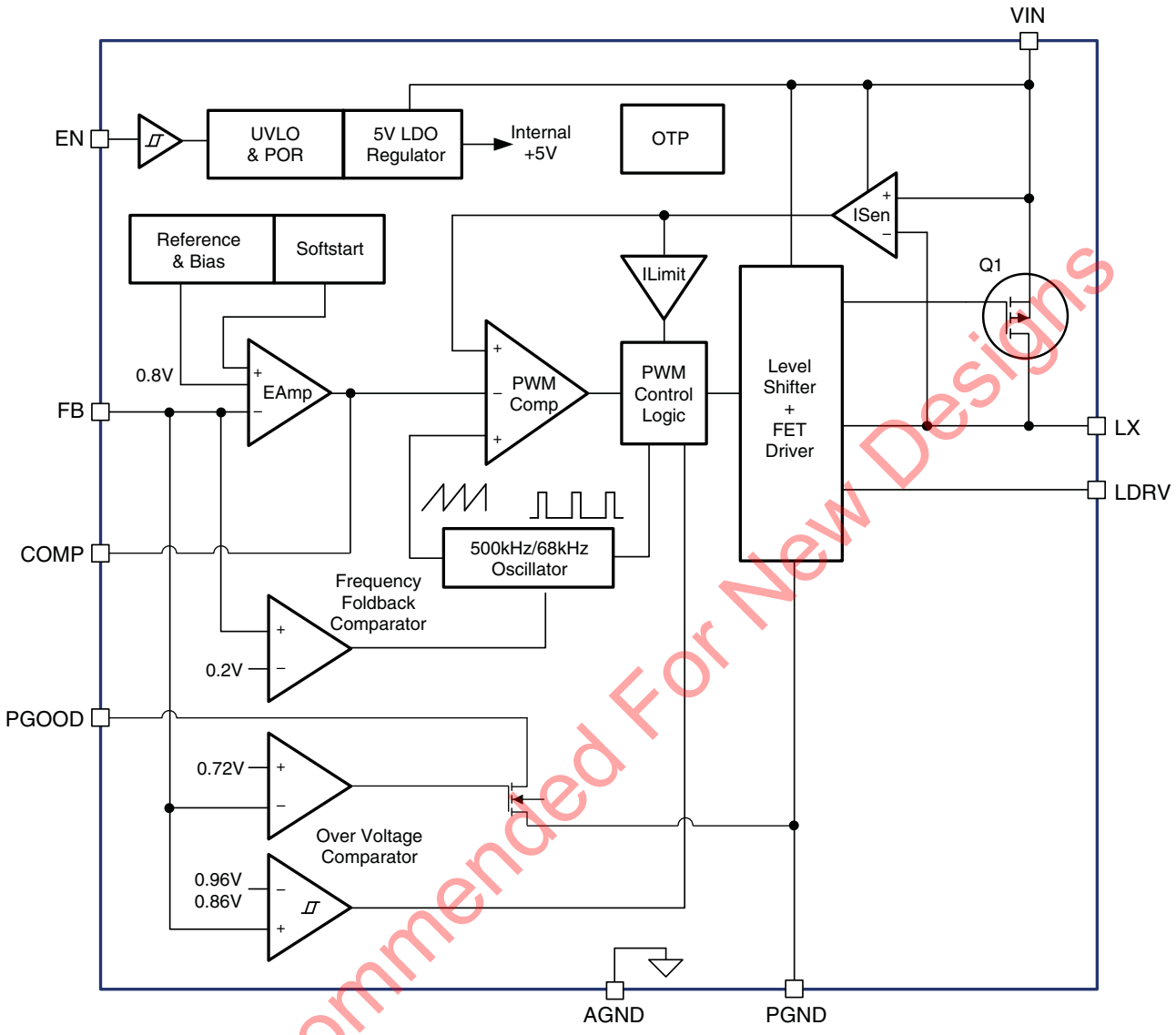


5 x 4 DFN-16
(Top Thru View)

Pin Description

Pin Number	Pin Name	Pin Function
1	LX	PWM output connection to inductor. Thermal connection for output stage.
2, 3, 4, 5	V_{IN}	Supply voltage input. When VIN rises above the UVLO threshold the device starts up.
6	AGND	Reference connection for controller section. Also used as thermal connection for controller section. Electrically needs to be connected to PGND
7	FB	The FB pin is used to determine the output voltage via a resistor divider between the output and GND.
8	NC	Not connected
9	COMP	External loop compensation pin.
10	EN	The enable pin is active high. Do not leave it open.
11	PGND	Power ground. Electrically needs to be connected to AGND.
12	PGOOD	Power Good. Open drain. Use resistor to pull up to 5V supply.
13	NGATE	Low side MOSFET driver; Connect it to the gate of external low side MOSFET.
14, 15, 16	LX	PWM output connection to inductor. Thermal connection for output stage.

Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Supply Voltage (V_{IN})	18V
LX to AGND	-0.7V to V_{IN}+0.3V
EN to AGND	-0.3V to V_{IN}+0.3V
FB to AGND	-0.3V to 6V
COMP to AGND	-0.3V to 6V
PGND to AGND	-0.3V to +0.3V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating(1)	2kV

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Recommend Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating Ratings.

Parameter	Rating
Supply Voltage (V_{IN})	4.75V to 16V
Output Voltage Range	0.8V to V_{IN}
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance 5 x 4 DFN-16 (Θ_{JA})(2)	50°C/W
Package Thermal Resistance 5 x 4 DFN-16 (Θ_{JC})(2)	5°C/W

Note:

2. The value of Θ_{JA} is measured with the device mounted on 1-in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.

Electrical Characteristics

T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 1.2V unless otherwise specified(3)

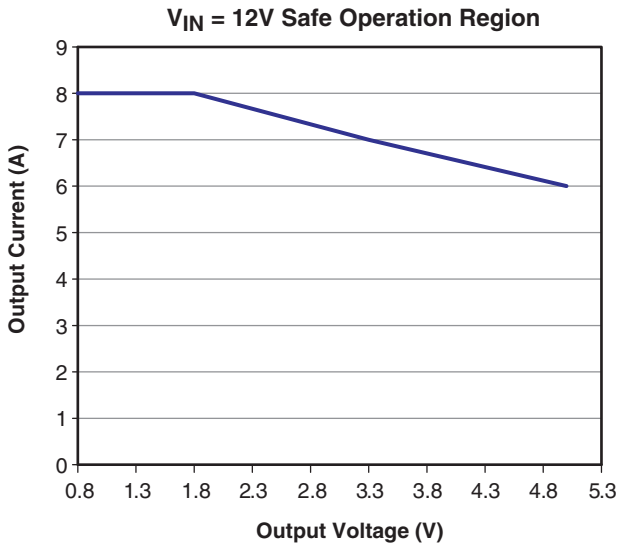
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN}	Supply Voltage		**4.75**		**16**	V
V_{UVLO}	Input Under-Voltage Lockout Threshold	V_{IN} Rising V_{IN} Falling		**4.1** **3.7**		V
I_{IN}	Supply Current (Quiescent)	I_{OUT} = 0, VFB = 1.2V, V_{EN} > 1.2V		**1.2**	**3**	mA
I_{OFF}	Shutdown Supply Current	V_{EN} = 0V			**30**	µA
V_{FB}	Feedback Voltage		0.788	0.8	0.812	V
	Load Regulation			0.5		%
	Line Regulation			0.2		%
I_{FB}	Feedback Voltage Input Current				200	nA
V_{EN}	EN Input Threshold	Off Threshold On Threshold	2		**0.6**	V
V_{HYS}	EN Input Hysteresis			100		mV
MODULATOR						
f_O	Frequency		350	500	600	kHz
D_{MAX}	Maximum Duty Cycle		100			%
D_{MIN}	Minimum Duty Cycle				6	%
	Error Amplifier Voltage Gain			500		V / V
	Error Amplifier Transconductance			200		µA / V
PROTECTION						
I_{LIM}	Current Limit			10		A
	Over-Temperature Shutdown Limit	T_J Rising T_J Falling		150 100		°C
V_{PR}	Output Over-voltage Protection Threshold	Off Threshold On Threshold		960 860		mV
t_{SS}	Soft Start Interval		3	4	6.5	ms
POWER GOOD						
V_{OLPG}	PG LOW Voltage	I_{OL} = 1mA			0.5	V
	PG Leakage				1	µA
V_{PGL}	PG Threshold Voltage		-12	-10	-8	%
	PG Threshold Voltage Hysteresis			3		%
	PG Delay Time			128		µs
OUTPUT STAGE						
	High-Side Switch On-Resistance	V_{IN} = 12V		43	57	mΩ
LOW SIDE DRIVER						
	Pull-up Resistance			20		Ω
	Pull-up Resistance			7		Ω

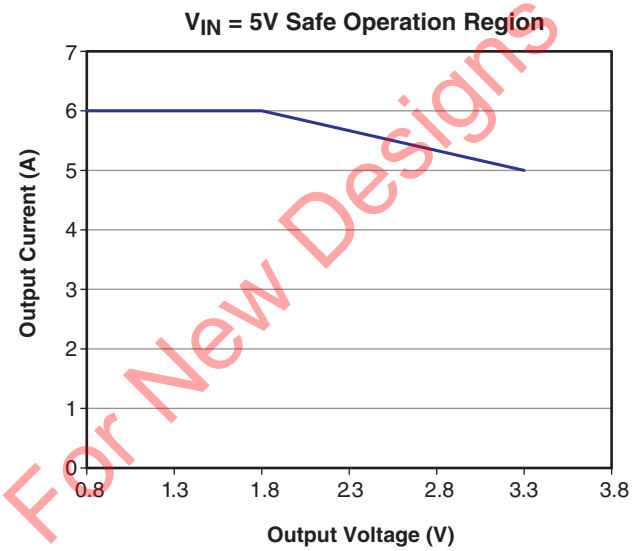
Note:
3. Specification in **BOLD** indicate an ambient temperature range of -40°C to +85°C. These specifications are guaranteed by design.

Maximum Output Current

Maximum output current of buck converters such as AOZ1025D is related with driving capability and thermal condition. AOZ1025D's driving voltage varies with the input voltage. When input voltage is higher than 6.5V, the driver inside the AOZ1025D can drive both high side and low side MOSFETs to deliver 8A output current; but when the input voltage is 5V, the recommended maximum output current is de-rated to 6A.

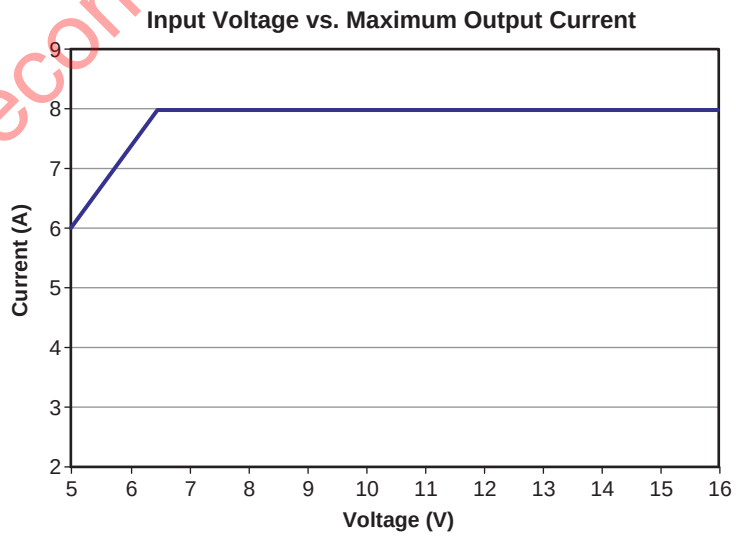
The output voltage within a fixed input voltage directed determines the turn-on ratio of integrated PMOS, and thus the thermal condition of AOZ1025D during the operation. The following diagrams show the safe operation region of AOZ1025 operating at V_{IN} = 5V, and V_{IN} = 12V respectively.





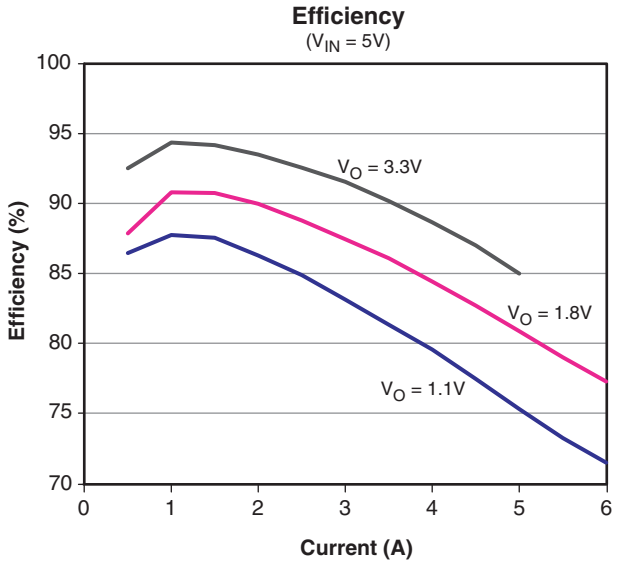
Input Voltage Vs. Maximum Output Current

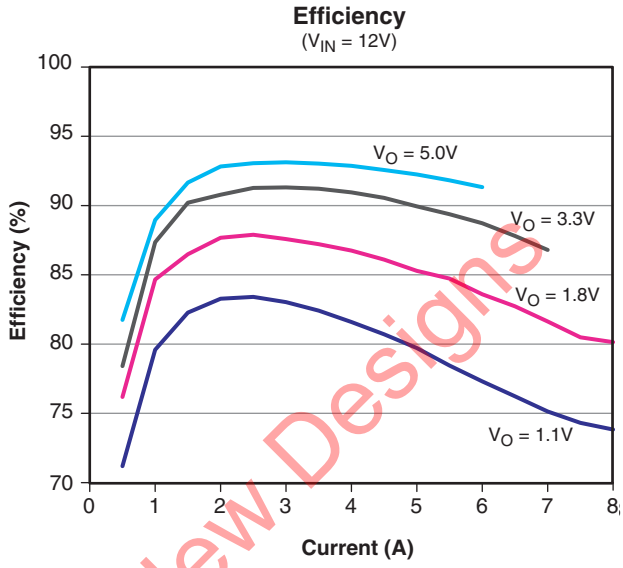
AOZ1025D's driving voltage varies with the input voltage.þWhen input voltage is higher than 6.5V, the driver inside the AOZ1025D can drive both high side and low side MOSFETs to deliver 8A output current; but when the input voltage is 5V, the recommended maximum output current is de-rated to 6A.þThe following diagram shows relations of the input voltage and the maximum output current of AOZ1025D.



Efficiency

The efficiency was measured based on Figure 1 with the low-side external MOSFET (AO4722).





Detailed Description

The AOZ1025D is a current-mode step down regulator with integrated high-side PMOS switch. It operates from a 4.75V to 16V input voltage range and supplies up to 8A of load current. The duty cycle can be adjusted from 6% to 100% allowing a wide range of output voltage. Features include enable control, Power-On Reset, input under voltage lockout, output over voltage protection, fixed internal soft-start and thermal shut down.

Enable and Soft Start

The AOZ1025D has internal soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. A soft start process begins when the input voltage rises to 4.0V and voltage on EN pin is HIGH. In soft start process, the output voltage is ramped to regulation voltage in typically 4ms. The 4ms soft start time is set internally.

The voltage on EN pin must rise above 1.8V to enable the AOZ1025D. When voltage on EN pin falls below 0.6V, the AOZ1025D is disabled.

Steady-State Operation

Under steady-state conditions, the converter operates in fixed frequency and Continuous-Conduction Mode (CCM).

The AOZ1025D integrates an internal P-MOSFET as the high-side switch. Inductor current is sensed by amplifying the voltage drop across the drain to source of the high side power MOSFET. Output voltage is divided down by the external voltage divider at the FB pin. The difference of the FB pin voltage and reference is amplified by the internal transconductance error amplifier. The error voltage, which shows on the COMP pin, is compared against the current signal, which is sum of inductor current signal and ramp compensation signal, at PWM comparator input. If the current signal is less than the error voltage, the internal high-side switch is on. The inductor current flows from the input through the inductor to the output. When the current signal exceeds the error voltage, the high-side switch is off. The inductor current is freewheeling through the external low-side N-MOSFET switch to output. The internal adaptive FET driver guarantees no turn on overlap of both high-side and low-side switch.

The AOZ1025D uses an external freewheeling NMOSFET to realize synchronous rectification. It greatly improves the converter efficiency and reduces power loss in the low-side switch.

The AOZ1025D uses a P-Channel MOSFET as the high-side switch. It saves the bootstrap capacitor normally seen in a circuit which is using an NMOS switch.

Switching Frequency

The AOZ1025D switching frequency is fixed and set by an internal oscillator. The practical switching frequency could range from 350 kHz to 600 kHz due to device variation.

Output Voltage Programming

Output voltage can be set by feeding back the output to the FB pin by using a resistor divider network. In the application circuit shown in Figure 1. The resistor divider network includes R_1 and R_2. Usually, a design is started by picking a fixed R_2 value and calculating the required R_1 with equation:

$$V_O = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Some standard value of R1, R2 and most used output voltage values are listed in Table 1.

Table 1.

V_O (V)	R_1 (kΩ)	R_2 (kΩ)
0.8	1.0	Open
1.2	4.99	10
1.5	10	11.5
1.8	12.7	10.2
2.5	21.5	10
3.3	31.6	10
5.0	52.3	10

The combination of R_1 and R_2 should be large enough to avoid drawing excessive current from the output, which will cause power loss.

Protection Features

The AOZ1025D has multiple protection features to prevent system circuit damage under abnormal conditions.

Over Current Protection (OCP)

The sensed inductor current signal is also used for over current protection. Since the AOZ1025D employs peak current mode control, the COMP pin voltage is proportional to the peak inductor current. The COMP pin voltage is limited to be between 0.4V and 2.5V internally. The peak inductor current is automatically limited cycle by cycle.

When the output is shorted to ground under fault conditions, the inductor current decays very slow during a switching cycle because of V_O = 0V. To prevent catastrophic failure, a secondary current limit is designed inside the AOZ1025D. The measured inductor current is compared against a preset voltage which represents the current limit. When the output current is more than current limit, the high side switch will be turned off and EN pin will be pulled down. The converter will initiate a soft start once the over-current condition disappears.

Output Over Voltage Protection (OVP)

The AOZ1025D monitors the feedback voltage: when the feedback voltage is higher than 960mV, it immediate turns-off the PMOS to protect the output voltage overshoot at fault condition. When feedback voltage is lower than 840mV, the PMOS is allowed to turn on in the next cycle.

Under-voltage Lock-out (UVLO)

A power-on reset circuit monitors the input voltage. When the input voltage exceeds 4V, the converter starts operation. When input voltage falls below 3.7V, the converter will be shut down.

Thermal Protection

An internal temperature sensor monitors the junction temperature. It shuts down the internal control circuit and high side PMOS if the junction temperature exceeds 150°C. The regulator will restart automatically under the control of soft-start circuit when the junction temperature decreases to 100°C.

Power Good

The output of Power-Good is an open drain N-channel MOSFET, which supplies an active high power good stage. A pull-up resistor should connect this pin to a DC power trail with maximum voltage no higher than 6V. The AOZ1025D monitors the FB voltage: when FB pin voltage is lower than 90% of the normal voltage, N-channel MOSFET turns on and the Power-Good pin is pulled low, which indicates the power is abnormal.

Application Information

The basic AOZ1025D application circuit is show in Figure 1. Component selection is explained below.

Input Capacitor

The input capacitor must be connected to the V_{IN} pin and PGND pin of AOZ1025D to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}}\left(1 - \frac{V_O}{V_{IN}}\right)}$$

if we let *m* equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relationship between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 2. It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is 0.5 x I_O.

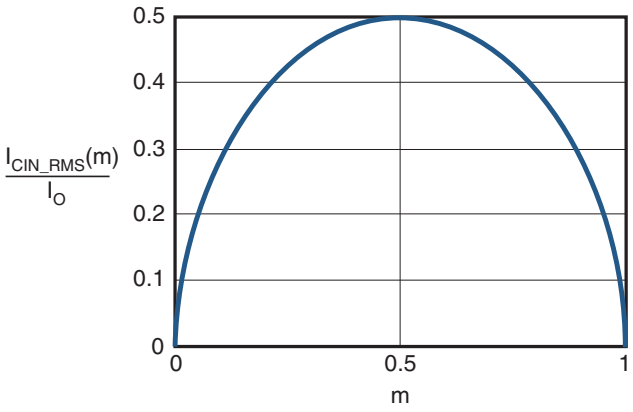


Figure 2. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than I_{CIN_RMS} at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high current rating. Depending on the application circuits, other low ESR tantalum capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors should be used for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures are based on certain amount of life time. Further de-rating may be necessary in practical design.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 20% to 40% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor need to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times \left(ESR_{CO} + \frac{1}{8 \times f \times C_O}\right)$$

where,

C_O is output capacitor value, and

ESR_{CO} is the equivalent series resistance of the output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \frac{1}{8 \times f \times C_O}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

Loop Compensation

The AOZ1025D employs peak current mode control for easy use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole is dominant pole can be calculated by:

$$f_{P1} = \frac{1}{2\pi \times C_O \times R_L}$$

The zero is a ESR zero due to output capacitor and its ESR. It is can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

where;

C_O is the output filter capacitor,

R_L is load resistor value, and

ESR_{CO} is the equivalent series resistance of output capacitor.

The compensation design is actually to shape the converter control loop transfer function to get desired gain and phase. Several different types of compensation network can be used for the AOZ1025D. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In the AOZ1025D, FB pin and COMP pin are the inverting input and the output of internal error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{P2} = \frac{G_{EA}}{2\pi \times C_C \times G_{VEA}}$$

where;

G_{EA} is the error amplifier transconductance, which is 200 x 10^{-6} A/V,

G_{VEA} is the error amplifier voltage gain, which is 500 V/V, and

C_C is the compensation capacitor.

The zero given by the external compensation network, capacitor C_C and resistor R_C, is located at:

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

To design the compensation circuit, a target crossover frequency f_C for close loop must be selected. The system crossover frequency is where control loop has unity gain. The crossover is the also called the converter bandwidth. Generally a higher bandwidth means faster response to load transient. However, the bandwidth should not be too high because of system stability concern. When designing the compensation loop, converter stability under all line and load condition must be considered.

Usually, it is recommended to set the bandwidth to be equal or less than 1/10 of switching frequency. The AOZ1025D operates at a fixed 500kHz switching frequency. It is recommended to choose a crossover frequency equal or less than 40kHz.

$$f_C = 40kHz$$

The strategy for choosing R_C and C_C is to set the cross over frequency with R_C and set the compensator zero with C_C. Using selected crossover frequency, f_C, to calculate R_C:

$$R_C = f_C \times \frac{V_O}{V_{FB}} \times \frac{2\pi \times C_O}{G_{EA} \times G_{CS}}$$

where;

f_C is the desired crossover frequency. For best performance, f_C is set to be about 1/10 of the switching frequency;

V_{FB} is 0.8V,

G_{EA} is the error amplifier transconductance, which is 200 x 10^{-6} A/V, and

G_{CS} is the current sense circuit transconductance, which is 10.8 A/V

The compensation capacitor C_C and resistor R_C together make a zero. This zero is put somewhere close to the dominate pole f_{p1} but lower than 1/5 of selected crossover frequency. C_C can is selected by:

$$C_C = \frac{1.5}{2\pi \times R_C \times f_{P1}}$$

The previous equation can also be simplified to:

$$C_C = \frac{C_O \times R_L}{R_C}$$

Thermal Management and Layout Consideration

In the AOZ1025 buck regulator circuit, the major power dissipating components are the AOZ1025 output inductor, and low-side NMOSFET. The total power dissipation of converter circuit can be measured by input power minus output power:

$$P_{total\_loss} = V_{IN} \times I_{IN} - V_O \times I_O$$

The power dissipation of inductor can be approximately calculated by output current and DCR of inductor:

$$P_{inductor\_loss} = I_O^2 \times R_{inductor} \times 1.1$$

The power dissipation of low-side NMOSFET can be approximately calculated by output current, Rdson, and duty cycle (V_O / V_{IN}).

$$P_{inductor\_loss} = I_O^2 \times R_{inductor} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The actual junction temperature can be calculated with power dissipation in the AOZ1025 and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total\_loss} - P_{inductor\_loss} - P_{nmos\_loss}) \times \Theta_{JA} + T_{amb}$$

The thermal performance of the AOZ1025D is strongly affected by the PCB layout. Extra care should be taken by users during design to ensure that the IC will operate under the recommended environmental conditions.

Several layout tips are listed below for the best electric and thermal performance:

1. Do not use thermal relief connection to the V_{IN} and the PGND pin. Pour a maximized copper area to the PGND pin and the VIN pin to help thermal dissipation.
2. Input capacitor should be connected to the V_{IN} pin and the PGND pin as close as possible.
3. A ground plane is preferred. If a ground plane is not used, separate PGND from AGND and connect them only at one point to avoid the PGND pin noise coupling to the AGND pin.
4. Make the current trace from LX pins to L to Co to the PGND as short as possible.
5. Pour copper plane on all unused board area and connect it to stable DC nodes, like V_{IN}, PGND or SGND.
6. Keep sensitive signal trace away from switching node, LX. The copper pour area connected to the LX pin should be as wide as possible to avoid the switching noise on the LX pin coupling to other part of circuit.

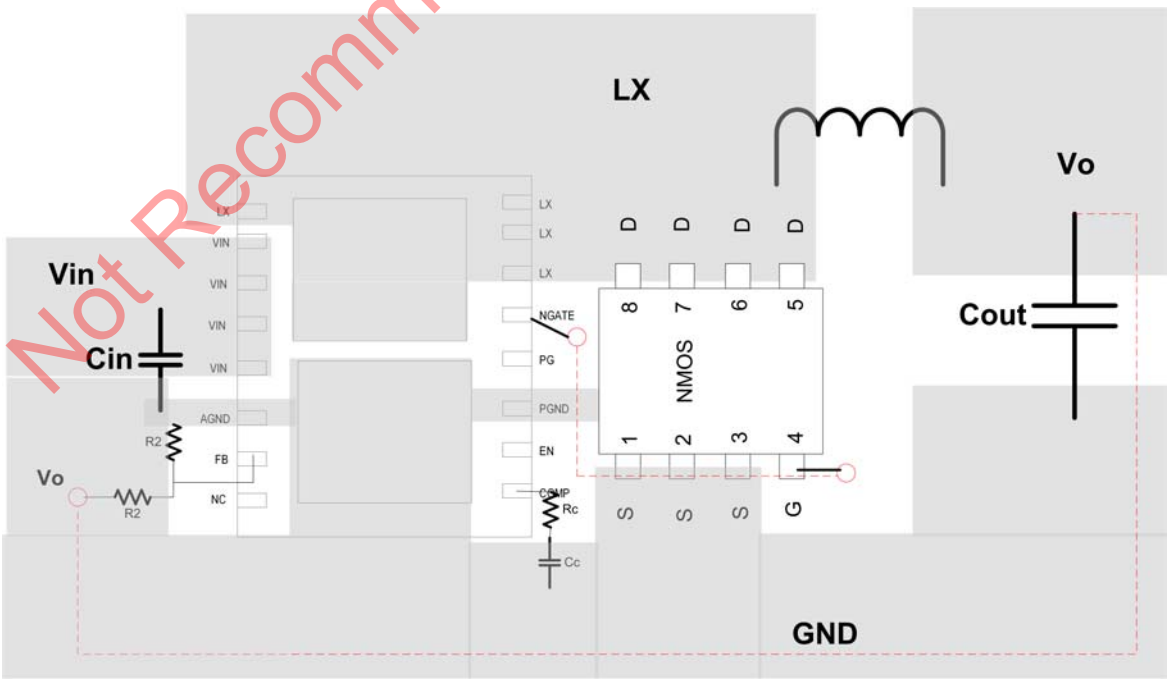
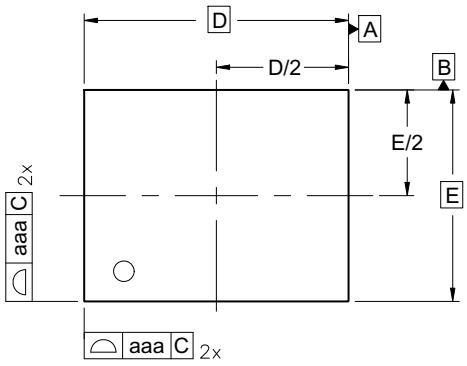
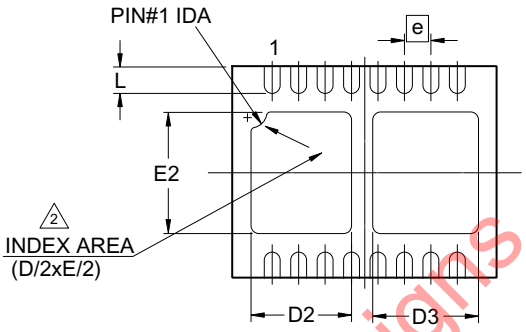
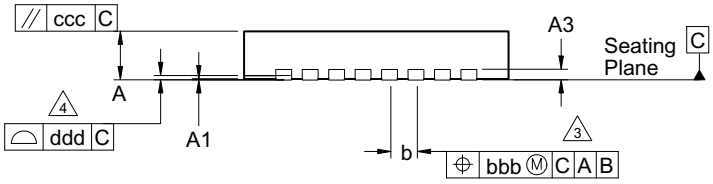


Figure 3. AOZ1025D (DFN 5x4) PCB Layout

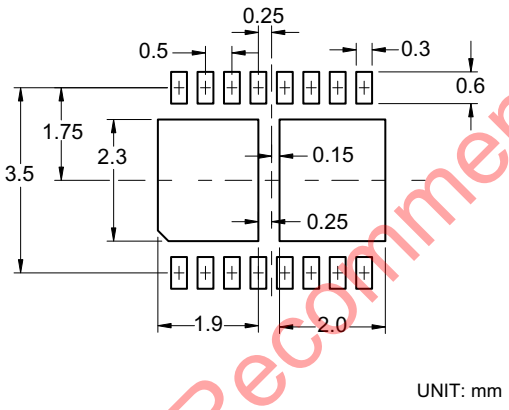
Package Dimensions, DFN-16 5x4







RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.17	0.25	0.35
D		5.00 BSC	
D2	1.75	1.90	2.00
D3	1.85	2.00	2.10
E		4.00 BSC	
E2	2.15	2.30	2.40
e		0.50 BSC	
L	0.40	0.50	0.60
R		0.30 REF	
aaa	–	0.15	–
bbb	–	0.10	–
ccc	–	0.10	–
ddd	–	0.08	–

Dimensions in inches

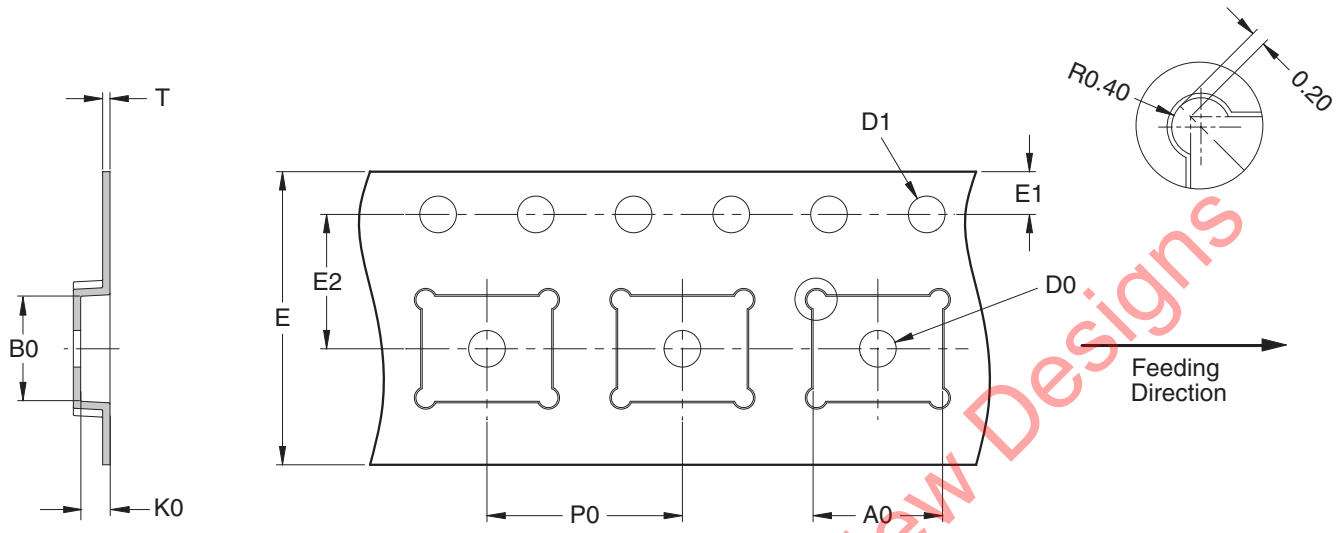
Symbols	Min.	Nom.	Max.
A	0.031	0.035	0.039
A1	0.000	0.001	0.002
A3		0.008 REF	
b	0.007	0.010	0.014
D		0.197 BSC	
D2	0.069	0.075	0.079
D3	0.073	0.079	0.083
E		0.157 BSC	
E2	0.085	0.091	0.094
e		0.020 BSC	
L	0.016	0.020	0.024
R		0.012 REF	
aaa	–	0.006	–
bbb	–	0.004	–
ccc	–	0.004	–
ddd	–	0.003	–

Notes:

1. All dimensions are in millimeters.
2. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SP-002.
3. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
4. Coplanarity applies to the terminals and all other bottom surface metallization.
5. Drawing shown are for illustration only.

Tape Dimensions, DFN-16 5x4

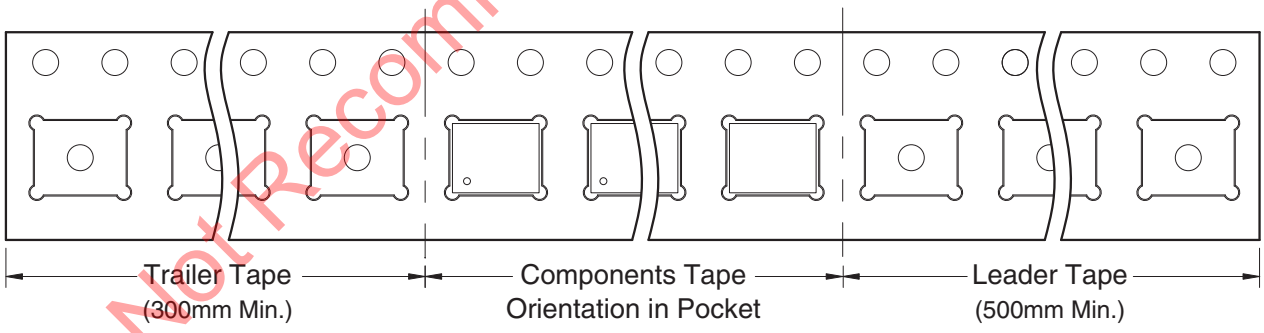
Tape



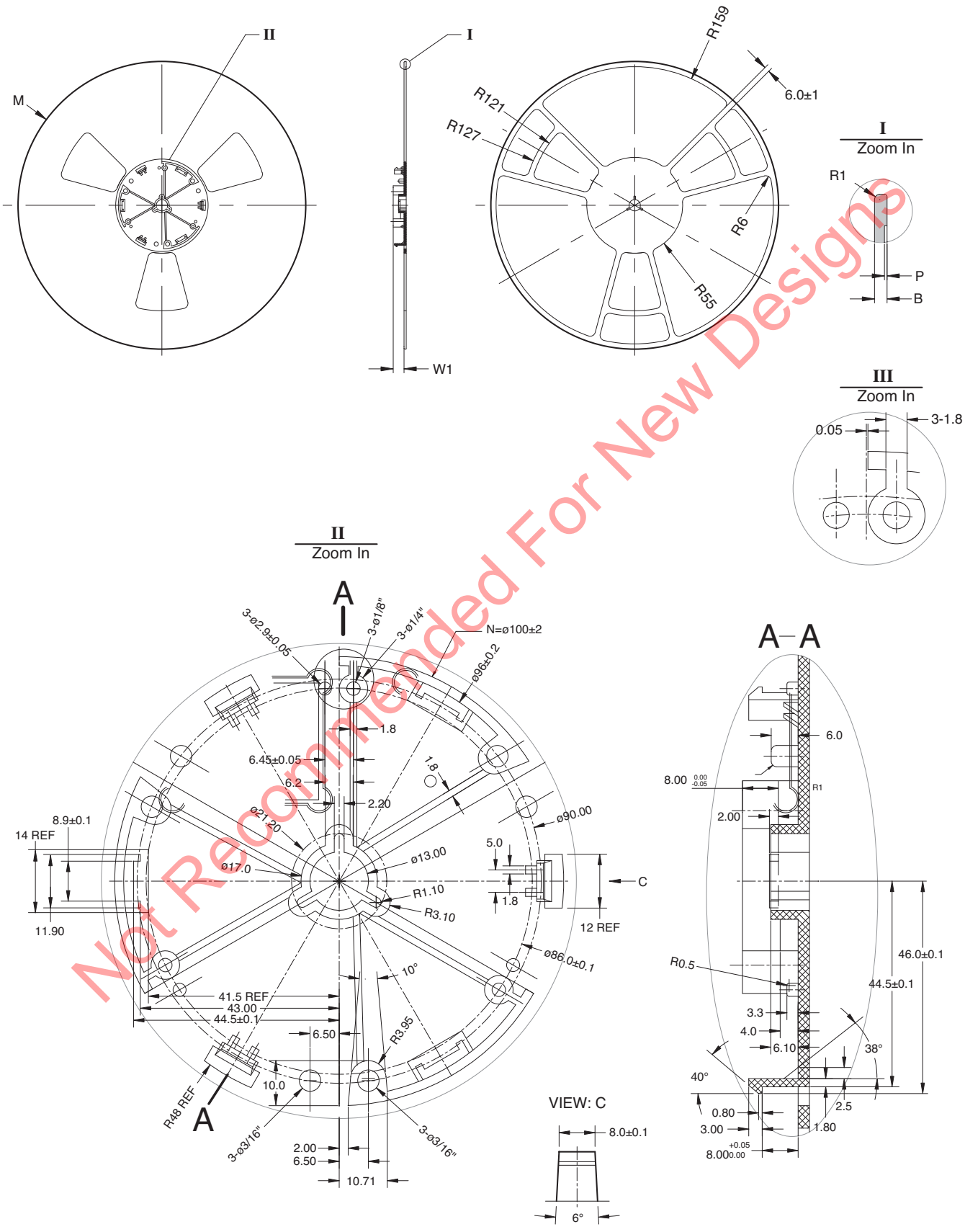
Unit: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN 5x4 (12 mm)	5.30 ±0.10	4.30 ±0.10	1.20 ±0.10	1.50 Min. Typ.	1.50 +0.10 / –0	12.00 ±0.30	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.20	2.00 ±0.10	0.30 ±0.05

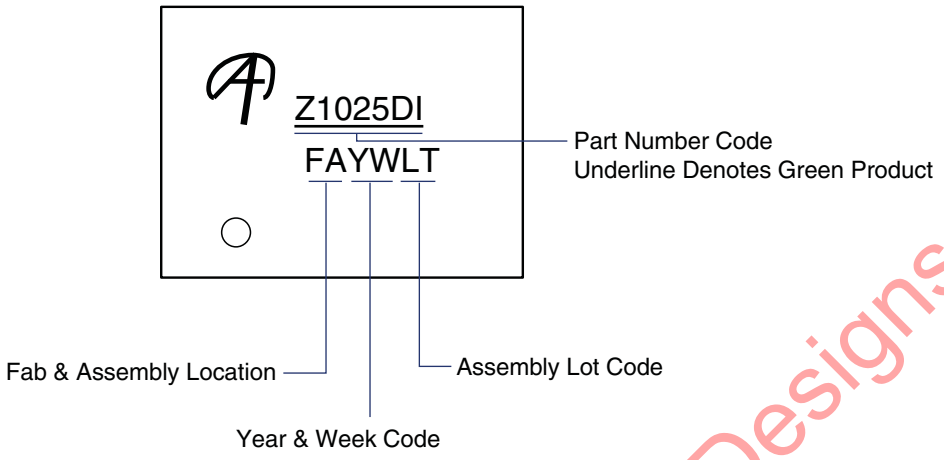
Leader/Trailer and Orientation



Reel Dimensions, DFN-16 5x4



Package Marking



This data sheet contains preliminary data; supplementary data may be published at a later date.
Alpha & Omega Semiconductor reserves the right to make changes at any time without notice.

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.