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10/15—Rev. C to Rev. D

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2/12—Rev. B to Rev. C

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8/10—Rev. 0 to Rev. A

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10/09—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at $T_A = 25°C$, $V_{DD1} = V_{DD2} = 5$ V. Minimum/maximum specifications apply over the entire recommended operation range of $4.5 \text{ V} \leq V_{DD1} \leq 5.5$ V, $4.5 \text{ V} \leq V_{DD2} \leq 5.5$ V, and $-40°C \leq T_A \leq +105°C$, unless otherwise noted. Switching specifications are tested with $C_L = 15$ pF, and CMOS signal levels, unless otherwise noted.

Table 1.

		A Grade			C Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS									
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		50	75	29	40	50	ns	50% input to 50% output
Pulse Width Distortion	PWD		10	25		2	5	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			5			3		ps/°C	
Pulse Width	PW	250			40			ns	Within PWD limit
Propagation Delay Skew[1]	t_{PSK}			20			10	ns	
Channel Matching									
Codirectional	t_{PSKCD}			25		2	4	ns	
Opposing-Direction	t_{PSKOD}			30		3	6	ns	
Jitter			2			2		ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 2.

		1 Mbps—A Grade			25 Mbps—C Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SUPPLY CURRENT									
ADuM7440	I_{DD1}		4.3	5.4		28	35	mA	
	I_{DD2}		2.5	3.6		6.0	11	mA	
ADuM7441	I_{DD1}		4.1	4.9		18	26	mA	
	I_{DD2}		3.6	4.7		8.5	14	mA	
ADuM7442	I_{DD1}		3.2	4.0		15	20	mA	
	I_{DD2}		3.2	4.0		12	17	mA	

Table 3. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	$0.7\ V_{DDx}$			V	
Logic Low Input Threshold	V_{IL}			$0.3\ V_{DDx}$	V	
Logic High Output Voltages	V_{OH}	$V_{DDx} - 0.1$	5.0		V	$I_{Ox} = -20\ \mu A$, $V_{Ix} = V_{IxH}$
		$V_{DDx} - 0.4$	4.8		V	$I_{Ox} = -4$ mA, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	$I_{Ox} = 20\ \mu A$, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	$I_{Ox} = 4$ mA, $V_{Ix} = V_{IxL}$
Input Current per Channel	I_I	−10	+0.01	+10	µA	$0 \text{ V} \leq V_{Ix} \leq V_{DDx}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.76	0.95	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.57	0.73	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.26		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.0		ns	10% to 90%
Common-Mode Transient Immunity[1]	$\lvert CM \rvert$	15	25		kV/µs	$V_{Ix} = V_{DDx}$, $V_{CM} = 1000$ V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	

[1] $\lvert CM \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at T_A = 25°C, $V_{DD1} = V_{DD2}$ = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range of 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V; and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 4.

Parameter	Symbol	A Grade Min	Typ	Max	C Grade Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS									
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		60	85	37	51	66	ns	50% input to 50% output
Pulse Width Distortion	PWD		10	25		2	5	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			5			3		ps/°C	
Pulse Width	PW	250			40			ns	Within PWD limit
Propagation Delay Skew[1]	t_{PSK}			20			10	ns	
Channel Matching									
Codirectional	t_{PSKCD}			25		3	5	ns	
Opposing-Direction	t_{PSKOD}			30		4	7	ns	
Jitter			2			2		ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 5.

Parameter	Symbol	1 Mbps—A, C Grades Min	Typ	Max	25 Mbps—C Grade Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT									
ADuM7440	I_{DD1}		3.0	3.8		20	28	mA	
	I_{DD2}		1.8	2.3		4.0	5.0	mA	
ADuM7441	I_{DD1}		2.8	3.5		14	20	mA	
	I_{DD2}		2.5	3.3		5.5	7.5	mA	
ADuM7442	I_{DD1}		2.2	2.7		10	13	mA	
	I_{DD2}		2.2	2.8		8.4	11	mA	

Table 6. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.2	3.3		V	I_{Ox} = −20 µA, $V_{Ix} = V_{IxH}$
		V_{DDx} − 0.4	3.1		V	I_{Ox} = −4 mA, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	I_{Ox} = 4 mA, $V_{Ix} = V_{IxL}$
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.50		mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.41		mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.18		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.02		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.8		ns	10% to 90%
Common-Mode Transient Immunity[1]	$\lvert CM \rvert$	15	20		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	

[1] $\lvert CM \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V OPERATION

All typical specifications are at $T_A = 25°C$, $V_{DD1} = 5$ V, $V_{DD2} = 3.3$ V. Minimum/maximum specifications apply over the entire recommended operation range of $4.5 \text{ V} \leq V_{DD1} \leq 5.5$ V, $3.0 \text{ V} \leq V_{DD2} \leq 3.6$ V; and $-40°C \leq T_A \leq +105°C$, unless otherwise noted. Switching specifications are tested with $C_L = 15$ pF and CMOS signal levels, unless otherwise noted.

Table 7.

Parameter	Symbol	A Grade Min	A Grade Typ	A Grade Max	C Grade Min	C Grade Typ	C Grade Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS									
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		55	80	30	42	55	ns	50% input to 50% output
Pulse Width Distortion	PWD		10	25		2	5	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			5			3		ps/°C	
Pulse Width	PW	250			40			ns	Within PWD limit
Propagation Delay Skew[1]	t_{PSK}			20			10	ns	
Channel Matching									
Codirectional	t_{PSKCD}			25		2	5	ns	
Opposing-Direction	t_{PSKOD}			30		3	6	ns	
Jitter			2			2		ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 8.

Parameter	Symbol	1 Mbps—A, C Grades Min	1 Mbps—A, C Grades Typ	1 Mbps—A, C Grades Max	25 Mbps—C Grade Min	25 Mbps—C Grade Typ	25 Mbps—C Grade Max	Unit	Test Conditions/Comments
SUPPLY CURRENT									
ADuM7440	I_{DD1}		4.4	5.5		28	35	mA	
	I_{DD2}		1.6	2.1		3.5	4.5	mA	
ADuM7441	I_{DD1}		3.7	5.0		19	27	mA	
	I_{DD2}		2.2	2.8		5.2	7.0	mA	
ADuM7442	I_{DD1}		3.2	3.9		15	20	mA	
	I_{DD2}		2.0	2.6		7.8	12	mA	

Table 9. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	$0.7 V_{DDx}$			V	
Logic Low Input Threshold	V_{IL}			$0.3 V_{DDx}$	V	
Logic High Output Voltages	V_{OH}	$V_{DDx} - 0.1$	V_{DDx}		V	$I_{Ox} = -20$ µA, $V_{Ix} = V_{IxH}$
		$V_{DDx} - 0.4$	$V_{DDx} - 0.2$		V	$I_{Ox} = -4$ mA, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	$I_{Ox} = 20$ µA, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	$I_{Ox} = 4$ mA, $V_{Ix} = V_{IxL}$
Input Current per Channel	I_I	−10	+0.01	+10	µA	$0 \text{ V} \leq V_{Ix} \leq V_{DDx}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.77		mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.40		mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.26		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.02		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	$\lvert CM \rvert$	15	20		kV/µs	$V_{Ix} = V_{DDx}$, $V_{CM} = 1000$ V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	

[1] $\lvert CM \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V, V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range of 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 10.

		A Grade			C Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS									
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		55	80	31	46	60	ns	50% input to 50% output
Pulse Width Distortion	PWD		10	25		2	5	ns	$\lvert t_{PLH} - t_{PHL}\rvert$
Change vs. Temperature			5			3		ps/°C	
Pulse Width	PW	250			40			ns	Within PWD limit
Propagation Delay Skew[1]	t_{PSK}			20			10	ns	
Channel Matching									
Codirectional	t_{PSKCD}			25		2	5	ns	
Opposing-Direction	t_{PSKOD}			30		3	7	ns	
Jitter			2			2		ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 11.

		1 Mbps—A, C Grades			25 Mbps—C Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SUPPLY CURRENT									
ADuM7440	I_{DD1}		2.7	3.3		18	24	mA	
	I_{DD2}		2.5	3.3		5.7	8.0	mA	
ADuM7441	I_{DD1}		2.5	3.3		12	20	mA	
	I_{DD2}		3.6	4.6		8.0	11	mA	
ADuM7442	I_{DD1}		2.0	2.4		8.9	13	mA	
	I_{DD2}		3.2	4.0		12	15	mA	

Table 12. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.50	0.60	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.61	0.73	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.17		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	15	20		kV/μs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 13.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	$θ_{JA}$		76		°C/W	Thermocouple located at center of package underside

[1] The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together and Pin 9 through Pin 16 are shorted together.

[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM7440/ADuM7441/ADuM7442 are approved by the organization listed in Table 14. See Table 18 and the Insulation Lifetime section for recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 14.

UL
Recognized under UL 1577 Component Recognition Program[1]
Single Protection, 1000 V rms Isolation Voltage
File E214100

[1] In accordance with UL 1577, each ADuM7440/ADuM7441/ADuM7442 is proof tested by applying an insulation test voltage ≥1200 V rms for 1 sec (current leakage detection limit = 5 μA).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 15.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		1000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	3.8	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	2.8	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		2.6	μm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

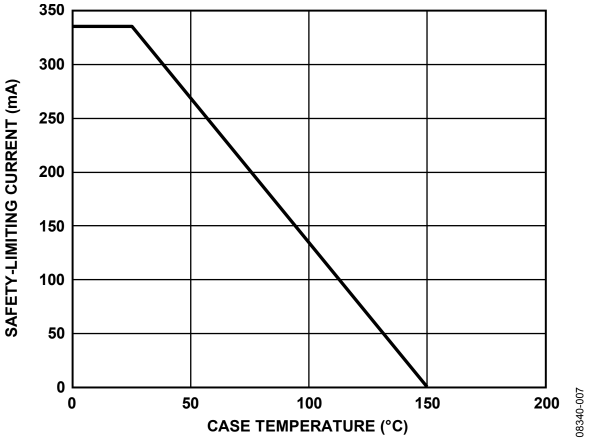


Figure 4. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 16.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	3.0	5.5	V
Input Signal Rise and Fall Times			1.0	ms

[1] All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 17.

Parameter	Rating
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +105°C
Supply Voltages (V_{DD1}, V_{DD2})	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB}, V_{IC}, V_{ID})[1, 2]	−0.5 V to V_{DDI} + 0.5 V
Output Voltages (V_{OA}, V_{OB}, V_{OC}, V_{OD})[1, 2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[3]	
Side 1 (I_{O1})	−10 mA to +10 mA
Side 2 (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[3]	−100 kV/µs to +100 kV/µs

[1] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the Printed Circuit Board (PCB) Layout section.

[2] See Figure 4 for maximum rated current values for various temperatures.

[3] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 18. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	420	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Basic Insulation	420	V peak	50-year minimum lifetime
DC Voltage			
Basic Insulation	420	V peak	50-year minimum lifetime

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

Table 19. Truth Table (Positive Logic)

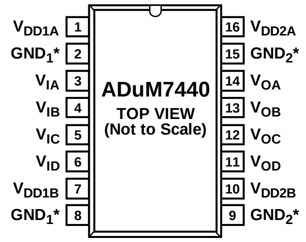
V_{Ix} Input[1]	V_{DDI} State[2]	V_{DDO} State[3]	V_{Ox} Output[1]	Description
H	Powered	Powered	H	Normal operation; data is high.
L	Powered	Powered	L	Normal operation; data is low.
X	Unpowered	Powered	H	Input unpowered. Outputs are in the default high state. Outputs return to input state within 1 µs of V_{DDI} power restoration. See the pin function descriptions (Table 20 through Table 22) for more details.
X	Powered	Unpowered	Z	Output unpowered. Output pins are in high impedance state. Outputs return to input state within 1 µs of V_{DDO} power restoration. See the pin function descriptions (Table 20 through Table 22) for more details.

[1] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, or D).

[2] V_{DDI} refers to the power supply on the input side of a given channel (A, B, C, or D).

[3] V_{DDO} refers to the power supply on the output side of a given channel (A, B, C, or D).

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

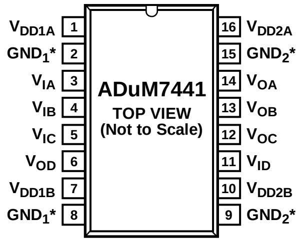


*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO GND$_1$ IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO GND$_2$ IS RECOMMENDED.

Figure 5. ADuM7440 Pin Configuration

Table 20. ADuM7440 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1A}	Supply Voltage A for Isolator Side 1 (3.0 V to 5.5 V). Pin 1 must be connected externally to Pin 7. Connect a ceramic bypass capacitor of value 0.01 µF to 0.1 µF between V_{DD1A} (Pin 1) and GND$_1$ (Pin 2).
2	GND$_1$	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND$_1$ is recommended.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{ID}	Logic Input D.
7	V_{DD1B}	Supply Voltage B for Isolator Side 1 (3.0 V to 5.5 V). Pin 7 must be connected externally to Pin 1. Connect a ceramic bypass capacitor of value 0.01 µF to 0.1 µF between V_{DD1B} (Pin 7) and GND$_1$ (Pin 8).
8	GND$_1$	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND$_1$ is recommended.
9	GND$_2$	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND$_2$ is recommended.
10	V_{DD2B}	Supply Voltage B for Isolator Side 2 (3.0 V to 5.5 V). Pin 10 must be connected externally to Pin 16. Connect a ceramic bypass capacitor of value 0.01 µF to 0.1 µF between V_{DD2B} (Pin 10) and GND$_2$ (Pin 9).
11	V_{OD}	Logic Output D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND$_2$	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND$_2$ is recommended.
16	V_{DD2A}	Supply Voltage A for Isolator Side 2 (3.0 V to 5.5 V). Pin 16 must be connected externally to Pin 10. Connect a ceramic bypass capacitor of value 0.01 µF to 0.1 µF between V_{DD2A} (Pin 16) and GND$_2$ (Pin 15).

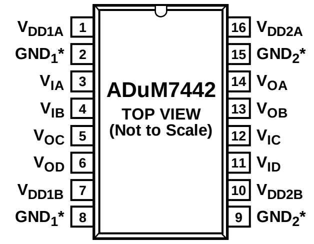


*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO GND_1 IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO GND_2 IS RECOMMENDED.

Figure 6. ADuM7441 Pin Configuration

Table 21. ADuM7441 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1A}	Supply Voltage A for Isolator Side 1 (3.0 V to 5.5 V). Pin 1 must be connected externally to Pin 7. Connect a ceramic bypass capacitor of value 0.01 µF to 0.1 µF between V_{DD1A} (Pin 1) and GND_1 (Pin 2).
2	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND_1 is recommended.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{OD}	Logic Output D.
7	V_{DD1B}	Supply Voltage B for Isolator Side 1 (3.0 V to 5.5 V). Pin 7 must be connected externally to Pin 1. Connect a ceramic bypass capacitor of value 0.01 µF to 0.1 µF between V_{DD1B} (Pin 7) and GND_1 (Pin 8).
8	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND_1 is recommended.
9	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND_2 is recommended.
10	V_{DD2B}	Supply Voltage B for Isolator Side 2 (3.0 V to 5.5 V). Pin 10 must be connected externally to Pin 16. Connect a ceramic bypass capacitor of value 0.01 µF to 0.1 µF between V_{DD2B} (Pin 10) and GND_2 (Pin 9).
11	V_{ID}	Logic Input D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND_2 is recommended.
16	V_{DD2A}	Supply Voltage A for Isolator Side 2 (3.0 V to 5.5 V). Pin 16 must be connected externally to Pin 10. Connect a ceramic bypass capacitor of value 0.01 µF to 0.1 µF between V_{DD2A} (Pin 16) and GND_2 (Pin 15).



*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO GND_1 IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO GND_2 IS RECOMMENDED.

Figure 7. ADuM7442 Pin Configuration

Table 22. ADuM7442 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1A}	Supply Voltage A for Isolator Side 1 (3.0 V to 5.5 V). Pin 1 must be connected externally to Pin 7. Connect a ceramic bypass capacitor of value 0.01 µF to 0.1 µF between V_{DD1A} (Pin 1) and GND_1 (Pin 2).
2	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND_1 is recommended.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{OC}	Logic Output C.
6	V_{OD}	Logic Output D.
7	V_{DD1B}	Supply Voltage B for Isolator Side 1 (3.0 V to 5.5 V). Pin 7 must be connected externally to Pin 1. Connect a ceramic bypass capacitor of value 0.01 µF to 0.1 µF between V_{DD1B} (Pin 7) and GND_1 (Pin 8).
8	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND_1 is recommended.
9	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND_2 is recommended.
10	V_{DD2B}	Supply Voltage B for Isolator Side 2 (3.0 V to 5.5 V). Pin 10 must be connected externally to Pin 16. Connect a ceramic bypass capacitor of value 0.01 µF to 0.1 µF between V_{DD2B} (Pin 10) and GND_2 (Pin 9).
11	V_{ID}	Logic Input D.
12	V_{IC}	Logic Input C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND_2 is recommended.
16	V_{DD2A}	Supply Voltage A for Isolator Side 2 (3.0 V to 5.5 V). Pin 16 must be connected externally to Pin 10. Connect a ceramic bypass capacitor of value 0.01 µF to 0.1 µF between V_{DD2A} (Pin 16) and GND_2 (Pin 15).

TYPICAL PERFORMANCE CHARACTERISTICS

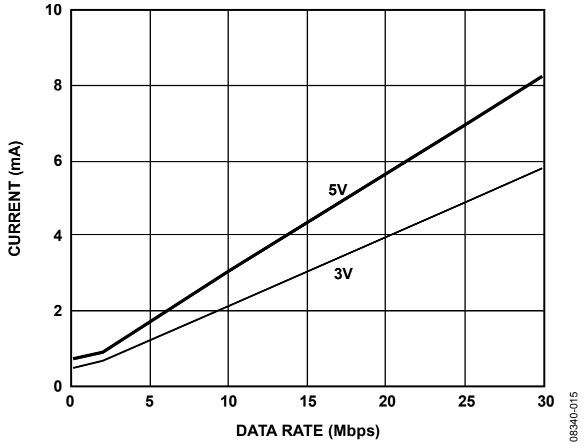


Figure 8. Typical Supply Current per Input Channel vs. Data Rate for 5 V and 3 V Operation

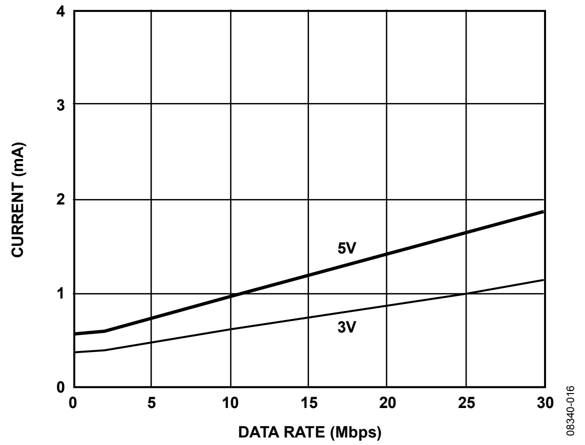


Figure 9. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

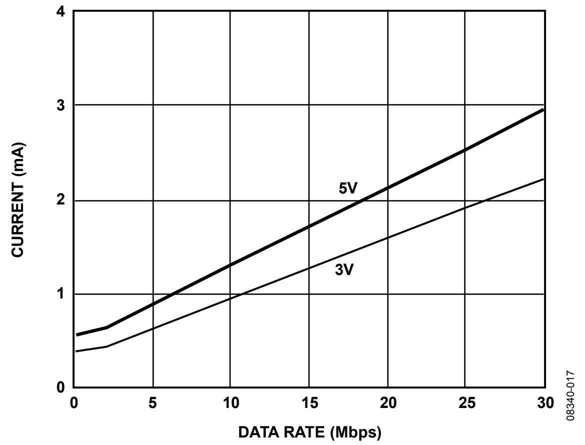


Figure 10. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

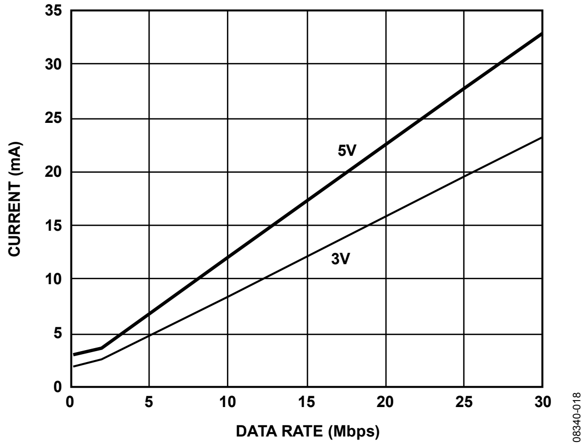


Figure 11. Typical ADuM7440 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

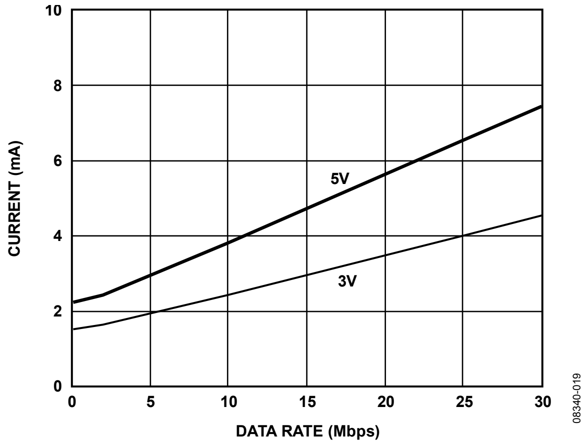


Figure 12. Typical ADuM7440 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

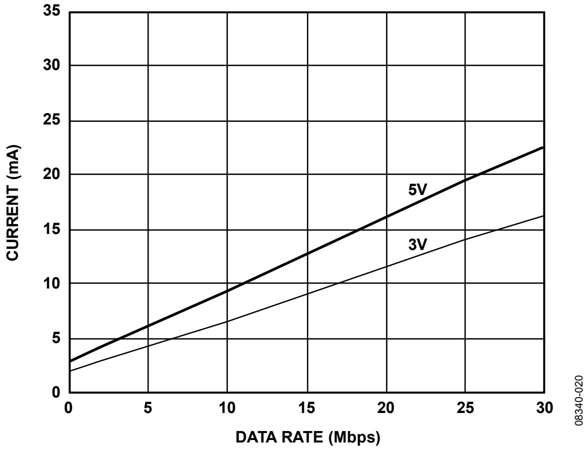


Figure 13. Typical ADuM7441 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

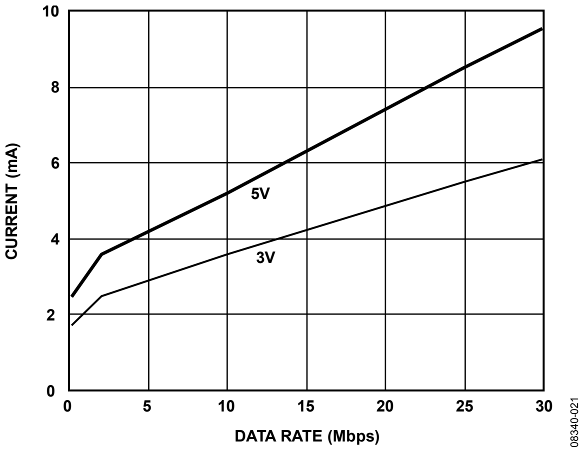


Figure 14. Typical ADuM7441 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

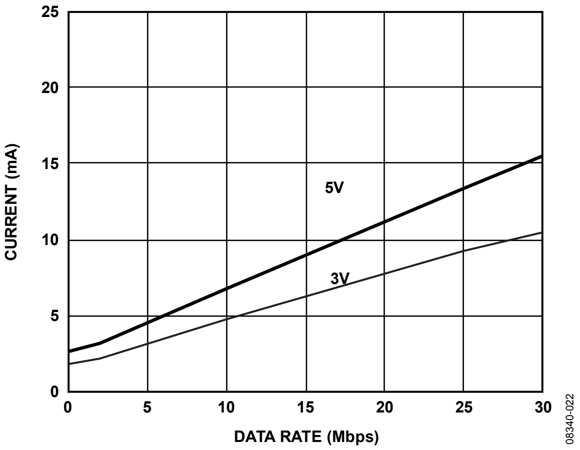


Figure 15. Typical ADuM7442 V_{DD1} or V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

APPLICATIONS INFORMATION

PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADuM7440/ADuM7441/ADuM7442 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 16). A total of four bypass capacitors should be connected between Pin 1 and Pin 2 for V_{DD1A}, between Pin 7 and Pin 8 for V_{DD1B}, between Pin 9 and Pin 10 for V_{DD2B}, and between Pin 15 and Pin 16 for V_{DD2A}. Supply V_{DD1A} Pin 1 and V_{DD1B} Pin 7 should be connected together and supply V_{DD2B} Pin 10 and V_{DD2A} Pin 16 should be connected together. The capacitor values should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the power supply pin should not exceed 20 mm.

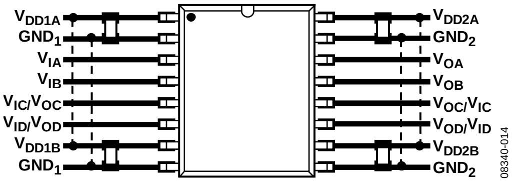


Figure 16. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, it is important to minimize board coupling across the isolation barrier. Furthermore, users should design the board layout so that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

See the AN-1109 Application Note for board layout guidelines.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The input-to-output propagation delay time for a high-to-low transition may differ from the propagation delay time of a low-to-high transition.

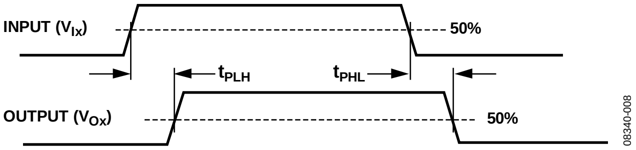


Figure 17. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM7440/ADuM7441/ADuM7442 component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM7440/ADuM7441/ADuM7442 components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder using the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 µs, a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than approximately 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default high state by the watchdog timer circuit.

The magnetic field immunity of the ADuM7440/ADuM7441/ADuM7442 is determined by the changing magnetic field, which induces a voltage in the transformer's receiving coil large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM7440/ADuM7441/ADuM7442 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta / dt) \sum \pi r_n^2; \ n = 1, 2, \ldots , N$$

where:

β is magnetic flux density (gauss).
r_n is the radius of the n^{th} turn in the receiving coil (cm).
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM7440/ADuM7441/ADuM7442 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field at a given frequency can be calculated. The result is shown in Figure 18.

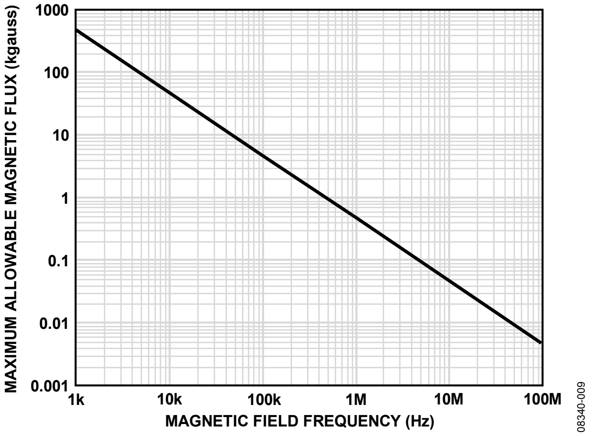


Figure 18. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.5 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurred during a transmitted pulse (and was of the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM7440/ADuM7441/ADuM7442 transformers. Figure 19 shows these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM7440/ ADuM7441/ADuM7442 are extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted previously, a 1.2 kA current would have to be placed 5 mm away from the ADuM7440/ADuM7441/ADuM7442 to affect the operation of the component.

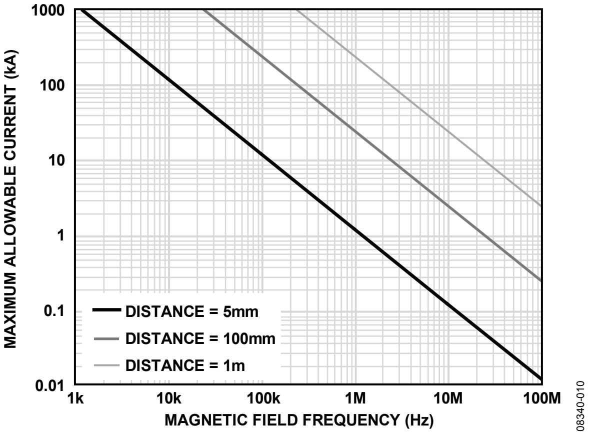


Figure 19. Maximum Allowable Current for Various Current-to-ADuM7440/ADuM7441/ADuM7442 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces can induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Take care in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM7440/ ADuM7441/ADuM7442 isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \qquad f \le 0.5\,f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \qquad f > 0.5\,f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO\,(Q)} \qquad f \le 0.5\,f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \qquad f > 0.5\,f_r$$

where:

$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

C_L is the output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

f is the input logic signal frequency (MHz); it is half the input data rate, expressed in Mbps.

f_r is the input stage refresh rate (Mbps).

$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total V_{DD1} and V_{DD2} supply current, the supply currents for each input and output channel corresponding to V_{DD1} and V_{DD2} are calculated and totaled. Figure 8 and Figure 9 show per-channel supply currents as a function of data rate for an unloaded output condition. Figure 10 shows the per-channel supply current as a function of data rate for a 15 pF output condition. Figure 11 through Figure 15 show the total V_{DD1} and V_{DD2} supply current as a function of data rate for ADuM7440/ ADuM7441/ADuM7442 channel configurations.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM7440/ ADuM7441/ADuM7442.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 18 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA approved working voltages. In many cases, the approved working voltage is higher than 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM7440/ADuM7441/ADuM7442 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 20, Figure 21, and Figure 22 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 18 can be applied while maintaining the 50-year minimum lifetime provided the voltage conforms to either the unipolar ac or dc voltage case. Any cross-insulation voltage waveform that does not conform to Figure 21 or Figure 22 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 18.

Note that the voltage presented in Figure 21 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

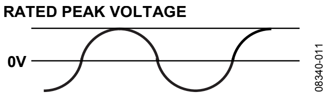


Figure 20. Bipolar AC Waveform

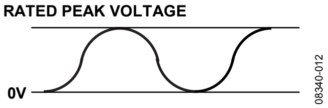


Figure 21. Unipolar AC Waveform

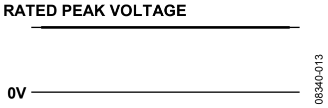
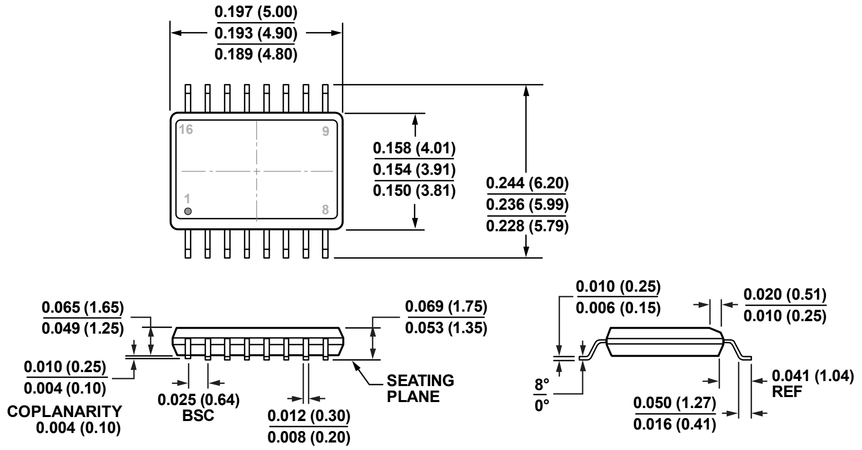


Figure 22. DC Waveform

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137-AB

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

09-12-2014-A

Figure 23. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	**Number of Inputs, V_{DD1} Side**	**Number of Inputs, V_{DD2} Side**	**Maximum Data Rate (Mbps)**	**Maximum Propagation Delay, 5 V (ns)**	**Maximum Pulse Width Distortion (ns)**	**Temperature Range**	**Package Description**	**Package Option**
ADuM7440ARQZ	4	0	1	75	25	−40°C to +105°C	16-Lead QSOP	RQ-16
ADuM7440ARQZ-RL7	4	0	1	75	25	−40°C to +105°C	16-Lead QSOP, 7″ Tape and Reel	RQ-16
ADuM7440CRQZ	4	0	25	50	5	−40°C to +105°C	16-Lead QSOP	RQ-16
ADuM7440CRQZ-RL7	4	0	25	50	5	−40°C to +105°C	16-Lead QSOP, 7″ Tape and Reel	RQ-16
ADuM7441ARQZ	3	1	1	75	25	−40°C to +105°C	16-Lead QSOP	RQ-16
ADuM7441ARQZ-RL7	3	1	1	75	25	−40°C to +105°C	16-Lead QSOP, 7″ Tape and Reel	RQ-16
ADuM7441CRQZ	3	1	25	50	5	−40°C to +105°C	16-Lead QSOP	RQ-16
ADuM7441CRQZ-RL7	3	1	25	50	5	−40°C to +105°C	16-Lead QSOP, 7″ Tape and Reel	RQ-16
ADuM7442ARQZ	2	2	1	75	25	−40°C to +105°C	16-Lead QSOP	RQ-16
ADuM7442ARQZ-RL7	2	2	1	75	25	−40°C to +105°C	16-Lead QSOP, 7″ Tape and Reel	RQ-16
ADuM7442CRQZ	2	2	25	50	5	−40°C to +105°C	16-Lead QSOP	RQ-16
ADuM7442CRQZ-RL7	2	2	25	50	5	−40°C to +105°C	16-Lead QSOP, 7″ Tape and Reel	RQ-16

[1] Z = RoHS Compliant Part.

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www.analog.com