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REVISION HISTORY

2/14—Rev. E to Rev. F

Updated Format ... Universal
Deleted 20-Terminal LCC and 12-Pin TO-8 ... Universal
Changed NC Pin to NIC Pin Throughout ... 1
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3/00—Rev. D to Rev. E

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—±15 V OPERATION

T_A = 25°C, unless otherwise specified. All minimum and maximum specifications are guaranteed. Specifications shown in **boldface** are tested on all production units.

Table 1.

Parameter	Test Conditions/ Comments	AD842JN/AD842JQ/AD842JR[1]			AD842KN/AD842KQ			AD842SQ			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[2]			0.5	**1.5**		0.3	**1.0**		0.5	**1.5**	mV
	T_{MIN} to T_{MAX}			2.5/2.5/3			**1.5**			3.5	mV
Offset Drift			14			14			14		µV/°C
INPUT BIAS CURRENT			4.2	**8**		3.5	**5**		4.2	**8**	µA
	T_{MIN} to T_{MAX}			10			**6**			**12**	µA
Input Offset Current			0.1	**0.4**		0.05	**0.2**		0.1	**0.4**	µA
	T_{MIN} to T_{MAX}			0.5			**0.3**			**0.6**	µA
INPUT CHARACTERISTICS	Differential mode										
Input Resistance			100			100			100		kΩ
Input Capacitance			2.0			2.0			2.0		pF
INPUT VOLTAGE RANGE											
Common Mode		**±10**			**±10**			**±10**			V
Common-Mode Rejection	V_{CM} = ±10 V	**86**	115		**90**	115		**86**	115		dB
	T_{MIN} to T_{MAX}	80			**86**			**80**			dB
INPUT VOLTAGE NOISE	f = 1 kHz		9			9			9		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		28			28			28		µV rms
OPEN-LOOP GAIN	V_{OUT} = ±10 V										
	R_{LOAD} ≥ 499 Ω	**40/40/30**	90		**50**	90		**40**	90		V/mV
	T_{MIN} to T_{MAX}	**20/20/15**			**25**			**20**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 499 Ω	**±10**			**±10**			**±10**			V
Current	V_{OUT} = ±10 V	**100**			**100**			**100**			mA
	Open loop		5			5			5		Ω
FREQUENCY RESPONSE											
Gain Bandwidth Product	V_{OUT} = 90 mV, A_{VCL} = 2		80			80			80		MHz
Full Power Bandwidth[3]	V_{OUT} = 20 V p-p, R_{LOAD} ≥ 499 Ω	4.7	6		4.7	6		4.7	6		MHz
Rise Time	A_{VCL} = −2		10			10			10		ns
Overshoot	A_{VCL} = −2		20			20			20		%
Slew Rate	A_{VCL} = −2	300	375		300	375		300	375		V/µs
Settling Time[4]	10 V step										
	To 0.1%		80			80			80		ns
	To 0.01%		100			100			100		ns
Differential Gain	f = 4.4 MHz		0.015			0.015			0.015		%
Differential Phase	f = 4.4 MHz		0.035			0.035			0.035		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current			13/13/14	**14/14/16**		13	**14**		13	**14**	mA
	T_{MIN} to T_{MAX}			16/16/19.5			**16**			**19**	mA
Power Supply Rejection Ratio	$\pm V_S$ = ±5 V to ±18 V	**86**	100		**90**	105		**86**	100		dB
	T_{MIN} to T_{MAX}	80			**86**			**80**			dB

[1] AD842JR specifications differ from those of the AD842JN and AD842JQ due to the thermal characteristics of the SOIC package.
[2] Input offset voltage specifications are guaranteed after 5 minutes at T_A = 25°C.
[3] Full power bandwidth = slew rate/2 π V peak.
[4] Refer to Figure 29 and Figure 30.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation[1]	
PDIP (N-14), SOIC_W (RW-16)	1.3 W
CERDIP (Q-14)	1.1 W
Input Voltage	$\pm V_S$
Differential Input Voltage	±6 V
Operating Temperature Range	
CERDIP (Q-14, AD842SQ Only)	−55°C to +125°C
PDIP (N-14), SOIC_W (RW-16), CERDIP (Q-14, AD842JQ and AD842KQ Only)	0°C to 70°C
Storage Temperature Range	
CERDIP (Q-14, All Models)	−65°C to +150°C
PDIP (N-14), SOIC_W (RW-16)	−65°C to +125°C
Junction Temperature	175°C
Lead Temperature (Soldering 60 sec)	300°C

[1] Maximum internal power dissipation is specified so that T_J does not exceed 150°C at an ambient temperature of 25°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Table 3.

Package	θ_{JC}	θ_{JA}	θ_{SA}	Unit
14-Lead PDIP	30	100		°C/W
14-Lead CERDIP	30	110	38	°C/W
16-Lead SOIC_W	30	100		°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

METALIZATION PHOTOGRAPH

Figure 3. Contact Factory for Latest Dimensions, Dimensions Shown in Inches and (Millimeters)

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C and V_S = ±15 V, unless otherwise noted.

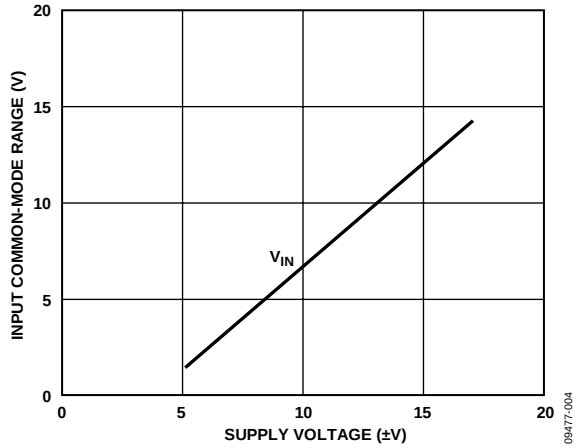


Figure 4. Input Common-Mode Range vs. Supply Voltage

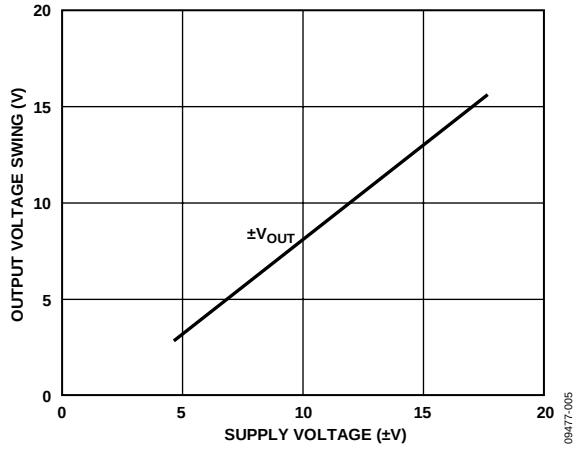


Figure 5. Output Voltage Swing vs. Supply Voltage

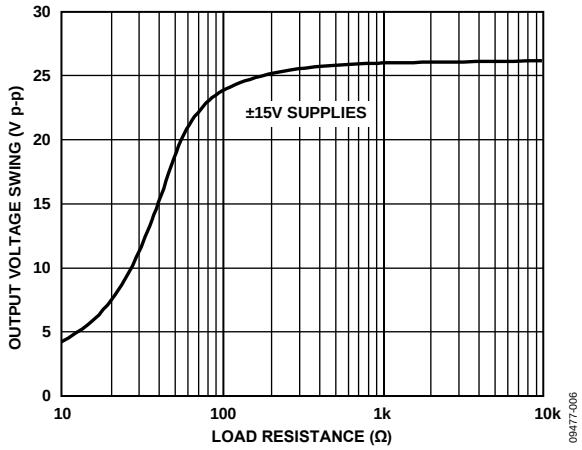


Figure 6. Output Voltage Swing vs. Load Resistance

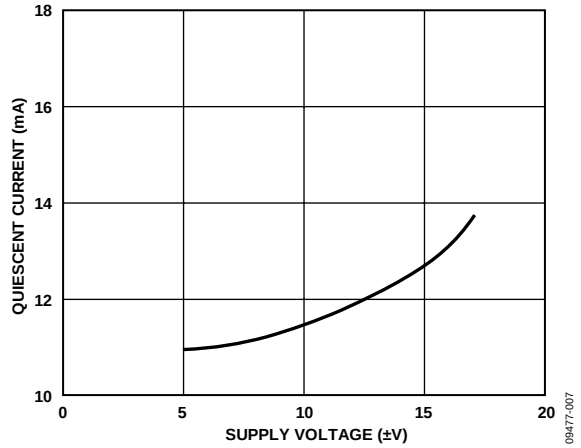


Figure 7. Quiescent Current vs. Supply Voltage

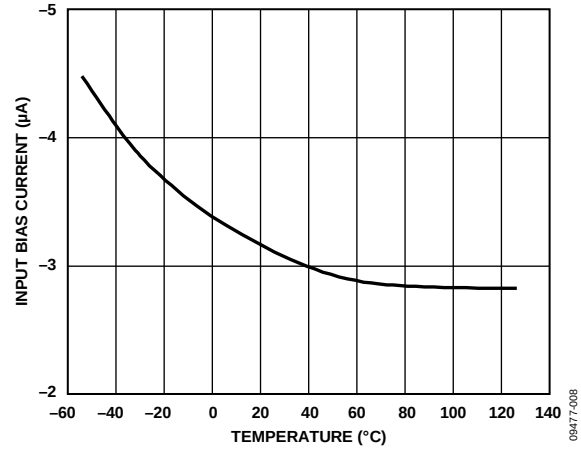


Figure 8. Input Bias Current vs. Temperature

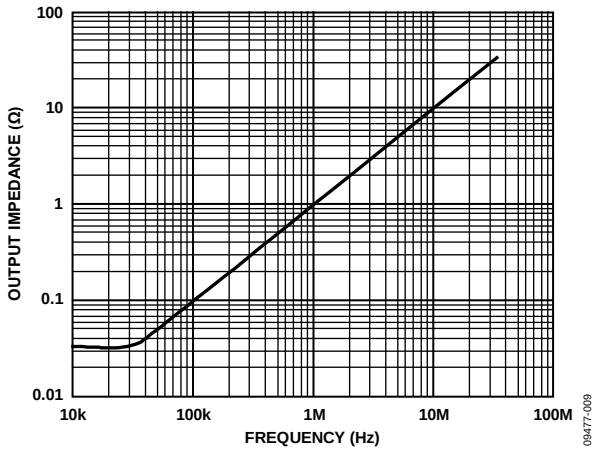


Figure 9. Output Impedance vs. Frequency

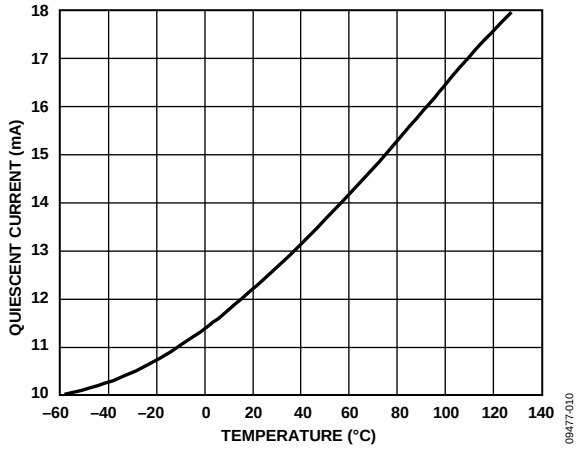


Figure 10. Quiescent Current vs. Temperature

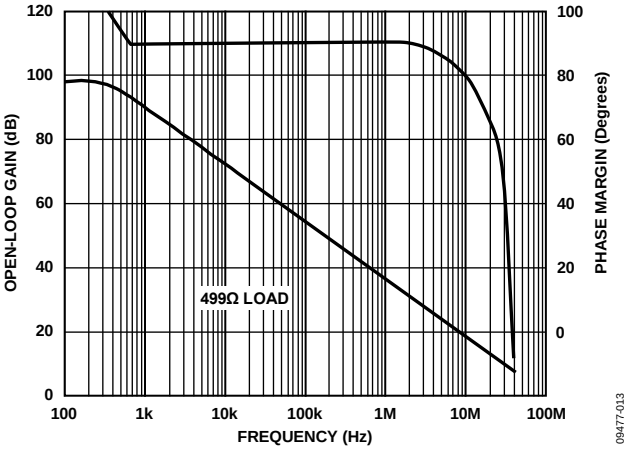


Figure 13. Open-Loop Gain and Phase Margin vs. Frequency

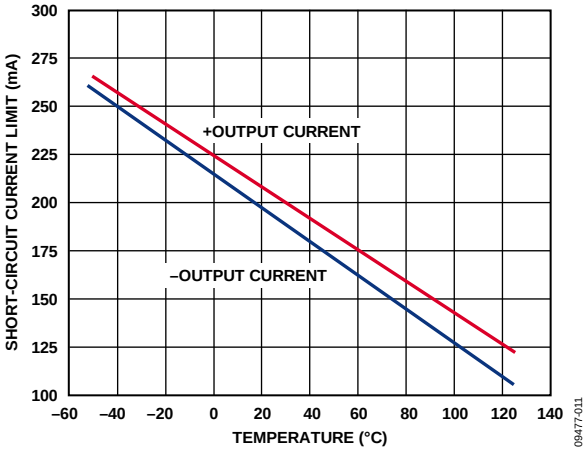


Figure 11. Short-Circuit Current Limit vs. Temperature

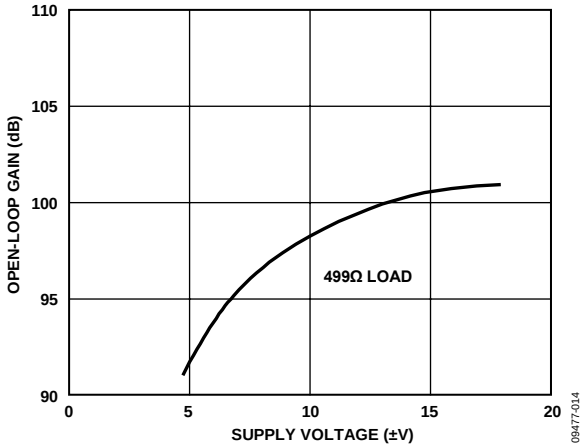


Figure 14. Open-Loop Gain vs. Supply Voltage

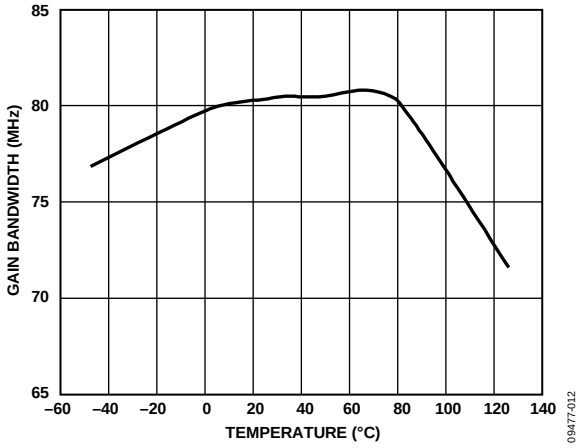


Figure 12. Gain Bandwidth Product vs. Temperature

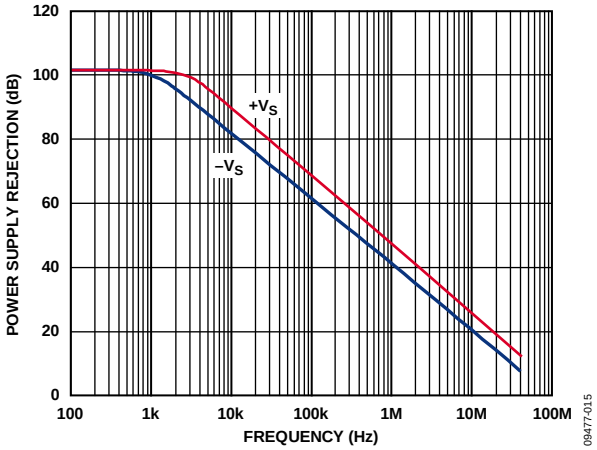


Figure 15. Power Supply Rejection vs. Frequency

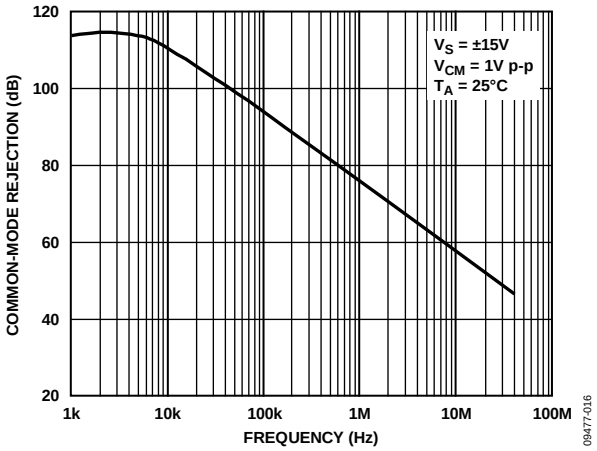


Figure 16. Common-Mode Rejection vs. Frequency

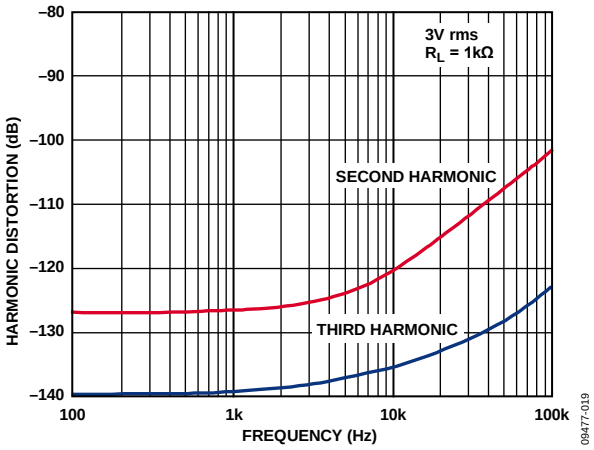


Figure 19. Harmonic Distortion vs. Frequency

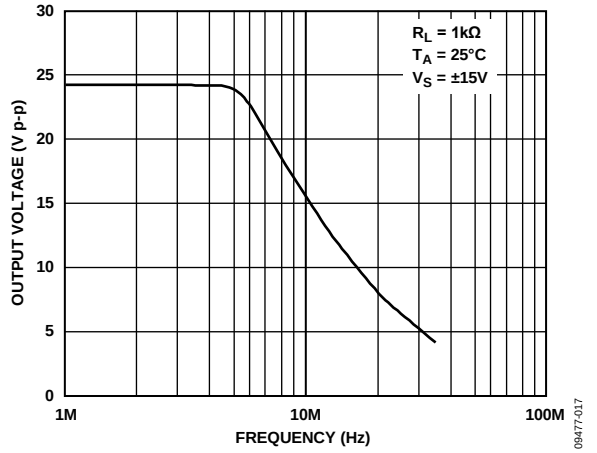


Figure 17. Large Signal Frequency Response

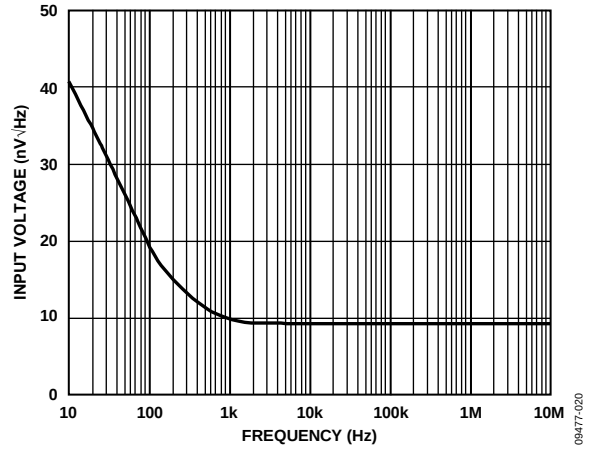


Figure 20. Input Voltage vs. Frequency

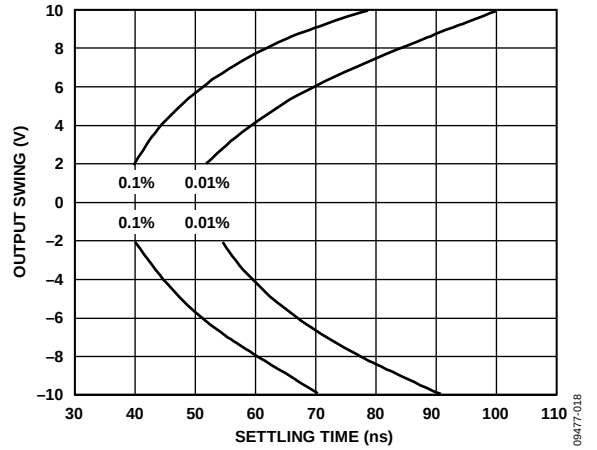


Figure 18. Output Swing vs. Settling Time

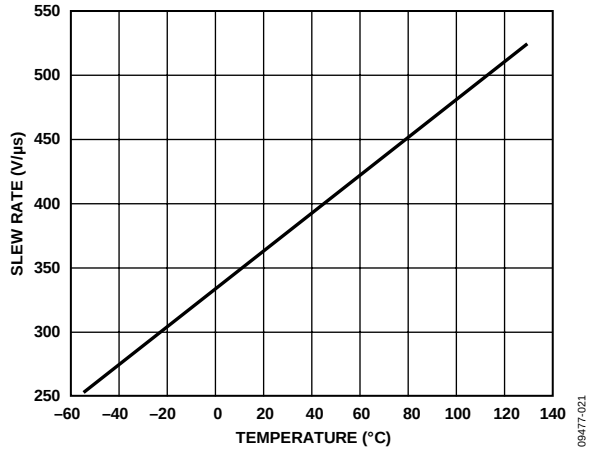


Figure 21. Slew Rate vs. Temperature

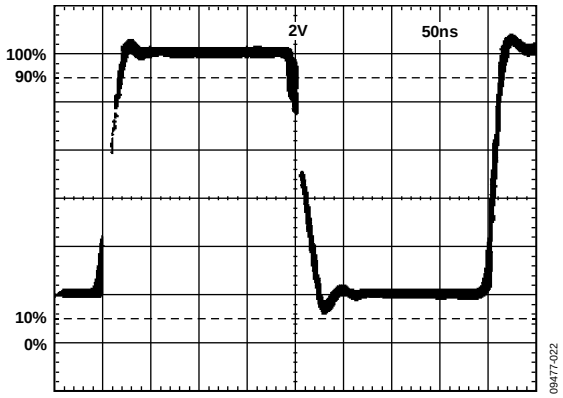


Figure 22. Inverting Large Signal Pulse Response (see Figure 24)

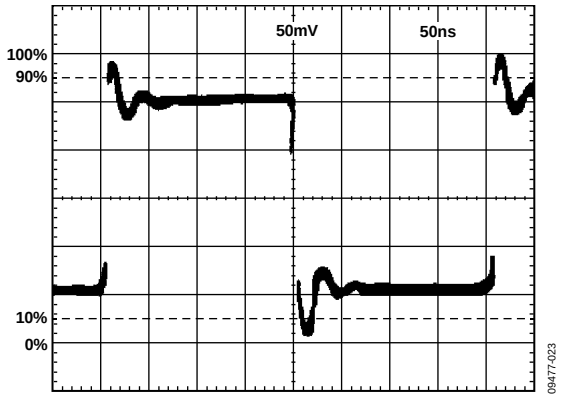


Figure 23. Inverting Small Signal Pulse Response (see Figure 24)

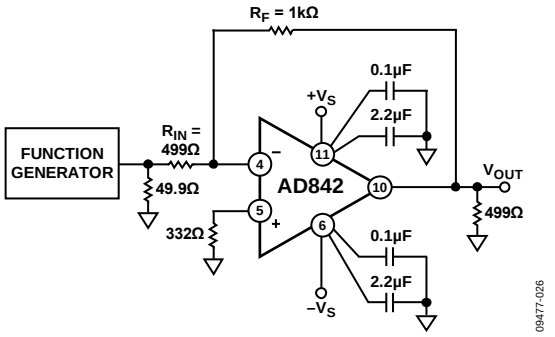


Figure 24. Inverting Amplifier Configuration (PDIP)

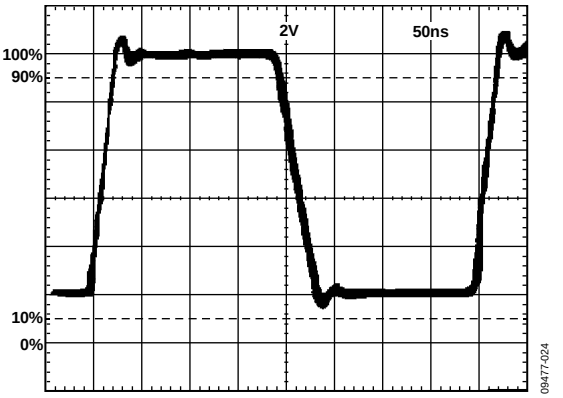


Figure 25. Noninverting Large Signal Pulse Response (see Figure 27)

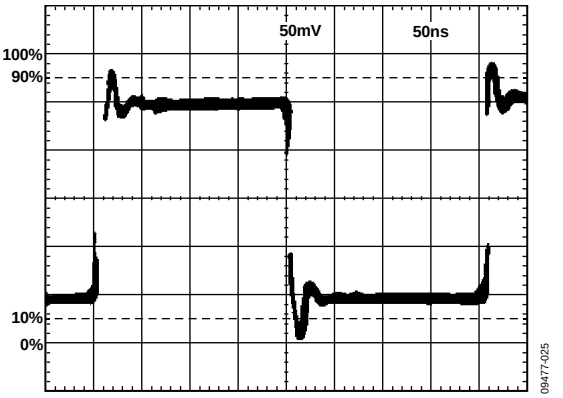


Figure 26. Noninverting Small Signal Pulse Response (see Figure 27)

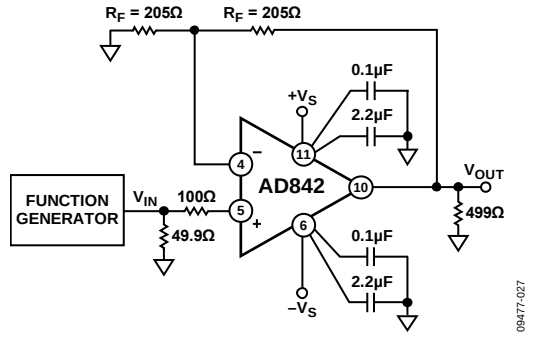


Figure 27. Noninverting Amplifier Configuration (PDIP)

THEORY OF OPERATION

OFFSET NULLING

The input offset voltage of the AD842 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 28 can be used.

SETTLING TIME

Figure 29 and Figure 31 show the settling performance of the AD842 in the test circuit shown in Figure 30.

Settling time is the interval of time from the application of an ideal step function input until the closed-loop amplifier output enters and remains within a specified error band.

This definition encompasses the major components that comprise settling time. They include the following:

- Propagation delay through the amplifier.
- Slewing time to approach the final output value.
- Time of recovery from the overload associated with slewing.
- Linear settling to within the specified error band.

Expressed in these terms, the measurement of settling time must be accurate to assure the user that the amplifier is worth consideration for the application.

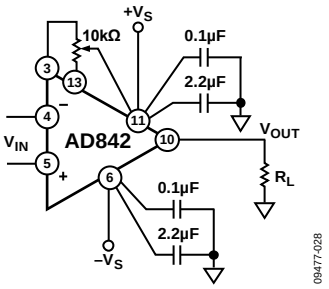


Figure 28. Offset Nulling (PDIP)

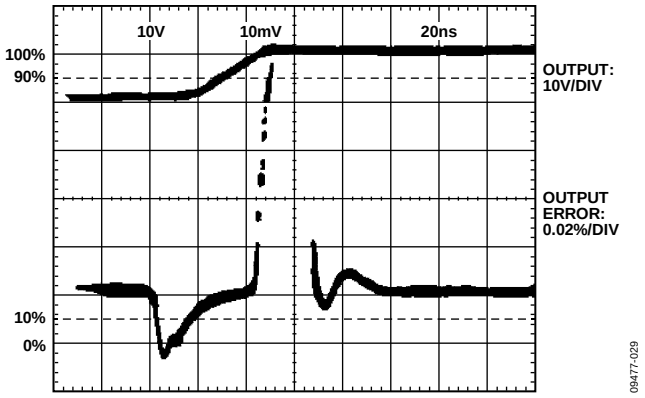


Figure 29. 0.01% Settling Time

Figure 30 shows how measurement of the AD842 0.01% settling in 100 ns is accomplished by amplifying the error signal from a false summing junction with a very high speed proprietary hybrid error amplifier specially designed to enable testing of small settling errors. Under test, the device drives a 300 Ω load. The input to the error amp is clamped to avoid possible problems associated with the overdrive recovery of the oscilloscope input amplifier. The error amp gains the error from the false summing junction by 15, and it contains a gain vernier to fine trim the gain.

Figure 31 shows the long-term stability of the settling characteristics of the AD842 output after a 10 V step. There is no evidence of settling tails after the initial transient recovery time. The use of a junction isolated process, together with careful layout, avoids these problems by minimizing the effects of transistor isolation capacitance discharge and thermally induced shifts in circuit operating points. These problems do not occur even under high output current conditions.

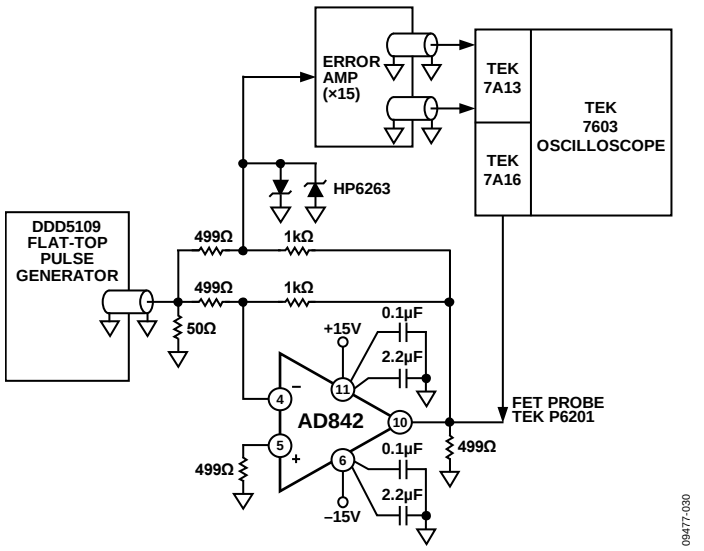


Figure 30. Settling Time Test Circuit (PDIP)

GROUNDING AND BYPASSING

In designing practical circuits with the AD842, the user must take some special precautions whenever high frequencies are involved.

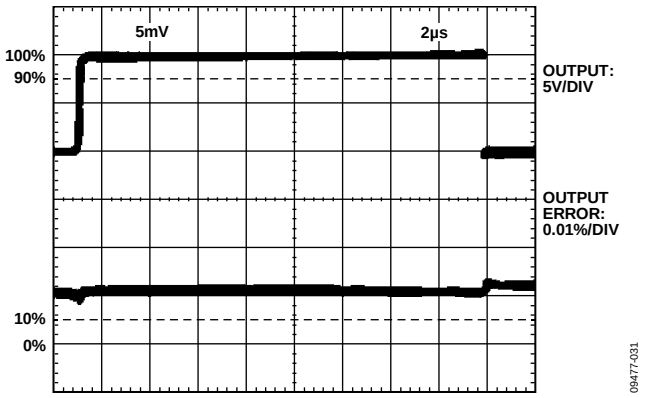


Figure 31. AD842 Settling Demonstrating No Settling Tails

Circuits must be built with short interconnect leads. Use large ground planes whenever possible to provide a low resistance, low inductance circuit path; this also minimizes the effects of high frequency coupling. Avoid sockets because the increased interlead capacitance can degrade bandwidth.

Use feedback resistors of low enough value to ensure that the time constant formed with the circuit capacitances does not limit the amplifier performance. Resistor values of less than 5 kΩ are recommended. If a larger resistor must be used, a small (<10 pF) feedback capacitor connected in parallel with the feedback resistor, R_F, can be used to compensate for these stray capacitances and to optimize the dynamic performance of the amplifier in the particular application.

Bypass power supply leads to ground as close as possible to the amplifier pins. A 2.2 µF capacitor in parallel with a 0.1 µF ceramic disk capacitor is recommended.

CAPACITIVE LOAD DRIVING ABILITY

Like all wideband amplifiers, the AD842 is sensitive to capacitive loading. The AD842 is designed to drive capacitive loads of up to 20 pF without degradation of its rated performance. Capacitive loads of greater than 20 pF decrease the dynamic performance of the device, although instability does not occur unless the load exceeds 100 pF.

USING A HEAT SINK

The AD842 draws less quiescent power than most precision high speed amplifiers and is specified for operation without a heat sink. However, when driving low impedance loads, the current to the load can be 10 times the quiescent current. This creates a noticeable temperature rise. Use of a small heat sink improves performance.

TERMINATED LINE DRIVER

The AD842 is optimized for high speed line driver applications. Figure 32 shows the AD842 driving a doubly terminated cable in a gain-of-2 follower configuration. The AD842 maintains a typical slew rate of 375 V/µs, which means it can drive a ±10 V, 6.0 MHz signal, or a ±3 V, 19.9 MHz signal.

The termination resistor, R_T, minimizes reflections from the far end of the cable when equal to the characteristic impedance of the cable. A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) can be placed between the AD842 output and the cable to damp any stray signals caused by a mismatch between R_T and the characteristic impedance of the cable. This configuration results in a cleaner signal. With this circuit, the voltage on the line equals V_{IN} because one half of V_{OUT} is dropped across R_{BT}.

The AD842 has a 100 mA minimum output current and, therefore, can drive ±5 V into a 50 Ω cable.

Choose the feedback resistors, R1 and R2, carefully. Large value resistors are desirable to limit the amount of current drawn from the amplifier output. Large resistors can cause amplifier instability because the parallel resistance of R1||R2 combines with the input capacitance (typically 2 pF to 5 pF) to create an additional pole. The voltage noise of the AD842 is equivalent to a 5 kΩ resistor; these large resistors can significantly increase the system noise. Resistor values of 1 kΩ or 2 kΩ are recommended.

If termination is not used, cables appear as capacitive loads and can be decoupled from the AD842 by a resistor in series with the output.

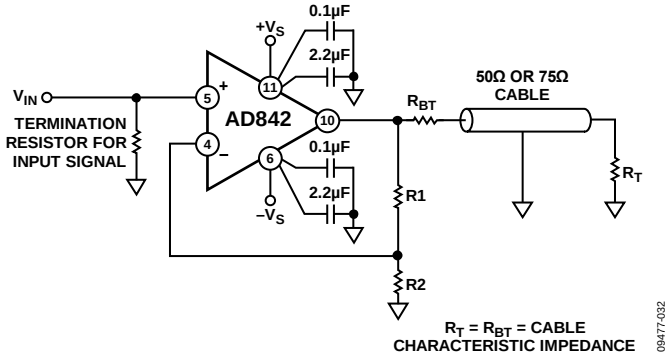


Figure 32. Line Driver Configuration (PDIP)

OVERDRIVE RECOVERY

Figure 33 shows the overdrive recovery capability of the AD842. Typical recovery time is 80 ns from negative overdrive and 400 ns from positive overdrive.

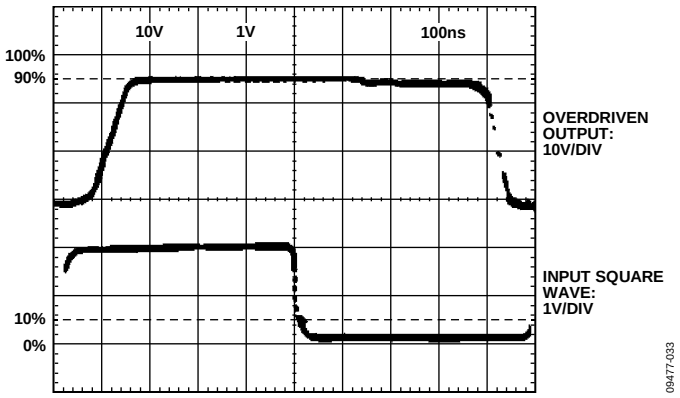


Figure 33. Overdrive Recovery

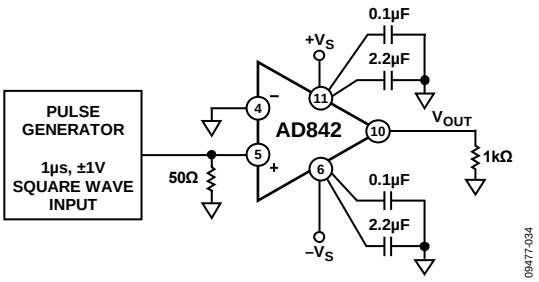
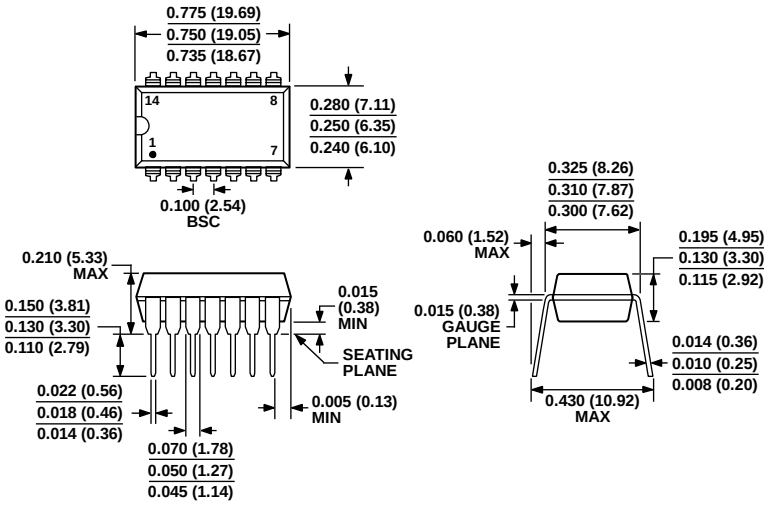


Figure 34. Overdrive Recovery Test Circuit (PDIP)

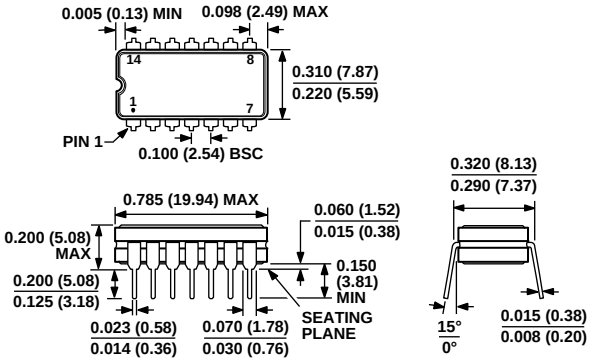
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 35. 14-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-14)
Dimensions Shown in Inches and (Millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 36. 14-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-14)
Dimensions Shown in Inches and (Millimeters)

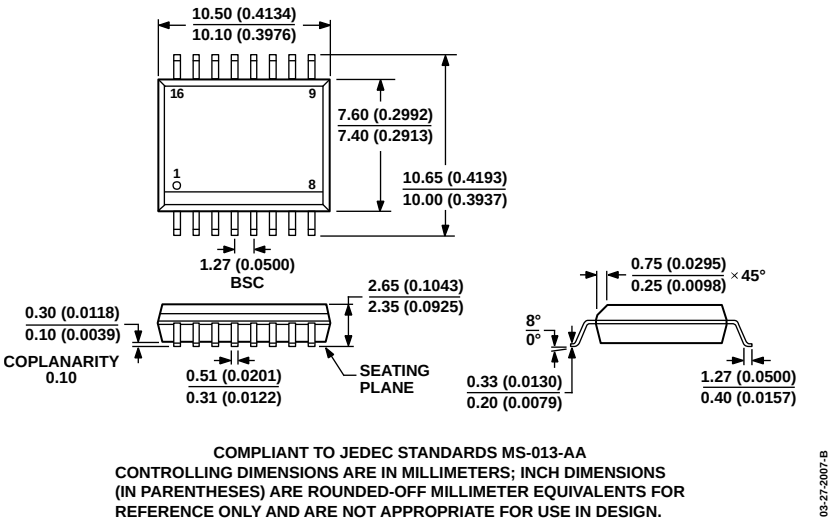


Figure 37. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions Shown in Inches and (Millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD842JNZ	0°C to 70°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
AD842JQ	0°C to 70°C	14-Lead Ceramic Dual In-Line Package [CERDIP]	Q-14
AD842KQ	0°C to 70°C	14-Lead Ceramic Dual In-Line Package [CERDIP]	Q-14
AD842JR-16	0°C to 70°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
AD842JRZ-16	0°C to 70°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
AD842KNZ	0°C to 70°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
AD842SCHIPS		Die	
AD842SQ	−55°C to +125°C	14-Lead Ceramic Dual In-Line Package [CERDIP]	Q-14

[1] Z = RoHS Compliant Part.

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