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REVISION HISTORY

10/2018—Rev. E to Rev. F

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Added 12-Ball WLCSP ... Universal
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Changes to Reference Output (1.25 V), Reference TC Parameter, Table 2 ... 4
Added θ_{JA} Thermal Impedance, WLCSP Parameter, Table 6 ... 10
Added Figure 8; Renumbered Sequentially ... 12
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Changes to Digital-to-Analog Converter (DAC) Section, Added Figure 54 and Figure 55, Renumbered Subsequent Figures ... 22
Changes to Ordering Guide ... 33

3/2007—Revision 0: Initial Version

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SPECIFICATIONS

SPECIFICATIONS—AD5625R/AD5645R/AD5665R

V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; $V_{REFIN} = V_{DD}$; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit	Test Conditions/Comments[1]
STATIC PERFORMANCE[2]								
AD5665R								
Resolution				16			Bits	
Relative Accuracy					±8	±16	LSB	
Differential Nonlinearity						±1	LSB	Guaranteed monotonic by design
AD5645R								
Resolution				14			Bits	
Relative Accuracy					±2	±4	LSB	
Differential Nonlinearity						±0.5	LSB	Guaranteed monotonic by design
AD5625R								
Resolution	12			12			Bits	
Relative Accuracy		±1	±4		±0.5	±1	LSB	
Differential Nonlinearity			±1			±0.25	LSB	Guaranteed monotonic by design
Zero-Code Error		2	10		2	10	mV	All 0s loaded to DAC register
Offset Error		±1	±10		±1	±10	mV	
Full-Scale Error		−0.1	±0.5		−0.1	±0.5	% FSR	All 1s loaded to DAC register
Gain Error		±0.1	±1.25		±0.1	±1	% FSR	
Zero-Code Error Drift		±2			±2		µV/°C	
Gain Temperature Coefficient		±2.5			±2.5		ppm	Of FSR/°C
DC Power Supply Rejection Ratio		−100			−100		dB	DAC code = midscale; V_{DD} = 5 V ± 10%
DC Crosstalk (External Reference)		15			15		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		10			10		µV/mA	Due to load current change
		8			8		µV	Due to powering down (per channel)
DC Crosstalk (Internal Reference)		25			25		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		20			20		µV/mA	Due to load current change
		10			10		µV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS[3]								
Output Voltage Range	0		V_{DD}	0		V_{DD}	V	Internal reference disabled
	0		$2 \times V_{REF}$			$2 \times V_{REF}$		Internal reference enabled
Capacitive Load Stability		2			2		nF	$R_L = \infty$
		10			10		nF	R_L = 2 kΩ
DC Output Impedance		0.5			0.5		Ω	
Short-Circuit Current		30			30		mA	V_{DD} = 5 V
Power-Up Time		4			4		µs	Coming out of power-down mode; V_{DD} = 5 V
REFERENCE INPUTS								
Reference Current		210	260		210	260	µA	$V_{REF} = V_{DD}$ = 5.5 V
Reference Input Range	0.75		V_{DD}	0.75		V_{DD}	V	
Reference Input Impedance		26			26		kΩ	

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Parameter	A Grade			B Grade			Unit	Test Conditions/Comments[1]
	Min	Typ	Max	Min	Typ	Max		
REFERENCE OUTPUT (1.25 V)								
Output Voltage	1.247		1.253	1.247		1.253	V	At ambient
Reference TC[3]		±10			±10		ppm/°C	TSSOP and LFCSP
					±15		ppm/°C	WLCSP
Output Impedance		7.5			7.5		kΩ	
REFERENCE OUTPUT (2.5 V)								V_{DD} = 4.5 V to 5.5 V
Output Voltage	2.495		2.505	2.495		2.505	V	At ambient
Reference TC[3]		±10			±5	±10	ppm/°C	
Output Impedance		7.5			7.5		kΩ	
LOGIC INPUTS (ADDRx, $\overline{CLR}$, $\overline{LDAC}$, POR)[3]								
I_{IN}, Input Current			±1			±1	µA	
V_{INL}, Input Low Voltage			0.15 × V_{DD}			0.15 × V_{DD}	V	
V_{INH}, Input High Voltage	0.85 × V_{DD}			0.85 × V_{DD}			V	
C_{IN}, Pin Capacitance		2			2		pF	
V_{HYST}, Input Hysteresis	0.1 × V_{DD}			0.1 × V_{DD}			V	
LOGIC INPUTS (SDA, SCL)[3]								
I_{IN}, Input Current			±1			±1	µA	
V_{INL}, Input Low Voltage			0.3 × V_{DD}			0.3 × V_{DD}	V	
V_{INH}, Input High Voltage	0.7 × V_{DD}			0.7 × V_{DD}			V	
C_{IN}, Pin Capacitance		2			2		pF	
V_{HYST}, Input Hysteresis	0.1 × V_{DD}			0.1 × V_{DD}			V	High speed mode
	0.05 × V_{DD}			0.05 × V_{DD}			V	Fast mode
LOGIC OUTPUTS (SDA)[3]								
V_{OL}, Output Low Voltage			0.4			0.4	V	I_{SINK} = 3 mA
			0.6			0.6	V	I_{SINK} = 6 mA
Floating-State Leakage Current			±1			±1	µA	
Floating-State Output Capacitance		2			2		pF	
POWER REQUIREMENTS								
V_{DD}	2.7		5.5	2.7		5.5	V	
I_{DD} (Normal Mode)[4]								$V_{IH} = V_{DD}$, V_{IL} = GND, full-scale loaded
V_{DD} = 4.5 V to 5.5 V		1.0	1.16		1.0	1.16	mA	Internal reference off
V_{DD} = 2.7 V to 3.6 V		0.9	1.05		0.9	1.05	mA	Internal reference off
V_{DD} = 4.5 V to 5.5 V		1.9	2.14		1.9	2.14	mA	Internal reference on
V_{DD} = 2.7 V to 3.6 V		1.4	1.59		1.4	1.59	mA	Internal reference on
I_{DD} (All Power-Down Modes)[5]								
V_{DD} = 2.7 V to 5.5 V		0.48	1		0.48	1	µA	$V_{IH} = V_{DD}$, V_{IL} = GND (LFCSP)
V_{DD} = 3.6 V to 5.5 V		0.48	1		0.48	1	µA	$V_{IH} = V_{DD}$, V_{IL} = GND (TSSOP)

[1] Temperature range of A and B grades is −40°C to +105°C.
[2] Linearity calculated using a reduced code range: AD5665R (Code 512 to Code 65,024), AD5645R (Code 128 to Code 16,256), AD5625R (Code 32 to Code 4064). Output unloaded.
[3] Guaranteed by design and characterization; not production tested.
[4] Interface inactive. All DACs active. DAC outputs unloaded.
[5] All DACs powered down. Power-down function is not available on 14-lead TSSOP devices when the device is powered with V_{DD} < 3.6 V.

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SPECIFICATIONS—AD5625/AD5665

V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; $V_{REFIN} = V_{DD}$; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	B Grade Min	B Grade Typ	B Grade Max	Unit	Test Conditions/Comments[1]
STATIC PERFORMANCE[2]					
AD5665					
Resolution	16			Bits	
Relative Accuracy		±8	±16	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic by design
AD5625					
Resolution	12			Bits	
Relative Accuracy		±0.5	±1	LSB	
Differential Nonlinearity			±0.25	LSB	Guaranteed monotonic by design
Zero-Code Error		2	10	mV	All 0s loaded to DAC register
Offset Error		±1	±10	mV	
Full-Scale Error		−0.1	±0.5	% FSR	All 1s loaded to DAC register
Gain Error		±0.1	±1	% FSR	
Zero-Code Error Drift		±2		µV/°C	
Gain Temperature Coefficient		±2.5		ppm	Of FSR/°C
DC Power Supply Rejection Ratio		−100		dB	DAC code = midscale; V_{DD} = 5 V ± 10%
DC Crosstalk (External Reference)		15		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		10		µV/mA	Due to load current change
		8		µV	Due to powering down (per channel)
DC Crosstalk (Internal Reference)		25		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		20		µV/mA	Due to load current change
		10		µV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0		V_{DD}	V	
Capacitive Load Stability		2		nF	$R_L = \infty$
		10		nF	R_L = 2 kΩ
DC Output Impedance		0.5		Ω	
Short-Circuit Current		30		mA	V_{DD} = 5 V
Power-Up Time		4		µs	Coming out of power-down mode; V_{DD} = 5 V
REFERENCE INPUTS					
Reference Current		210	260	µA	$V_{REF} = V_{DD}$ = 5.5 V
Reference Input Range	0.75		V_{DD}	V	
Reference Input Impedance		26		kΩ	
LOGIC INPUTS (ADDRx, $\overline{CLR}$, $\overline{LDAC}$, POR)[3]					
I_{IN}, Input Current			±1	µA	
V_{INL}, Input Low Voltage			0.15 × V_{DD}	V	
V_{INH}, Input High Voltage	0.85 × V_{DD}			V	
C_{IN}, Pin Capacitance		2		pF	
V_{HYST}, Input Hysteresis	0.1 × V_{DD}			V	
LOGIC INPUTS (SDA, SCL)[3]					
I_{IN}, Input Current			±1	µA	
V_{INL}, Input Low Voltage			0.3 × V_{DD}	V	
V_{INH}, Input High Voltage	0.7 × V_{DD}			V	
C_{IN}, Pin Capacitance		2		pF	
V_{HYST}, Input Hysteresis	0.1 × V_{DD}			V	High speed mode
	0.05 × V_{DD}			V	Fast mode

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Parameter	B Grade Min	B Grade Typ	B Grade Max	Unit	Test Conditions/Comments[1]
LOGIC OUTPUTS (SDA)[3]					
V_{OL}, Output Low Voltage			0.4	V	I_{SINK} = 3 mA
			0.6	V	I_{SINK} = 6 mA
Floating-State Leakage Current			±1	µA	
Floating-State Output Capacitance		2		pF	
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
I_{DD} (Normal Mode)[4]					$V_{IH} = V_{DD}$, V_{IL} = GND, full-scale loaded
V_{DD} = 4.5 V to 5.5 V		1.0	1.16	mA	
V_{DD} = 2.7 V to 3.6 V		0.9	1.05	mA	
I_{DD} (All Power-Down Modes)[5]					
V_{DD} = 2.7 V to 5.5 V		0.48	1	µA	$V_{IH} = V_{DD}$, V_{IL} = GND (LFCSP)
V_{DD} = 3.6 V to 5.5 V		0.48	1	µA	$V_{IH} = V_{DD}$, V_{IL} = GND (TSSOP)

[1] Temperature range of B grade is −40°C to +105°C.
[2] Linearity calculated using a reduced code range: AD5665 (Code 512 to Code 65,024), AD5625 (Code 32 to Code 4064). Output unloaded.
[3] Guaranteed by design and characterization; not production tested.
[4] Interface inactive. All DACs active. DAC outputs unloaded.
[5] All DACs powered down. Power-down function is not available on 14-lead TSSOP devices when the device is powered with V_{DD} < 3.6 V.

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AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; V_{REFIN} = V_{DD}; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments[3]
Output Voltage Settling Time					
AD5625R/AD5625		3	4.5	µs	¼ to ¾ scale settling to ±0.5 LSB
AD5645R		3.5	5	µs	¼ to ¾ scale settling to ±0.5 LSB
AD5665R/AD5665		4	7	µs	¼ to ¾ scale settling to ±2 LSB
Slew Rate		1.8		V/µs	
Digital-to-Analog Glitch Impulse					1 LSB change around major carry
		15		nV-s	LFCSP
		5		nV-s	TSSOP
Digital Feedthrough		0.1		nV-s	
Reference Feedthrough		−90		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency 10 Hz to 20 MHz
Digital Crosstalk		0.1		nV-s	
Analog Crosstalk		1		nV-s	External reference
		4		nV-s	Internal reference
DAC-to-DAC Crosstalk		1		nV-s	External reference
		4		nV-s	Internal reference
Multiplying Bandwidth		340		kHz	V_{REF} = 2 V ± 0.1 V p-p
Total Harmonic Distortion		−80		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency = 10 kHz
Output Noise Spectral Density		120		nV/√Hz	DAC code = midscale, 1 kHz
		100		nV/√Hz	DAC code = midscale, 10 kHz
Output Noise		15		µV p-p	0.1 Hz to 10 Hz

[1] Guaranteed by design and characterization; not production tested.
[2] See the Terminology section.
[3] Temperature range is −40°C to +105°C, typical at 25°C.

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I²C TIMING SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, f_{SCL} = 3.4 MHz, unless otherwise noted (see Figure 3; high speed mode timing specification applies only to the AD5625RBRUZ-2/AD5625RBRUZ-2REEL7 and AD5665RBRUZ-2/AD5665RBRUZ-2REEL7).

Table 5.

Parameter	Test Conditions[1]	Min	Max	Unit	Description
f_{SCL}[2]	Standard mode		100	kHz	Serial clock frequency
	Fast mode		400	kHz	
	High speed mode, C_B = 100 pF		3.4	MHz	
	High speed mode, C_B = 400 pF		1.7	MHz	
t_1	Standard mode	4		µs	t_{HIGH}, SCL high time
	Fast mode	0.6		µs	
	High speed mode, C_B = 100 pF	60		ns	
	High speed mode, C_B = 400 pF	120		ns	
t_2	Standard mode	4.7		µs	t_{LOW}, SCL low time
	Fast mode	1.3		µs	
	High speed mode, C_B = 100 pF	160		ns	
	High speed mode, C_B = 400 pF	320		ns	
t_3	Standard mode	250		ns	$t_{SU;DAT}$, data setup time
	Fast mode	100		ns	
	High speed mode	10		ns	
t_4	Standard mode	0	3.45	µs	$t_{HD;DAT}$, data hold time
	Fast mode	0	0.9	µs	
	High speed mode, C_B = 100 pF	0	70	ns	
	High speed mode, C_B = 400 pF	0	150	ns	
t_5	Standard mode	4.7		µs	$t_{SU;STA}$, setup time for a repeated start condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_6	Standard mode	4		µs	$t_{HD;STA}$, hold time (repeated) start condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_7	Standard mode	4.7		µs	t_{BUF}, bus-free time between a stop and a start condition
	Fast mode	1.3		µs	
t_8	Standard mode	4		µs	$t_{SU;STO}$, setup time for a stop condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_9	Standard mode		1000	ns	t_{RDA}, rise time of SDA signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	80	ns	
	High speed mode, C_B = 400 pF	20	160	ns	
t_{10}	Standard mode		300	ns	t_{FDA}, fall time of SDA signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	80	ns	
	High speed mode, C_B = 400 pF	20	160	ns	
t_{11}	Standard mode		1000	ns	t_{RCL}, rise time of SCL signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	40	ns	
	High speed mode, C_B = 400 pF	20	80	ns	
t_{11A}	Standard mode		1000	ns	t_{RCL1}, rise time of SCL signal after a repeated start condition and after an acknowledge bit
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	80	ns	
	High speed mode, C_B = 400 pF	20	160	ns	

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Parameter	Test Conditions[1]	Min	Max	Unit	Description
t_{12}	Standard mode		300	ns	t_{FCL}, fall time of SCL signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	40	ns	
	High speed mode, C_B = 400 pF	20	80	ns	
t_{13}	Standard mode	10		ns	$\overline{LDAC}$ pulse width low
	Fast mode	10		ns	
	High speed mode	10		ns	
t_{14}	Standard mode	300		ns	Falling edge of ninth SCL clock pulse of last byte of a valid write to $\overline{LDAC}$ falling edge
	Fast mode	300		ns	
	High speed mode	30		ns	
t_{15}	Standard mode	20		ns	$\overline{CLR}$ pulse width low
	Fast mode	20		ns	
	High speed mode	20		ns	
t_{SP}[3]	Fast mode	0	50	ns	Pulse width of spike suppressed
	High speed mode	0	10	ns	

[1] C_B refers to the capacitance on the bus line.
[2] The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate but has a negative effect on the EMC behavior of the device.
[3] Input filtering on the SCL and SDA inputs suppresses noise spikes that are less than 50 ns for fast mode or less than 10 ns for high speed mode.

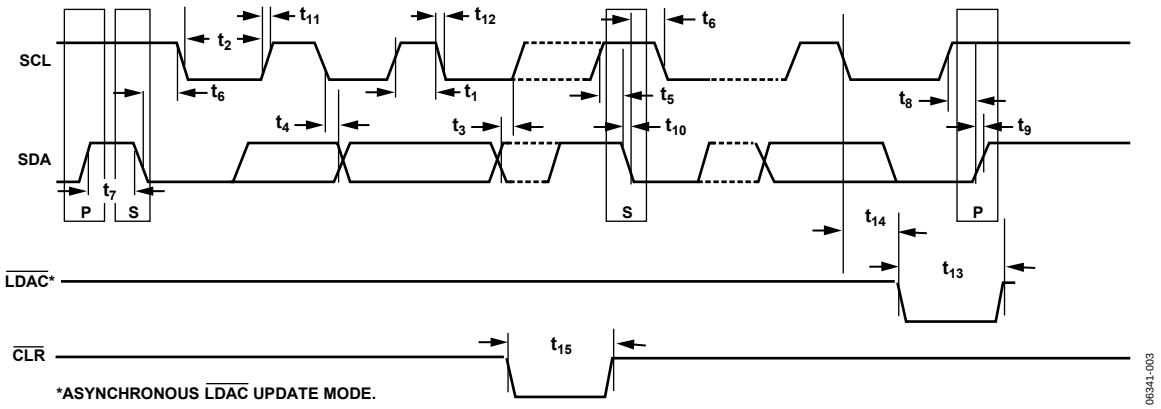

Figure 3. 2-Wire Serial Interface Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REFIN}/V_{REFOUT} to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range, Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J maximum)	150°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
θ_{JA} Thermal Impedance	
LFCSP (4-Layer Board)	61°C/W
TSSOP	150.4°C/W
WLCSP	75°C/W
Reflow Soldering Peak Temperature, RoHS Compliant	260°C ± 5°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

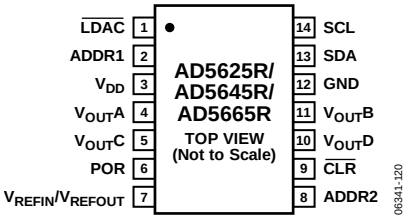

Figure 4. Pin Configuration (14-Lead TSSOP), R Suffix Version

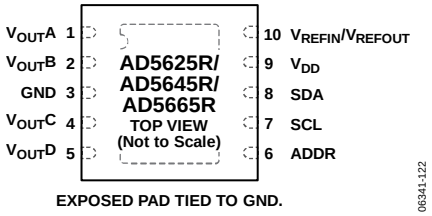

Figure 6. Pin Configuration (10-Lead LFCSP), R Suffix Version

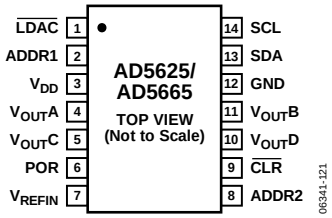

Figure 5. Pin Configuration (14-Lead TSSOP)

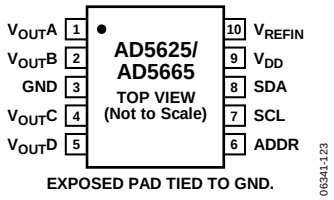

Figure 7. Pin Configuration (10-Lead LFCSP)

Table 7. Pin Function Descriptions

Pin Number			
14-Lead	**10-Lead**	**Mnemonic**	**Description**
1	N/A[1]	$\overline{\text{LDAC}}$	Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows simultaneous update of all DAC outputs. Alternatively, this pin can be tied permanently low.
2	N/A[1]	ADDR1	Three-State Address Input. Sets the two least significant bits (Bit A1, Bit A0) of the 7-bit slave address (see Table 10).
3	9	V_{DD}	Power Supply Input. These devices can be operated from 2.7 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	1	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
5	4	$V_{OUT}C$	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
6	N/A[1]	POR	Power-On Reset Pin. Tying the POR pin to GND powers up the device to 0 V. Tying the POR pin to V_{DD} powers up the device to midscale.
7	10	V_{REFIN}/V_{REFOUT}	The AD5625R/AD5645R/AD5665R have a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input. (The internal reference and reference output are only available on R suffix versions.) The AD5625/AD5665 have a reference input pin only.
8	N/A[1]	ADDR2	Three-State Address Input. Sets Bit A3 and Bit A2 of the 7-bit slave address (see Table 10).
9	N/A[1]	$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling-edge sensitive. While $\overline{\text{CLR}}$ is low, all LDAC pulses are ignored. When $\overline{\text{CLR}}$ is activated, zero scale is loaded to all input and DAC registers. This clears the output to 0 V. The device exits clear code mode on the falling edge of the ninth clock pulse of the last byte of the valid write. If $\overline{\text{CLR}}$ is activated during a write sequence, the write is aborted. If $\overline{\text{CLR}}$ is activated during high speed mode, the device exits high speed mode.
10	5	$V_{OUT}D$	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
11	2	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
12	3	GND	Ground Reference Point for All Circuitry on the Device.
13	8	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into or out of the 16-bit input register. It is a bidirectional, open-drain data line that should be pulled to the supply with an external pull-up resistor.
14	7	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into or out of the 16-bit input register.
N/A[1]	6	ADDR	Three-State Address Input. Sets the two least significant bits (Bit A1, Bit A0) of the 7-bit slave address (see Table 9).
	EPAD		For the 10-lead LFCSP, the exposed pad must be tied to GND.

[1] N/A means not applicable.

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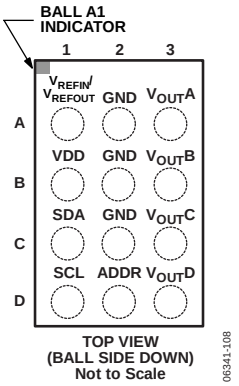

Figure 8. Pin Configuration (12-Ball WLCSP)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	V_{REFIN}/V_{REFOUT}	The AD5665R has a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input.
A2, B2, C2	GND	Ground Reference Point for All Circuitry on the Device.
A3	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
B1	V_{DD}	Power Supply Input. The AD5665R can be operated from 2.7 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
B3	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
C1	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into or out of the 16-bit input register. It is a bidirectional, open-drain data line that should be pulled to the supply with an external pull-up resistor.
C3	$V_{OUT}C$	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
D1	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into or out of the 16-bit input register.
D2	ADDR	Three-State Address Input. Sets the two least significant bits (Bit A1, Bit A0) of the 7-bit slave address (see Table 9).
D3	$V_{OUT}D$	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.

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TYPICAL PERFORMANCE CHARACTERISTICS

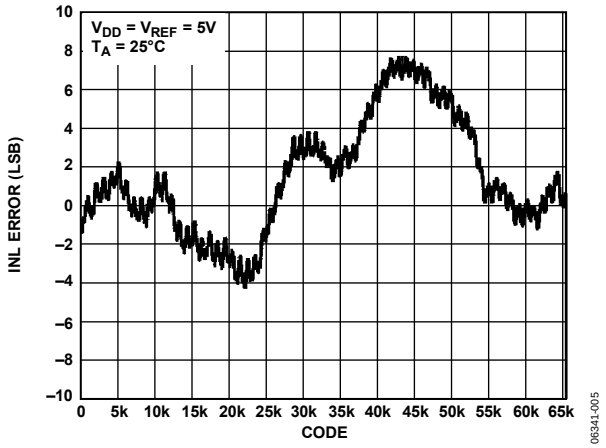

Figure 9. INL, AD5665, External Reference

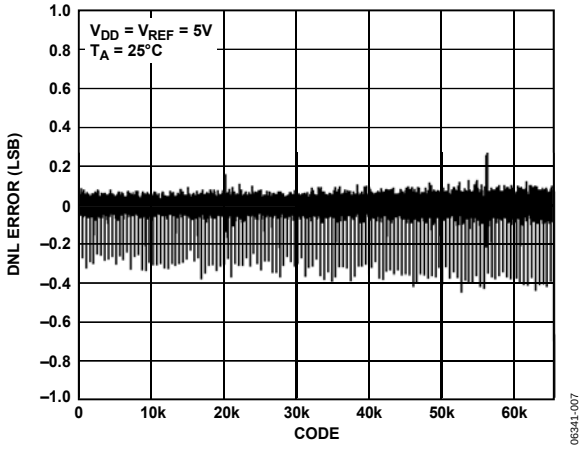

Figure 12. DNL, AD5665, External Reference

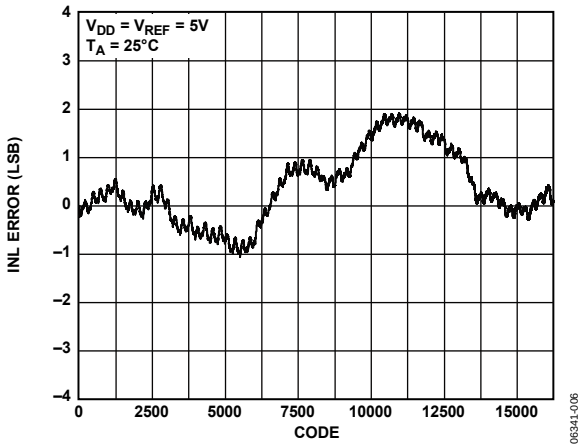

Figure 10. INL, AD5645R, External Reference

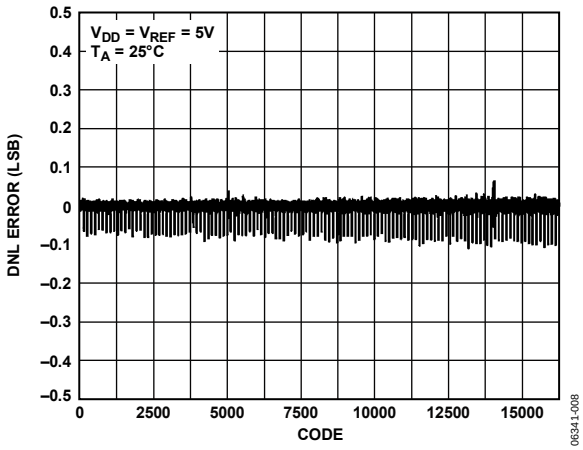

Figure 13. DNL, AD5645R, External Reference

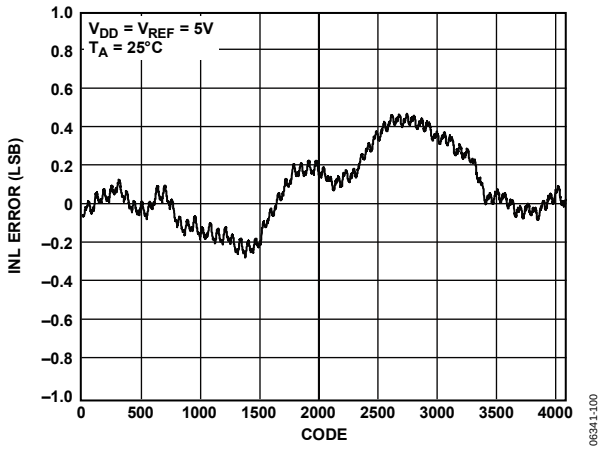

Figure 11. INL, AD5625, External Reference

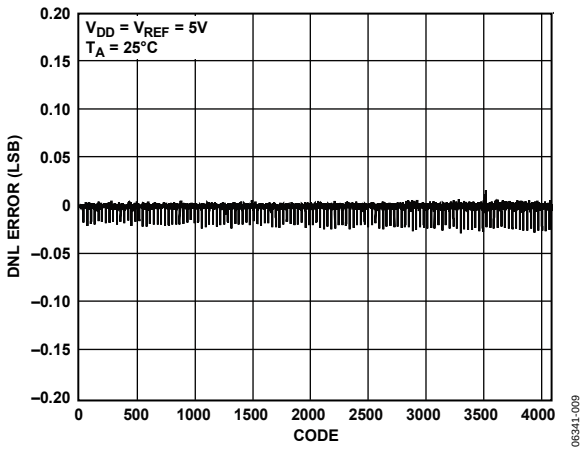

Figure 14. DNL, AD5625, External Reference

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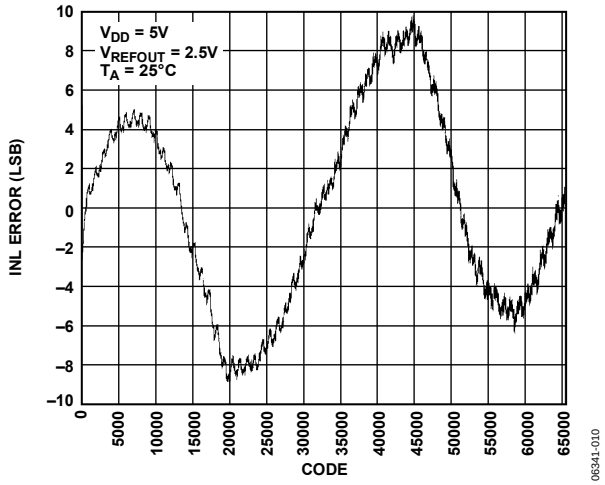

Figure 15. INL, AD5665R, 2.5 V Internal Reference

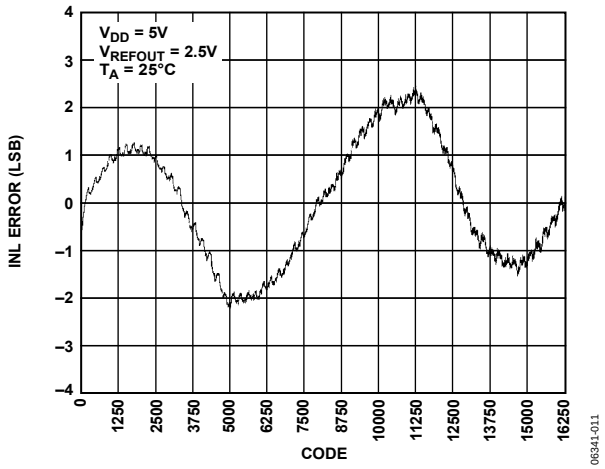

Figure 16. INL, AD5645R, 2.5 V Internal Reference

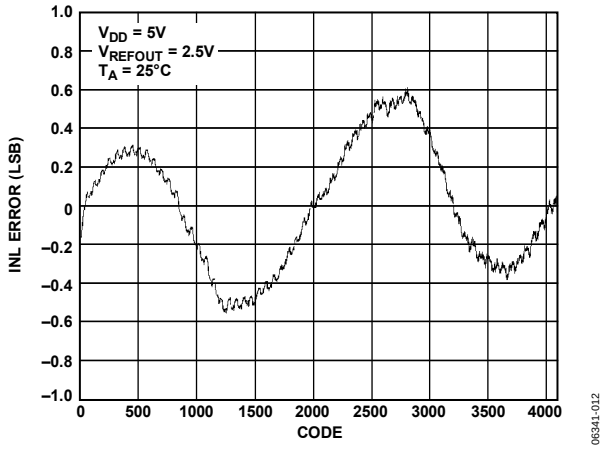

Figure 17. INL, AD5625R, 2.5 V Internal Reference

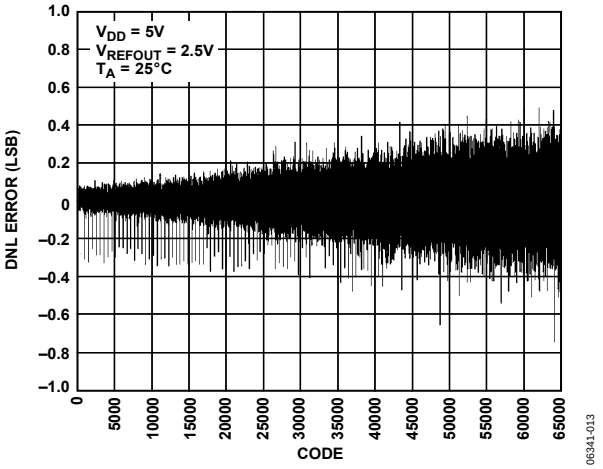

Figure 18. DNL, AD5665R, 2.5 V Internal Reference

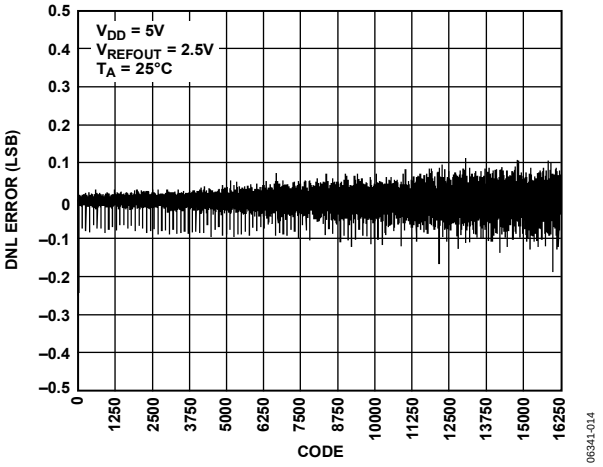

Figure 19. DNL, AD5645R, 2.5 V Internal Reference

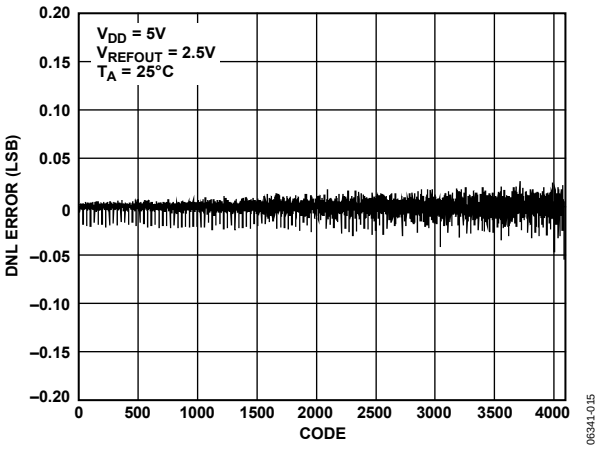

Figure 20. DNL, AD5625R, 2.5 V Internal Reference

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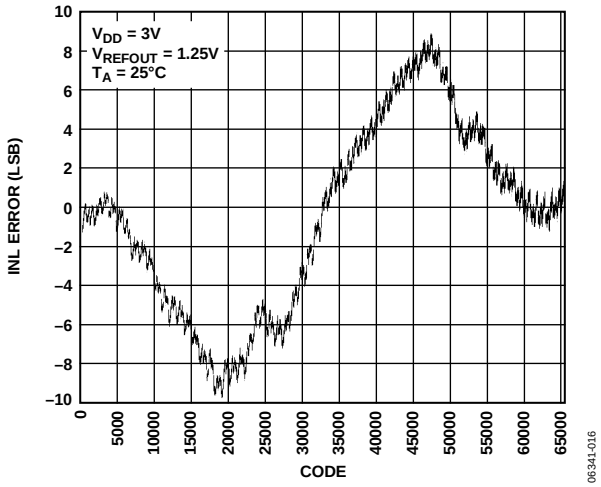

Figure 21. INL, AD5665R, 1.25 V Internal Reference

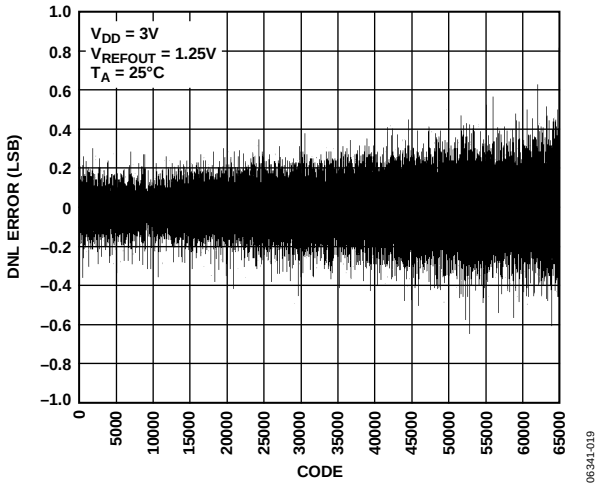

Figure 24. DNL, AD5665R, 1.25 V Internal Reference

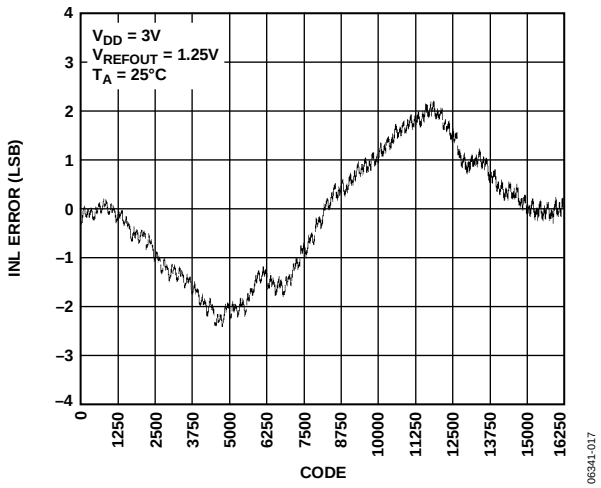

Figure 22. INL, AD5645R, 1.25 V Internal Reference

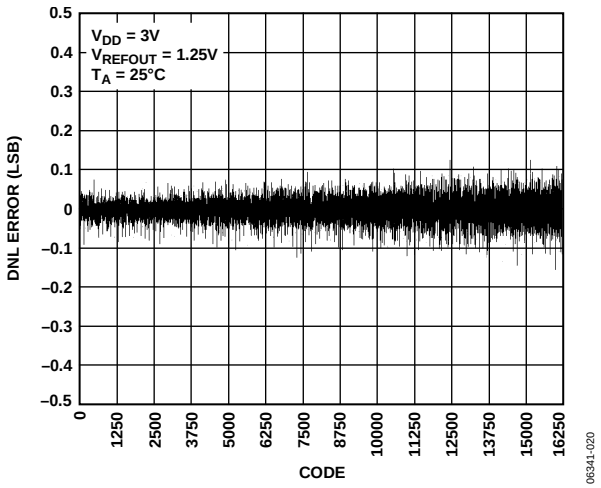

Figure 25. DNL, AD5645R, 1.25 V Internal Reference

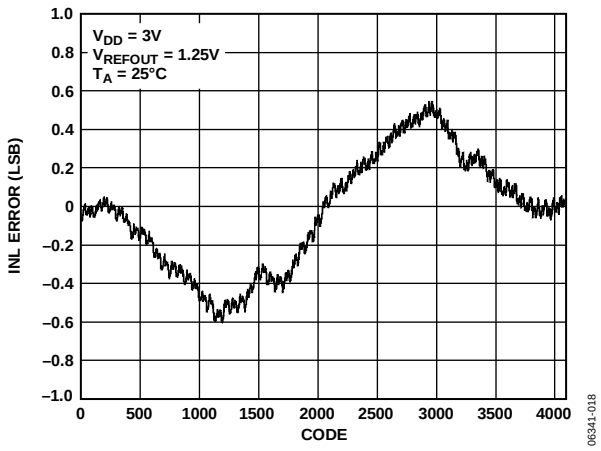

Figure 23. INL, AD5625R, 1.25 V Internal Reference

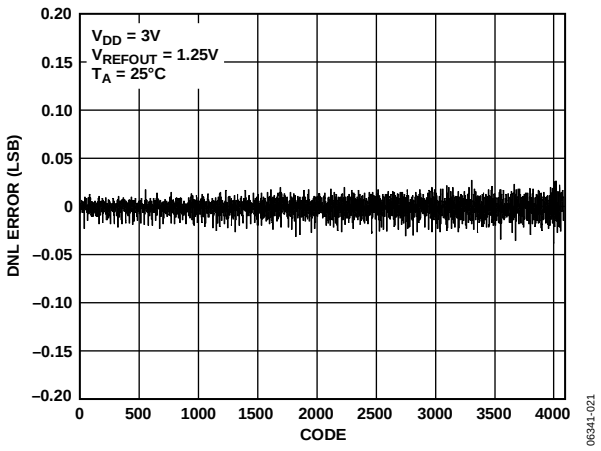

Figure 26. DNL, AD5625R, 1.25 V Internal Reference

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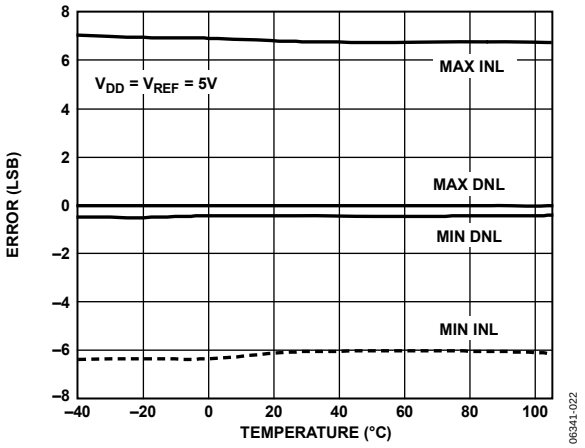

Figure 27. INL Error and DNL Error vs. Temperature

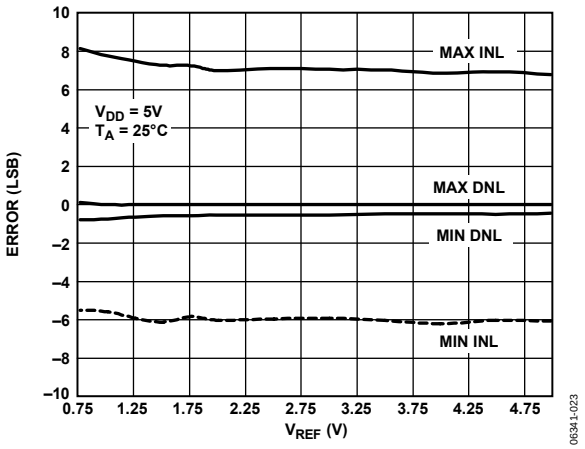

Figure 28. INL Error and DNL Error vs. V_{REF}

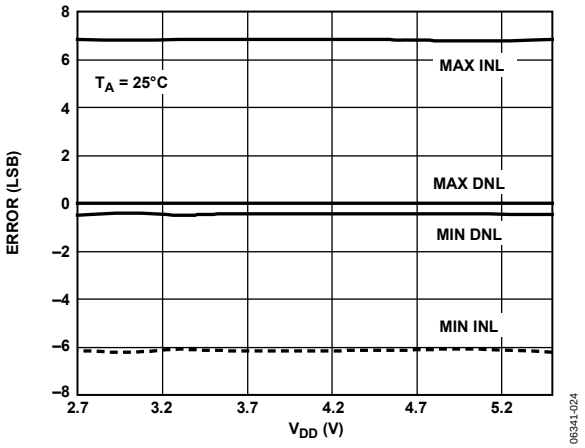

Figure 29. INL Error and DNL Error vs. Supply

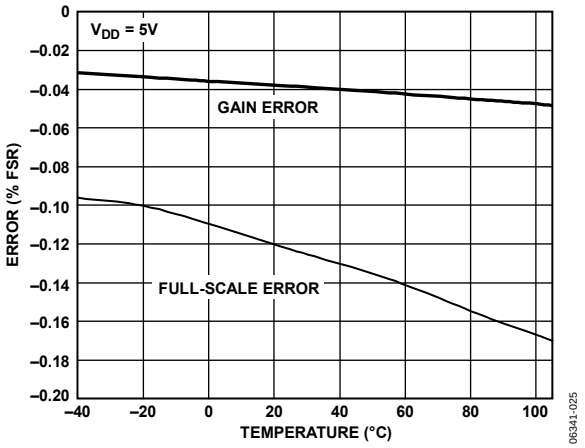

Figure 30. Gain Error and Full-Scale Error vs. Temperature

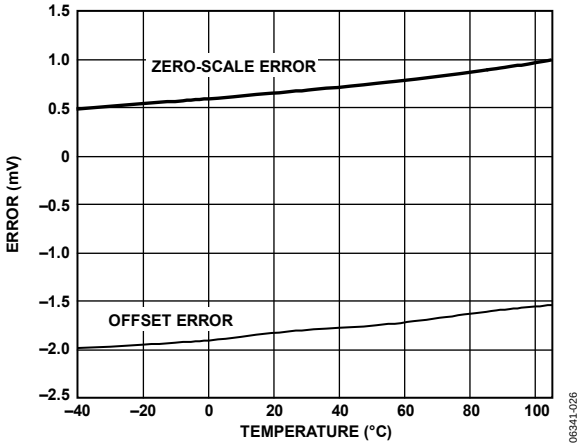

Figure 31. Zero-Scale Error and Offset Error vs. Temperature

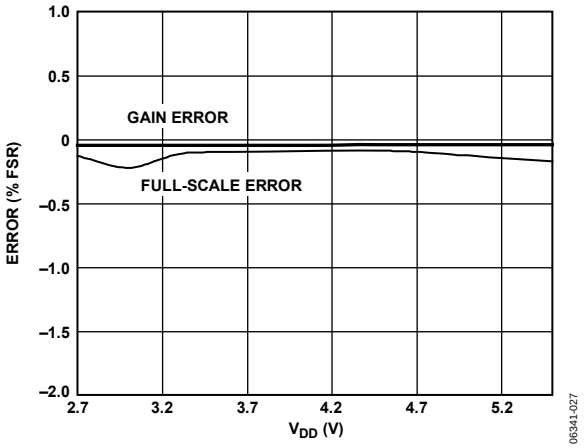

Figure 32. Gain Error and Full-Scale Error vs. Supply

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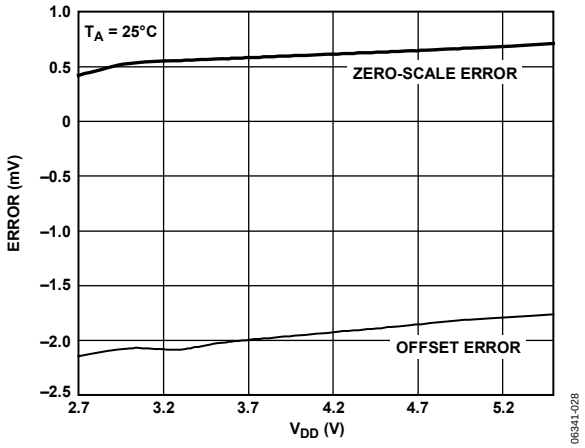

Figure 33. Zero-Scale Error and Offset Error vs. Supply

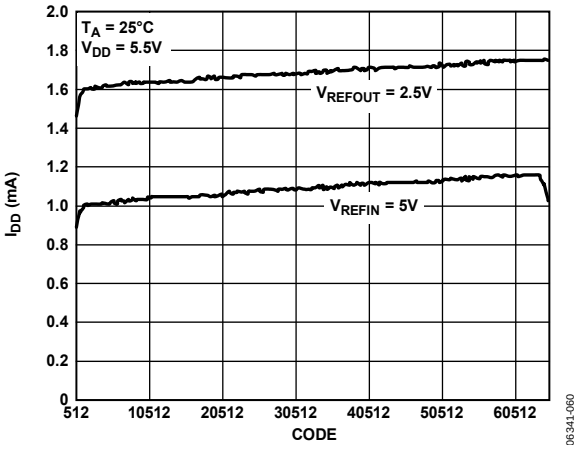

Figure 36. Supply Current vs. DAC Code

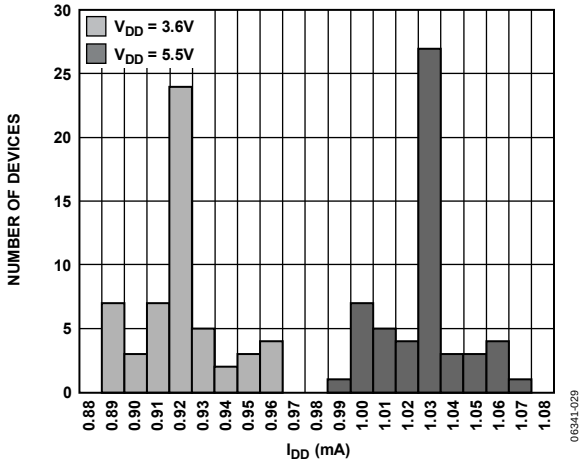

Figure 34. I_{DD} Histogram with External Reference

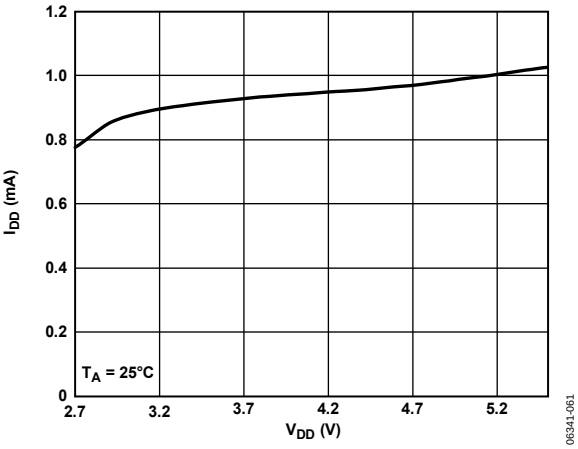

Figure 37. Supply Current vs. Supply

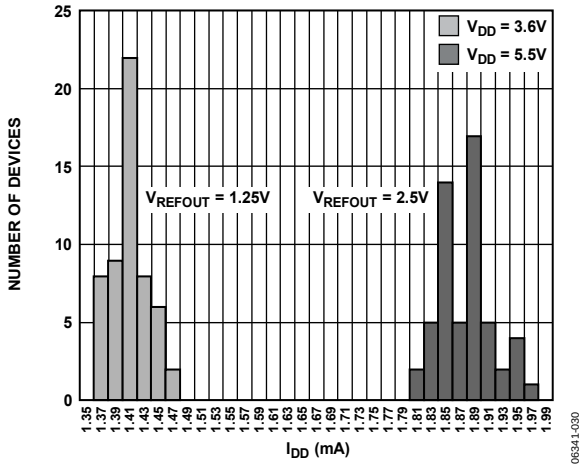

Figure 35. I_{DD} Histogram with Internal Reference

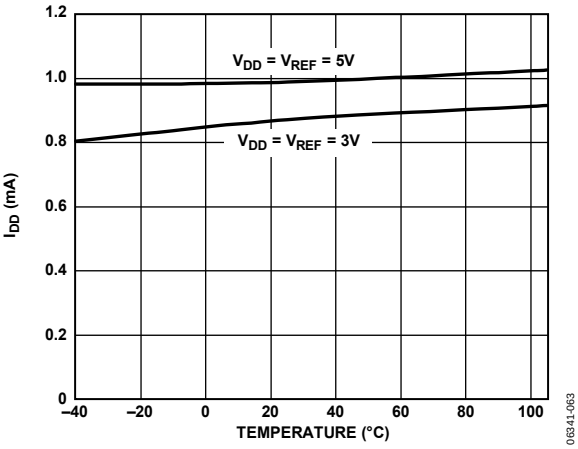

Figure 38. Supply Current vs. Temperature

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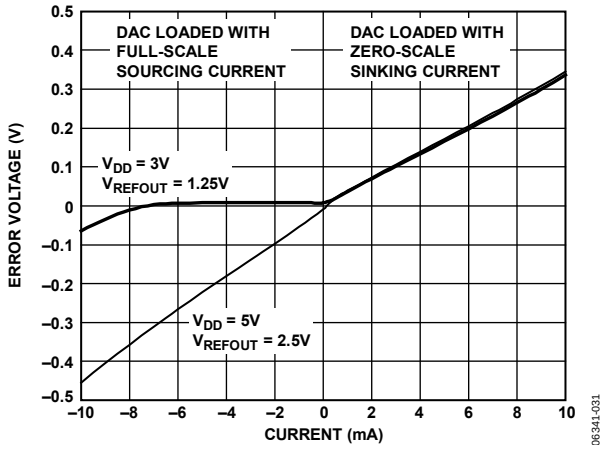

Figure 39. Headroom at Rails vs. Source and Sink

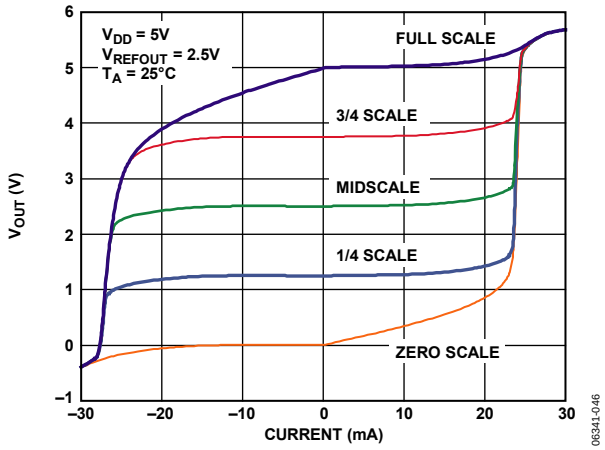

Figure 40. AD5625R/AD5645R/AD5665R with 2.5 V Reference, Source and Sink Capability

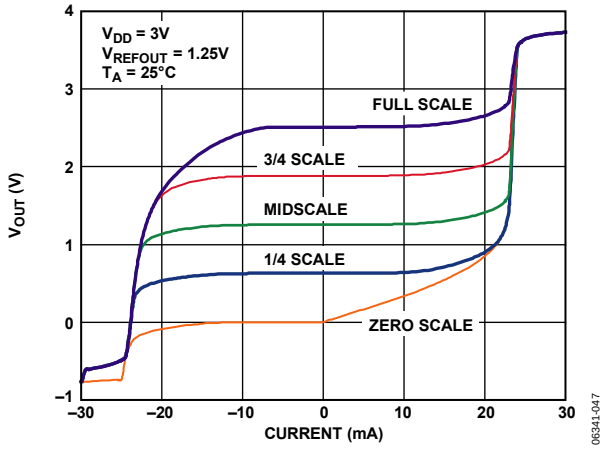

Figure 41. AD5625R/AD5645R/AD5665R with 1.25 V Reference, Source and Sink Capability

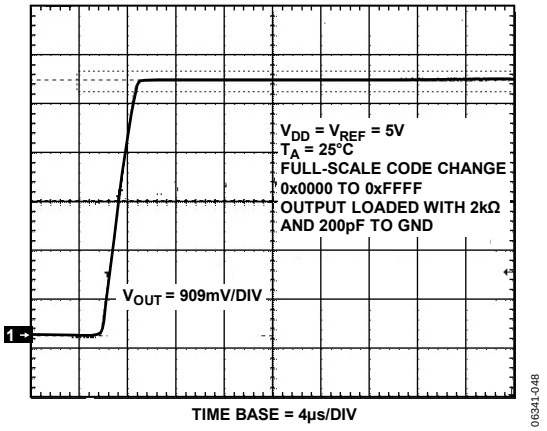

Figure 42. Full-Scale Settling Time, 5 V

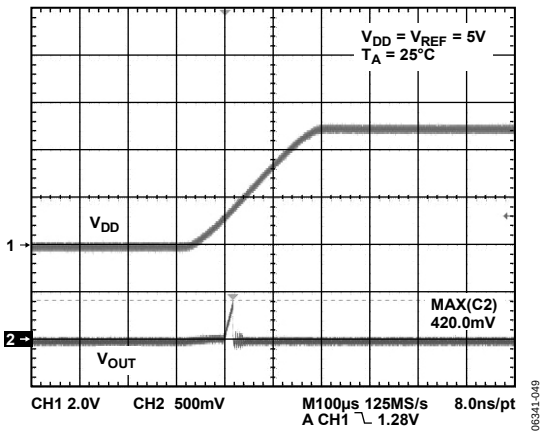

Figure 43. Power-On Reset to 0 V

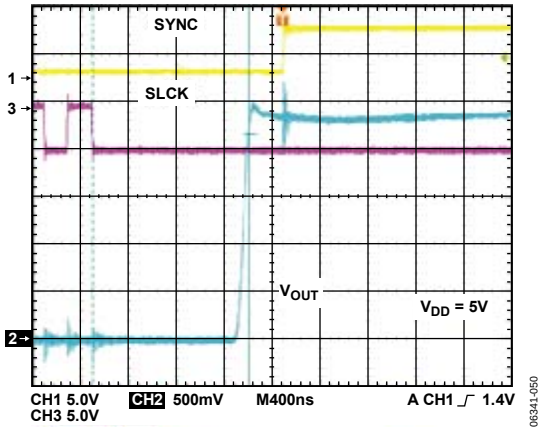

Figure 44. Exiting Power-Down to Midscale

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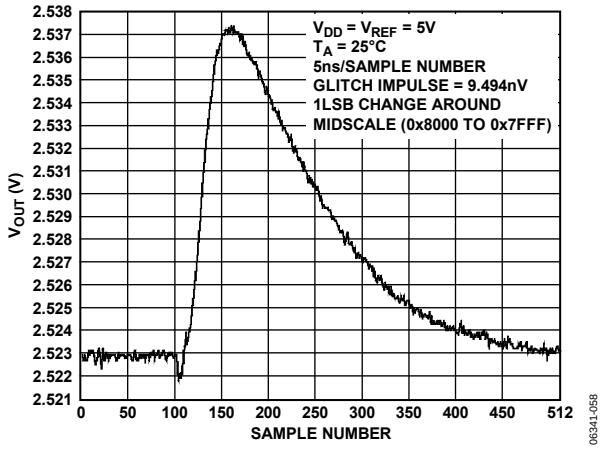

Figure 45. Digital-to-Analog Glitch Impulse (Negative)

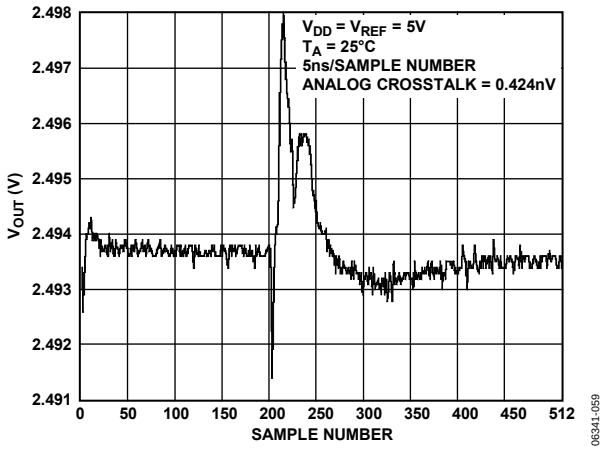

Figure 46. Analog Crosstalk, External Reference

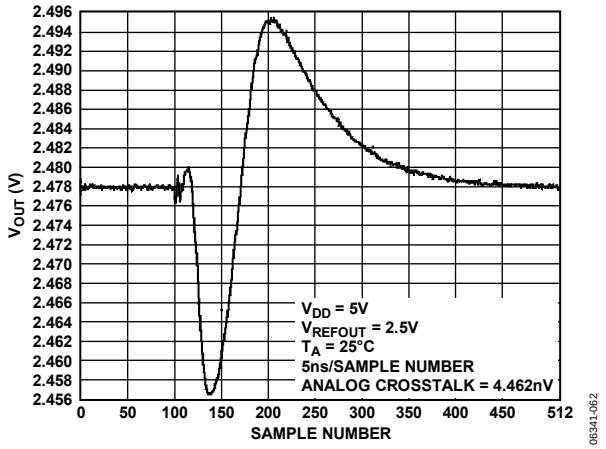

Figure 47. Analog Crosstalk, Internal Reference

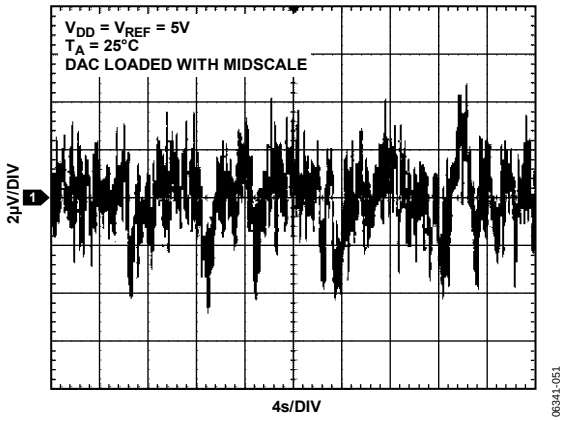

Figure 48. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

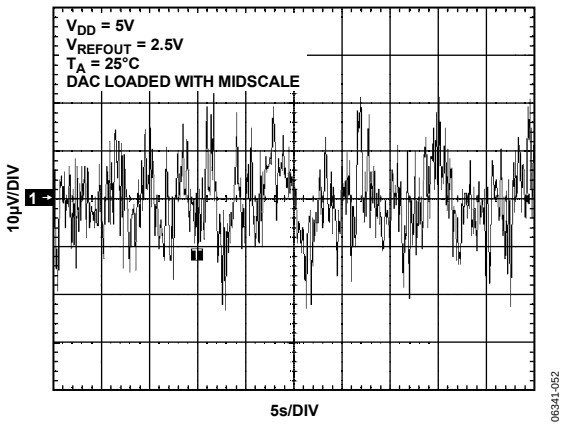

Figure 49. 0.1 Hz to 10 Hz Output Noise Plot, 2.5 V Internal Reference

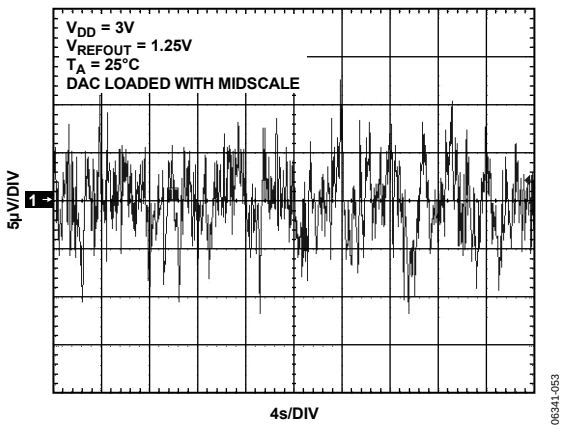

Figure 50. 0.1 Hz to 10 Hz Output Noise Plot, 1.25 V Internal Reference

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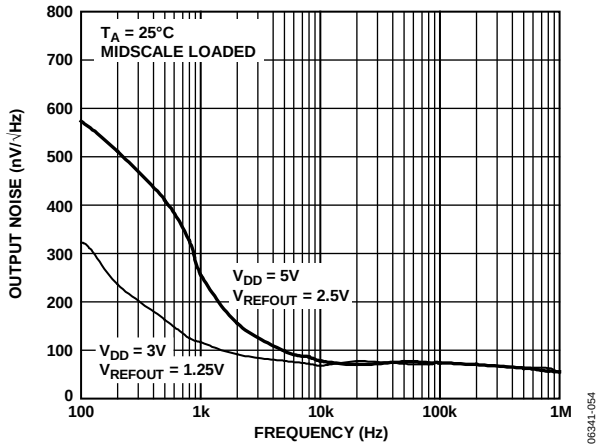

Figure 51. Noise Spectral Density, Internal Reference

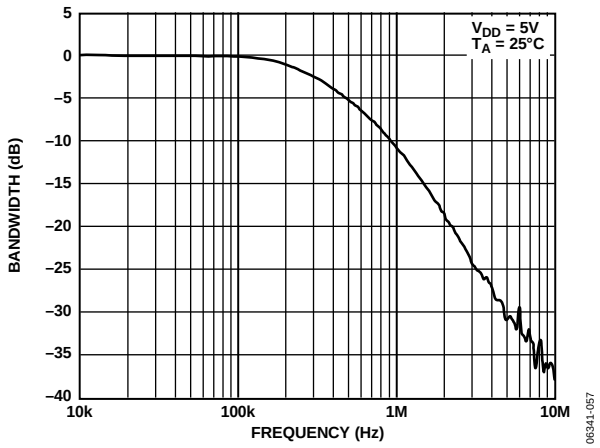

Figure 54. Multiplying Bandwidth

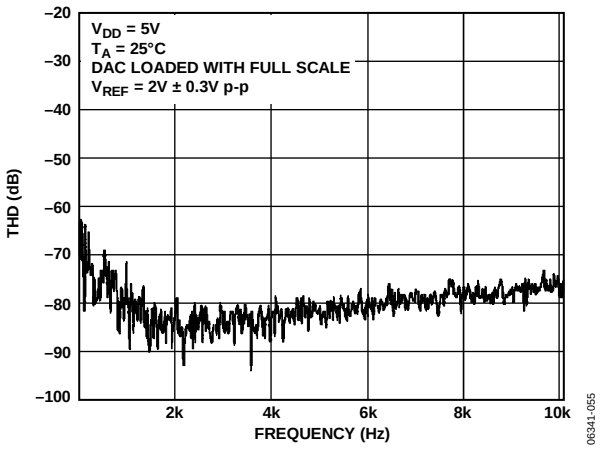

Figure 52. Total Harmonic Distortion

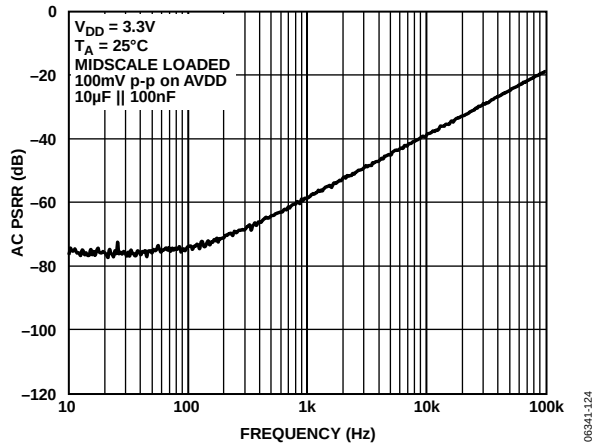

Figure 55. AC Power Supply Rejection Ratio (AC PSRR) vs. Frequency

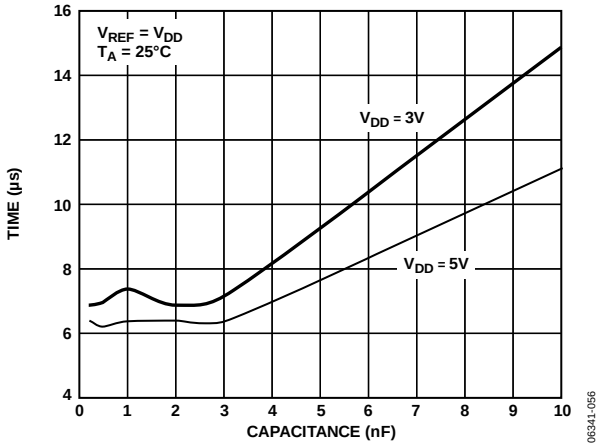

Figure 53. Settling Time vs. Capacitive Load

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TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design.

Zero-Code Error
Zero-code error is a measurement of the output error when zero scale (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5665R because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero-code error is expressed in millivolts (mV).

Full-Scale Error
Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed as a percentage of full-scale range (FSR).

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percentage of full-scale range (FSR).

Zero-Code Error Drift
Zero-code error drift is a measurement of the change in zero-code error with a change in temperature. It is expressed in microvolts per degrees Celsius (µV/°C).

Gain Temperature Coefficient
Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in parts per million (ppm) of full-scale range per degrees Celsius (FSR/°C).

Offset Error
Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured on the AD5665R with Code 512 loaded in the DAC register. It can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)
DC PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to the change in V_{DD} for full-scale output of the DAC. It is measured in decibels (dB). V_{REF} is held at 2 V, and V_{DD} is varied by ±10%.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change, and it is measured from the rising edge of the stop condition.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000) (see Figure 45).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV-s and is measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated. It is expressed in decibels (dB).

Output Noise Spectral Density
Output noise spectral density is a measurement of the internally generated random noise, which is characterized as a spectral density (nanovolts per square root of hertz frequency (nV/√Hz)). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nanovolts per square root of hertz frequency (nV/√Hz). A plot of noise spectral density is shown in Figure 51.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in microvolts (µV).

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has on another DAC kept at midscale. It is expressed in microvolts per milliampere (µV/mA).

Digital Crosstalk
This is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nanovolts per second (nV-s).

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Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) and then executing a software LDAC and monitoring the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nanovolts per second (nV-s).

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa) with $\overline{\text{LDAC}}$ low while monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in nanovolts per second (nV-s).

Multiplying Bandwidth
The multiplying bandwidth is a measure of the finite bandwidth of the amplifiers within the DAC. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)
THD is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. It is measured in decibels (dB).

AC Power Supply Rejection Ratio (AC PSRR)
AC PSRR is a measure of the rejection of the output voltage to ac changes in the power supplies applied to the DAC. It is measured for a given amplitude and frequency change in power supply voltage and is expressed in decibels.

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THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER (DAC)

The AD5625R/AD5645R/AD5665R and AD5625/AD5665 DACs are fabricated on a CMOS process. The AD5625/AD5665 do not have an internal reference, and the DAC architecture is shown in Figure 56. The AD5625R/AD5645R/AD5665R do have an internal reference and can be configured for use with either an internal or external reference (see Figure 56 and Figure 57).

Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by

$$V_{OUT} = V_{REFIN} \times \left(\frac{D}{2^N} \right)$$

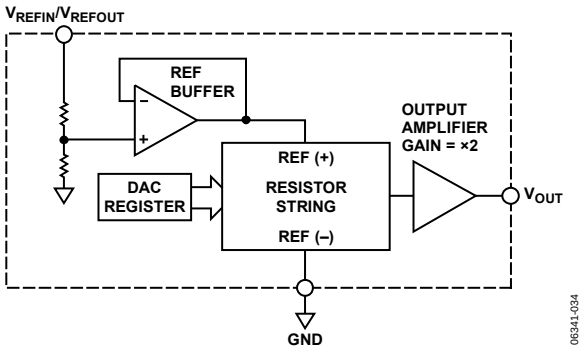

Figure 56. Internal Configuration When Using an External Reference

The ideal output voltage when using the internal reference is given by

$$V_{OUT} = 2 \times V_{REFOUT} \times \left(\frac{D}{2^N} \right)$$

where:
D is the decimal equivalent of the binary code that is loaded to the DAC register, as follows:

0 to 4095 for AD5625R/AD5625 (12-bit).
0 to 16,383 for AD5645R (14-bit).
0 to 65,535 for AD5665R/AD5665 (16-bit).

N is the DAC resolution.

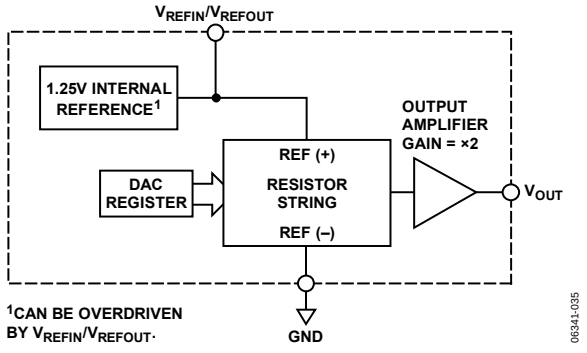

Figure 57. Internal Configuration When Using the Internal Reference

RESISTOR STRING

The resistor string is shown in Figure 58. It is simply a string of resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

OUTPUT AMPLIFIER

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. It can drive a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier are shown in Figure 39 and Figure 40. The slew rate is 1.8 V/µs with a ¼ to ¾ full-scale settling time of 7 µs.

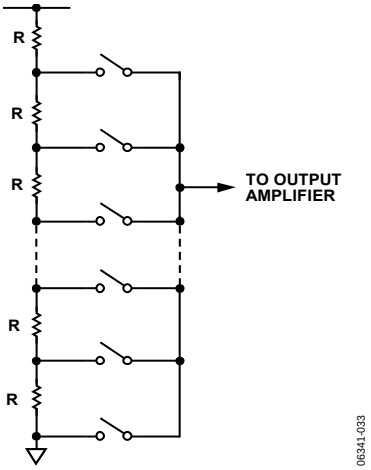

Figure 58. Resistor String

INTERNAL REFERENCE

The AD5625R/AD5645R/AD5665R feature an on-chip reference. Versions without the R suffix require an external reference. The on-chip reference is off at power-up and is enabled via a write to a control register. See the Internal Reference Setup section for details.

Versions packaged in a 10-lead LFCSP have a 1.25 V reference or a 2.5 V reference, giving a full-scale output of 2.5 V or 5 V, depending on the model selected (see the Ordering Guide). The WLCSP has an internal reference of 1.25 V. These devices can be operated with a V_{DD} supply of 2.7 V to 5.5 V. Versions packaged in a 14-lead TSSOP have a 2.5 V reference, giving a full-scale output of 5 V. Devices are functional with a V_{DD} supply of 2.7 V to 5.5 V, but with a V_{DD} supply of less than 5 V, the output is clamped to V_{DD}. See the Ordering Guide for a full list of models. The internal reference associated with each device is available at the V_{REFOUT} pin (available on R suffix versions only).

A buffer is required if the reference output is used to drive external loads. When using the internal reference, it is recommended that a 100 nF capacitor be placed between the reference output and GND for reference stability.

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EXTERNAL REFERENCE

The V_{REFIN} pin on the AD5625R/AD5645R/AD5665R allows the use of an external reference if the application requires it. The default condition of the on-chip reference is off at power-up. All devices can be operated from a single 2.7 V to 5.5 V supply.

SERIAL INTERFACE

The AD5625R/AD5645R/AD5665R and AD5625/AD5665 have 2-wire I²C-compatible serial interfaces. The AD5625R/AD5645R/AD5665R and AD5625/AD5665 can be connected to an I²C bus as a slave device, under the control of a master device. See Figure 3 for a timing diagram of a typical write sequence.

The AD5625R/AD5645R/AD5665R and AD5625/AD5665 support standard (100 kHz), fast (400 kHz), and high speed (3.4 MHz) data transfer modes. High speed operation is only available on selected models. See the Ordering Guide for a full list of models. Support is not provided for 10-bit addressing and general call addressing.

The AD5625R/AD5645R/AD5665R and AD5625/AD5665 each have a 7-bit slave address. The 10-lead and 12-ball versions of the device have a slave address whose five MSBs are 00011, and the two LSBs are set by the state of the ADDR address pin, which determines the state of the A0 and A1 address bits. The 14-lead versions of the device have a slave address whose three MSBs are 001, and the four LSBs are set by the ADDR1 and ADDR2 address pins, which determine the state of the A0 and A1 and A2 and A3 address bits, respectively.

The facility to make hardwired changes to the ADDR pin allows the user to incorporate up to three of these devices on one bus, as outlined in Table 9.

Table 9. ADDR Pin Settings (10-Lead and 12-Ball Packages)

ADDR Pin Connection	A1	A0
V_{DD}	0	0
NC	1	0
GND	1	1

The facility to make hardwired changes to the ADDR1 and the ADDR2 pins allows the user to incorporate up to nine of these devices on one bus, as outlined in Table 10.

Table 10. ADDR1, ADDR2 Pin Settings (14-Lead Package)

ADDR2 Pin Connection	ADDR1 Pin Connection	A3	A2	A1	A0
V_{DD}	V_{DD}	0	0	0	0
V_{DD}	NC	0	0	1	0
V_{DD}	GND	0	0	1	1
NC	V_{DD}	1	0	0	0
NC	NC	1	0	1	0
NC	GND	1	0	1	1
GND	V_{DD}	1	1	0	0
GND	NC	1	1	1	0
GND	GND	1	1	1	1

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address. The slave address corresponding to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its shift register.
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. When all data bits have been read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. If a stop condition is generated between the 7th and 8th clock pulse of the I²C address frame, a power cycle is required to recover the device. In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master brings the SDA line low before the 10th clock pulse, and then high during the 10th clock pulse to establish a stop condition.

WRITE OPERATION

When writing to the AD5625R/AD5645R/AD5665R and AD5625/AD5665, the user must begin with a start command followed by an address byte ($R/\overline{W} = 0$), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The AD5665 requires two bytes of data for the DAC and a command byte that controls various DAC functions. Three bytes of data must, therefore, be written to the DAC, the command byte followed by the most significant data byte and the least significant data byte, as shown in Figure 59 and Figure 60. After these data bytes are acknowledged by the AD5625R/AD5645R/AD5665R and AD5625/AD5665, a stop condition follows.

READ OPERATION

When reading data back from the AD5625R/AD5645R/AD5665R and AD5625/AD5665, the user begins with a start command followed by an address byte ($R/\overline{W} = 1$), after which the DAC acknowledges that it is prepared to transmit data by pulling SDA low. Two bytes of data are then read from the DAC, which are both acknowledged by the master as shown in Figure 61 and Figure 62. A stop condition follows. When a read operation is performed, the DAC shifts out the last transferred command.

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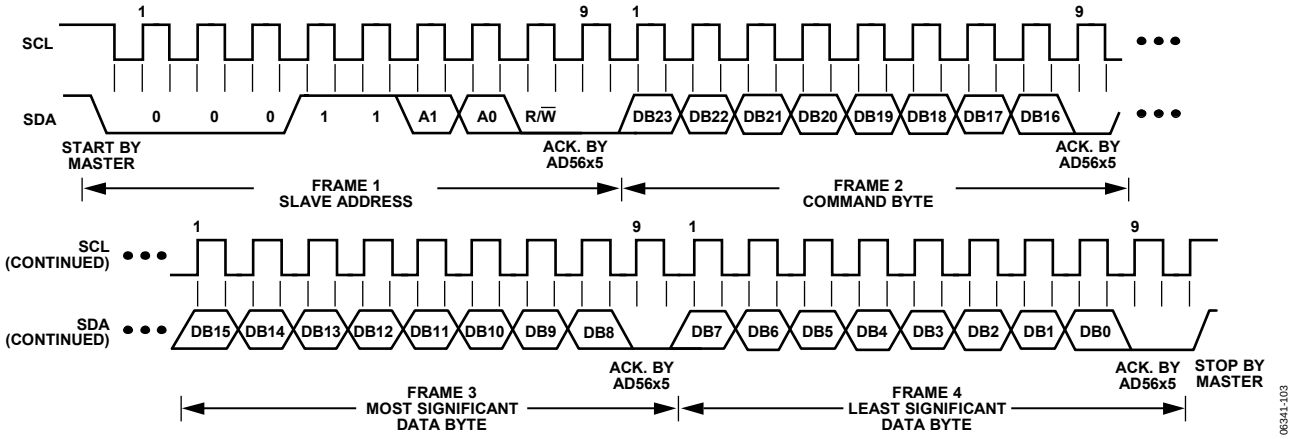

Figure 59. I²C Write Operation (10-Lead and 12-Ball Packages)

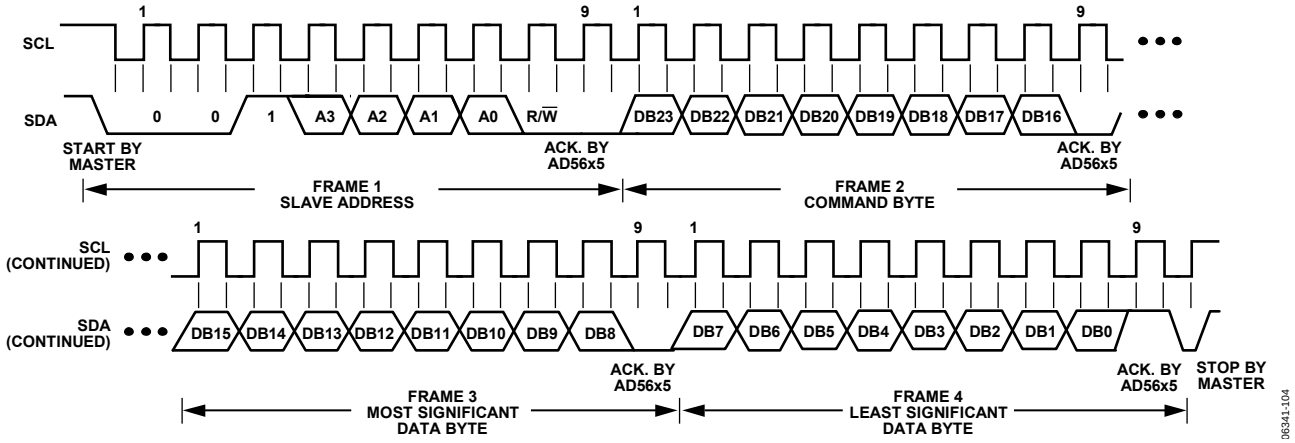

Figure 60. I²C Write Operation (14-Lead Package)

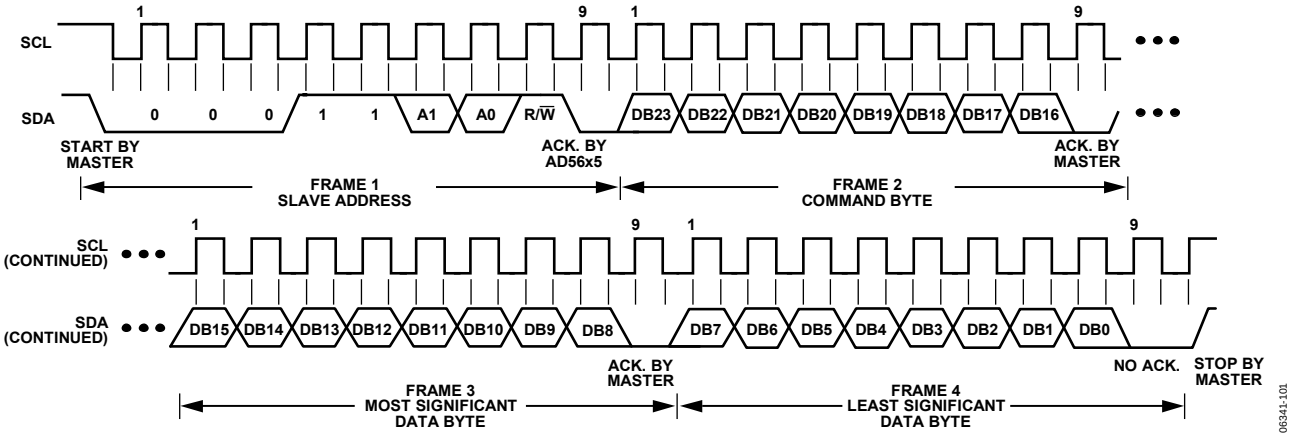

Figure 61. I²C Read Operation (10-Lead and 12-Ball Packages)

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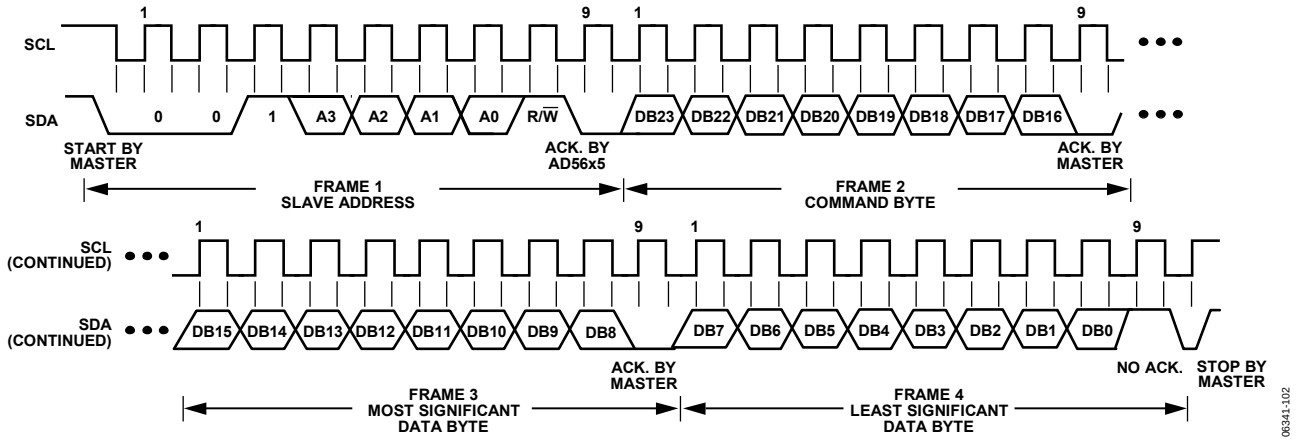

Figure 62. I²C Read Operation (14-Lead Package)

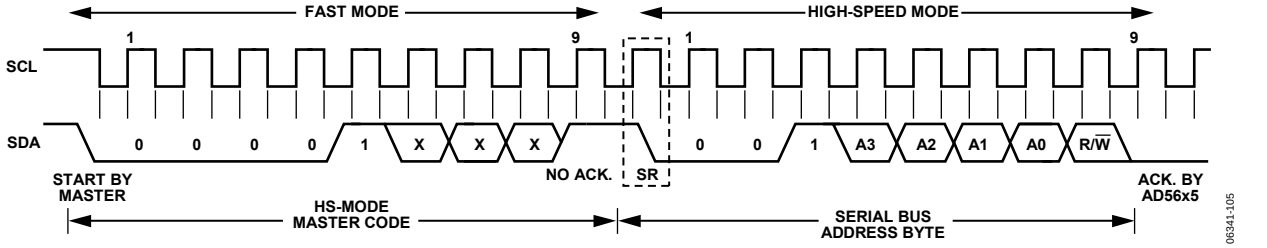

Figure 63. Placing the AD5625RBRUZ-2/AD5645RBRUZ-2/AD5665RBRUZ-2/AD5625RBRUZ-2REEL7/AD5645RBRUZ-2REEL7/AD5665RBRUZ-2REEL7 in High Speed Mode

HIGH SPEED MODE

Some models offer high speed serial communication with a clock frequency of 3.4 MHz. See the Ordering Guide for a full list of models.

High speed mode communication commences after the master addresses all devices connected to the bus with the Master Code 00001XXX to indicate that a high speed mode transfer is to begin. No device connected to the bus is permitted to acknowledge the high speed master code; therefore, the code is followed by a no acknowledge. Next, the master must issue a repeated start followed by the device address. The selected device then acknowledges its address. All devices continue to operate in high speed mode until the master issues a stop condition. When the stop condition is issued, the devices return to standard/fast mode. The device also returns to standard/fast mode when $\overline{\text{CLR}}$ is activated while the device is in high speed mode.

INPUT SHIFT REGISTER

The input shift register is 24 bits wide. Data is loaded into the device as a 24-bit word under the control of a serial clock input, SCL. The timing diagram for this operation is shown in Figure 3. The eight MSBs make up the command byte. DB23 is reserved and should always be set to 0 when writing to the device. DB22 (S) is used to select multiple byte operation. The next three bits are the command bits (C2, C1, and C0) that control the mode of operation of the device. See Table 11 for details. The last three bits of the first byte are the address bits (A2, A1, and A0). See Table 12 for details. The rest of the bits are the 16-/14-/12-bit data-word. The data-word comprises the 16-/14-/12-bit input code followed by two or four don't care bits for the AD5645R and the AD5625R/AD5625, respectively (see Figure 66 through Figure 68).

MULTIPLE BYTE OPERATION

Multiple byte operation is supported on the AD5625R/AD5645R/AD5665R and AD5625/AD5665. A 2-byte operation is useful for applications that require fast DAC updating and do not need to change the command byte. The S bit (DB22) in the command register can be set to 1 for 2-byte mode of operation (see Figure 65). For standard 3-byte and 4-byte operation, the S bit (DB22) in the command byte should be set to 0 (see Figure 64).

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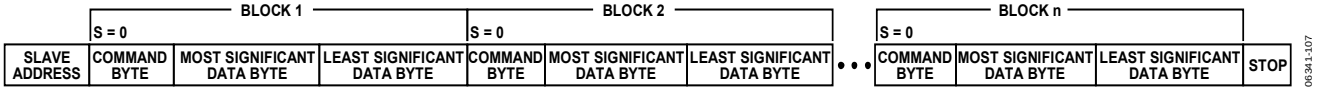

Figure 64. Multiple Block Write with Command Byte in Each Block (S = 0)

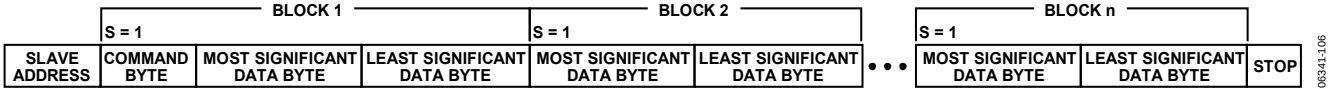

Figure 65. Multiple Block Write with Initial Command Byte Only (S = 1)

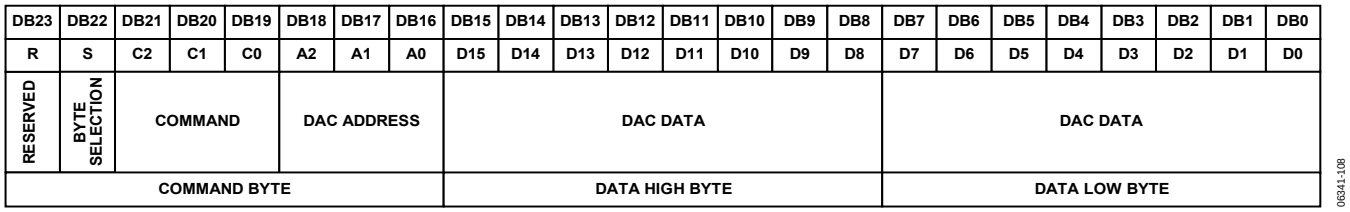

Figure 66. AD5665R/AD5665 Input Shift Register (16-Bit DAC)

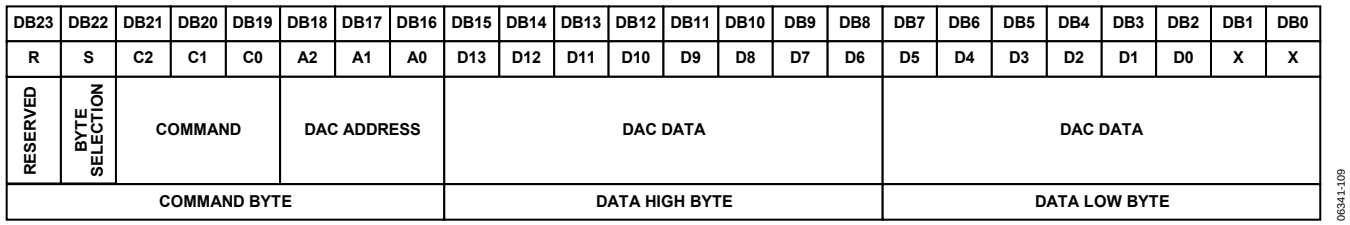

Figure 67. AD5645R Input Shift Register (14-Bit DAC)

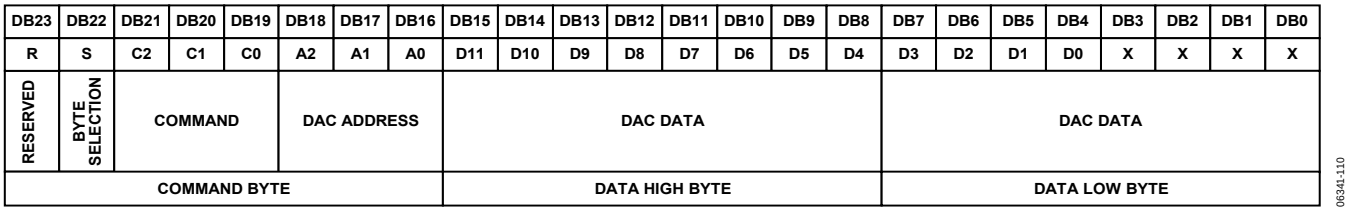

Figure 68. AD5625R/AD5625 Input Shift Register (12-Bit DAC)

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BROADCAST MODE

Broadcast addressing is supported on the AD5625R/AD5645R/AD5665R and AD5625/AD5665 in write mode only. Broadcast addressing can be used to synchronously update or power down multiple AD5625R/AD5645R/AD5665R and AD5625/AD5665 devices. When the broadcast address is used, the AD5625R/AD5645R/AD5665R and AD5625/AD5665 respond regardless of the states of the address pins. The AD5625R/AD5645R/AD5665R and AD5625/AD5665 broadcast address is 00010000.

Table 11. Command Definition

C2	C1	C0	Command
0	0	0	Write to input Register n
0	0	1	Update DAC Register n
0	1	0	Write to input Register n, update all (software $\overline{\text{LDAC}}$)
0	1	1	Write to and update DAC Channel n
1	0	0	Power up/power down
1	0	1	Reset
1	1	0	$\overline{\text{LDAC}}$ register setup
1	1	1	Internal reference setup (on/off)

Table 12. DAC Address Command

A2	A1	A0	ADDRESS (n)
0	0	0	DAC A
0	0	1	DAC B
0	1	0	DAC C
0	1	1	DAC D
1	1	1	All DACs

$\overline{\text{LDAC}}$ FUNCTION

The AD5625R/AD5645R/AD5665R and AD5625/AD5665 DACs have double-buffered interfaces consisting of two banks of registers: input registers and DAC registers. The input registers are connected directly to the input shift register, and the digital code is transferred to the relevant input register upon completion of a valid write sequence. The DAC registers contain the digital code used by the resistor strings.

Access to the DAC registers is controlled by the $\overline{\text{LDAC}}$ pin. When the $\overline{\text{LDAC}}$ pin is high, the DAC registers are latched and the input registers can change state without affecting the contents of the DAC registers. When $\overline{\text{LDAC}}$ is brought low, however, the DAC registers become transparent and the contents of the input registers are transferred to them. The double-buffered interface is useful if the user requires simultaneous updating of all DAC outputs. The user can write to one of the input registers individually and then, by bringing $\overline{\text{LDAC}}$ low when writing to the other DAC input register, all outputs update simultaneously.

These devices each contain an extra feature whereby a DAC register is not updated unless its input register has been updated since the last time $\overline{\text{LDAC}}$ was brought low. Normally, when $\overline{\text{LDAC}}$ is brought low, the DAC registers are filled with the contents of the input registers. In the case of the AD5625R/AD5645R/AD5665R and AD5625/AD5665, the DAC register updates only if the input register has changed since the last time the DAC register was updated, thereby removing unnecessary digital crosstalk.

The outputs of all DACs can be simultaneously updated, using the hardware $\overline{\text{LDAC}}$ pin.

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Synchronous $\overline{\text{LDAC}}$

The DAC registers are updated after new data is read in. $\overline{\text{LDAC}}$ can be permanently low or pulsed.

Asynchronous $\overline{\text{LDAC}}$

The outputs are not updated at the same time that the input registers are written to. When $\overline{\text{LDAC}}$ goes low, the DAC registers are updated with the contents of the input register.

The $\overline{\text{LDAC}}$ register gives the user full flexibility and control over the hardware $\overline{\text{LDAC}}$ pin (and software $\overline{\text{LDAC}}$ on the 10-lead devices that do not have the hardware $\overline{\text{LDAC}}$ pin—see Table 13). This register allows the user to select which combination of channels to simultaneously update when the hardware $\overline{\text{LDAC}}$ pin is executed. Setting the $\overline{\text{LDAC}}$ bit register to 0 for a DAC channel means that the update of this channel is controlled by the $\overline{\text{LDAC}}$ pin. If this bit is set to 1, this channel synchronously updates; that is, the DAC register is updated after new data is read in, regardless of the state of the $\overline{\text{LDAC}}$ pin. The device effectively sees the $\overline{\text{LDAC}}$ pin as being pulled low. See Table 14 for the $\overline{\text{LDAC}}$ register mode of operation. This flexibility is useful in applications when the user wants to simultaneously update select channels while the rest of the channels are synchronously updating.

Writing to the DAC using Command 110 loads the 4-bit $\overline{\text{LDAC}}$ register [DB3:DB0]. The default for each channel is 0; that is, the $\overline{\text{LDAC}}$ pin works normally. Setting the bits to 1 means that the DAC register is updated, regardless of the state of the $\overline{\text{LDAC}}$ pin. See Figure 69 for the contents of the input shift register during the $\overline{\text{LDAC}}$ register setup command.

Table 13. $\overline{\text{LDAC}}$ Register Mode of Operation on the 10-Lead LFCSP (Load DAC Register)

$\overline{\text{LDAC}}$ Bits (DB3 to DB0)	$\overline{\text{LDAC}}$ Mode of Operation
0	Normal operation (default), DAC register update is controlled by the write command.
1	The DAC registers are updated after new data is read in.

Table 14. $\overline{\text{LDAC}}$ Register Mode of Operation on the 14-Lead TSSOP (Load DAC Register)

$\overline{\text{LDAC}}$ Bits (DB3 to DB0)	$\overline{\text{LDAC}}$ Pin	$\overline{\text{LDAC}}$ Operation
0	1/0	Determined by the $\overline{\text{LDAC}}$ pin.
1	X = don't care	The DAC registers are updated after new data is read in.

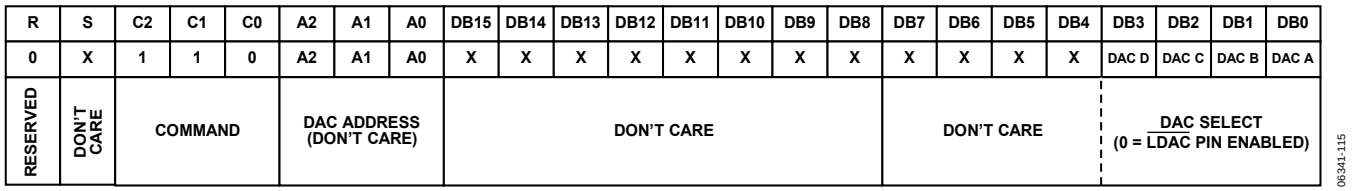

Figure 69. $\overline{\text{LDAC}}$ Setup Command

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POWER-DOWN MODES

Command 100 is reserved for the power-up/power-down function. The power-up/power-down modes are programmed by setting Bit DB5 and Bit DB4. This defines the output state of the DAC amplifier, as shown in Table 15. Bit DB3 to Bit DB0 determine to which DAC or DACs the power-up/power-down command is applied. Setting one of these bits to 1 applies the power-up/power-down state defined by DB5 and DB4 to the corresponding DAC. If a bit is 0, the state of the DAC is unchanged. Figure 71 shows the contents of the input shift register for the power-up/power-down command.

When Bit DB5 and Bit DB4 are set to 0, the device works normally with its normal power consumption of 1 mA at 5 V. However, for the three power-down modes, the supply current falls to 480 nA at 5 V. Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This allows the output impedance of the device to be known while the device is in power-down mode. The outputs can either be connected internally to GND through a 1 kΩ or 100 kΩ resistor or be left open-circuited (three-state) as shown in Figure 68.

Note that the 14-lead TSSOP models offer the power-down function when the device is operated with a V_{DD} of 3.6 V to 5.5 V. The 10-lead LFCSP models offer the power-down function when the device is powered with a V_{DD} of 2.7 V to 5.5 V.

Table 15. Modes of Operation for the AD5625R/AD5645R/AD5665R and AD5625/AD5665

DB5	DB4	Operating Mode
0	0	Normal operation
		Power-down modes
0	1	1 kΩ pull-down resistor to GND
1	0	100 kΩ pull-down resistor to GND
1	1	Three-state, high impedance

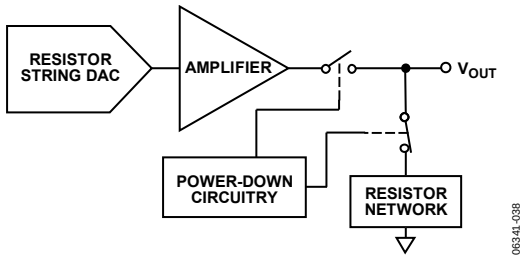

Figure 70. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry are shut down when power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 4 µs for V_{DD} = 5 V or V_{DD} = 3 V.

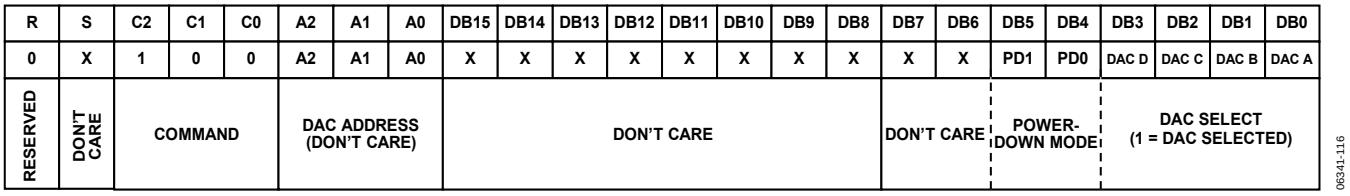

Figure 71. Power-Up/Power-Down Command

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POWER-ON RESET AND SOFTWARE RESET

The AD5625R/AD5645R/AD5665R and AD5625/AD5665 contain a power-on reset circuit that controls the output voltage during power-up. The 10-lead version of the device powers up to 0 V. The 14-lead version has a power-on reset (POR) pin that allows the output voltage to be selected. By connecting the POR pin to GND, the AD5625R/AD5645R/AD5665R and AD5625/AD5665 output powers up to 0 V; by connecting the POR pin to V_{DD}, the AD5625R/AD5645R/AD5665R and AD5625/AD5665 output powers up to midscale. The output remains powered up at this level until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

Any events on $\overline{\text{LDAC}}$ or $\overline{\text{CLR}}$ during power-on reset are ignored.

There is also a software reset function. Command 101 is the software reset command. The software reset command contains two reset modes that are software programmable by setting bit DB0 in the input shift register.

Table 16 shows how the state of the bit corresponds to the software reset modes of operation of the devices. Figure 72 shows the contents of the input shift register during the software reset mode of operation.

Table 16. Software Reset Modes for the AD5625R/AD5645R/AD5665R and AD5625/AD5665

DB0	Registers Reset to Zero
0	DAC register
	Input shift register
1 (Power-On Reset)	DAC register
	Input shift register
	$\overline{\text{LDAC}}$ register
	Power-down register
	Internal reference setup register

INTERNAL REFERENCE SETUP (R VERSIONS)

The on-chip reference is off at power-up by default. It can be turned on by sending the reference setup command (111) and setting DB0 in the input shift register. Table 17 shows how the state of the bit corresponds to the mode of operation.

Table 17. Reference Setup Command

DB0	Action
0	Internal reference off (default)
1	Internal reference on

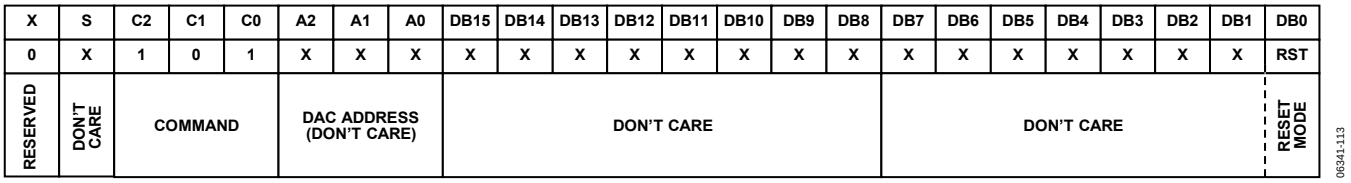

Figure 72. Reset Command

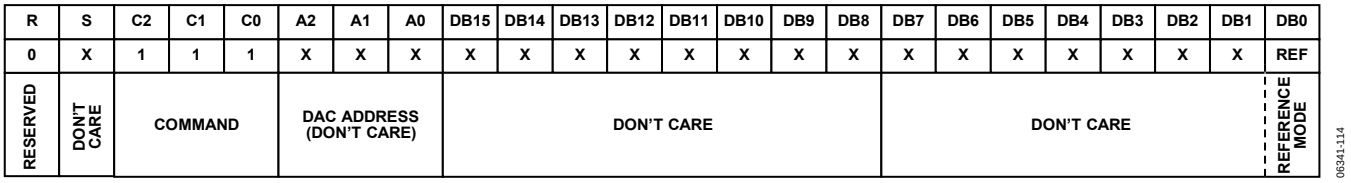

Figure 73. Reference Setup Command

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APPLICATIONS INFORMATION

USING A REFERENCE AS A POWER SUPPLY FOR THE AD5625R/AD5645R/AD5665R AND AD5625/AD5665

Because the supply current required by the AD5625R/AD5645R/AD5665R and AD5625/AD5665 is extremely low, an alternative option is to use a voltage reference to supply the required voltage to the device (see Figure 74). This is especially useful if the power supply is noisy or if the system supply voltages are at some value other than 5 V or 3 V, for example, 15 V. The voltage reference outputs a steady supply voltage for the AD5625R/AD5645R/AD5665R and AD5625/AD5665. If the low dropout REF195 is used, it must supply 450 µA of current to the AD5625R/AD5645R/AD5665R and AD5625/AD5665 with no load on the output of the DAC. When the DAC output is loaded, the REF195 also must supply the current to the load. The total current required (with a 5 kΩ load on the DAC output) is

1 mA + (5 V/5 kΩ) = 2 mA

The load regulation of the REF195 is typically 2 ppm/mA, resulting in a 4 ppm (20 µV) error for the 2 mA current drawn from it. This corresponds to a 0.263 LSB error.

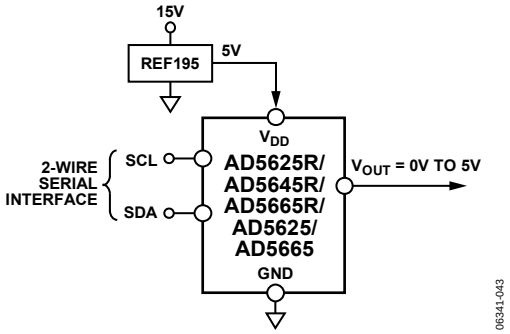

Figure 74. REF195 as Power Supply to the AD5625R/AD5645R/ AD5665R and AD5625/AD5665

BIPOLAR OPERATION USING THE AD5625R/ AD5645R/AD5665R AND AD5625/AD5665

The AD5625R/AD5645R/AD5665R and AD5625/AD5665 have been designed for single-supply operation, but a bipolar output range is also possible using the circuit shown in Figure 75. The circuit gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{DD} \times \left(\frac{D}{65{,}536} \right) \times \left(\frac{R1 + R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0 to 65,535).

If V_{DD} = 5 V, R1 = R2 = 10 kΩ,

$$V_O = \left(\frac{10 \times D}{65{,}536} \right) - 5 \text{ V}$$

This is an output voltage range of ±5 V, with 0x0000 corresponding to a −5 V output and 0xFFFF corresponding to a +5 V output.

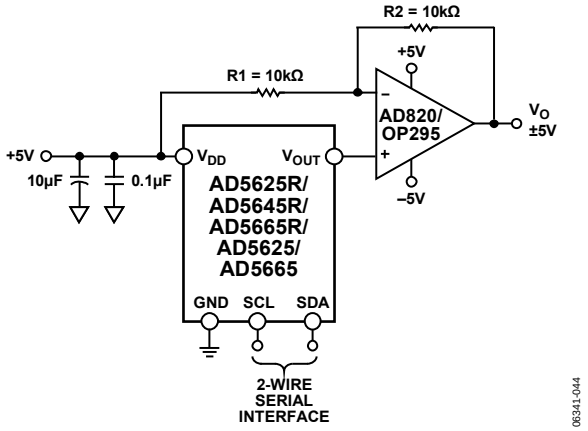

Figure 75. Bipolar Operation with the AD5625R/AD5645R/AD5665R and AD5625/AD5665

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5625R/AD5645R/AD5665R and AD5625/AD5665 should have separate analog and digital sections, each having its own area of the board. If the AD5625R/AD5645R/AD5665R and AD5625/AD5665 are in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5625R/AD5645R/AD5665R and AD5625/AD5665.

The power supply to the AD5625R/AD5645R/AD5665R and AD5625/AD5665 should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should be located as close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitor is the tantalum bead type. It is important that the 0.1 µF capacitor have low effective series resistance (ESR) and low effective series inductance (ESI), for example, common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and to reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only, and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

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OUTLINE DIMENSIONS

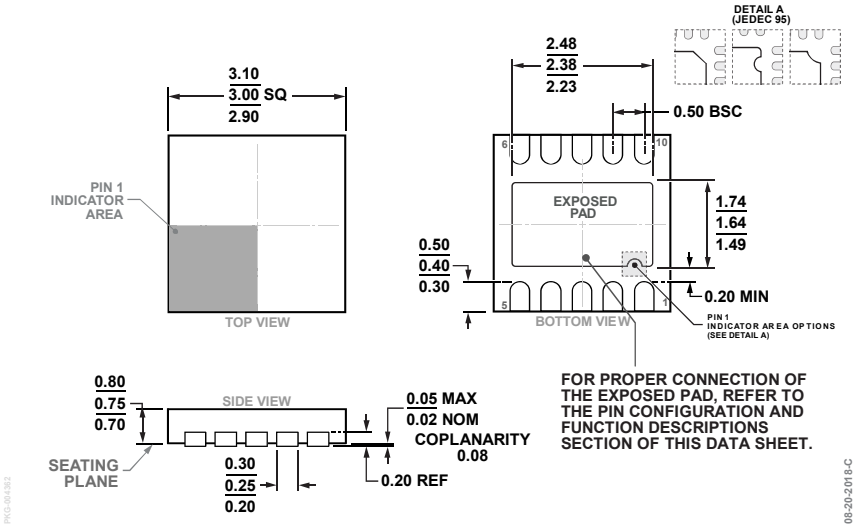
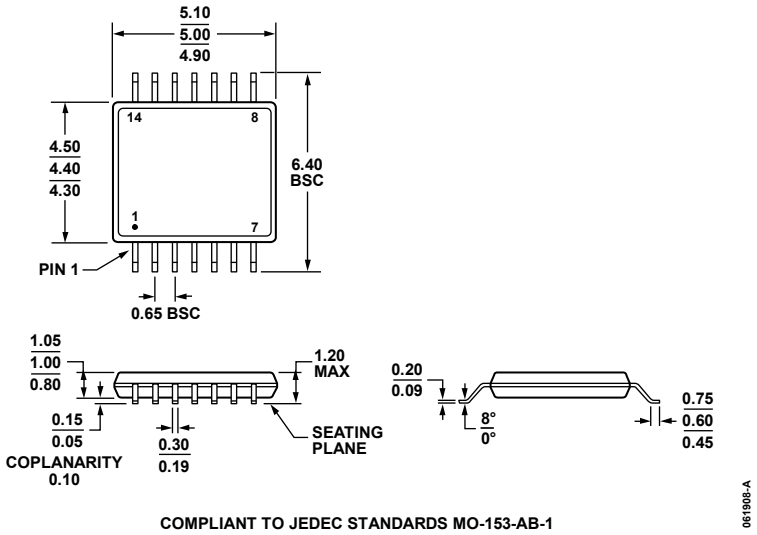


Figure 76. 10-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-10-9)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 77. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

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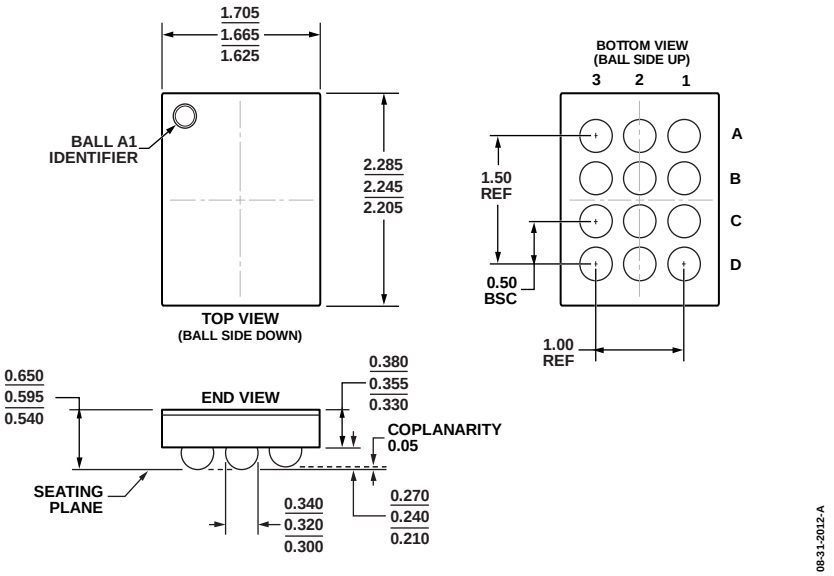

Figure 78. 12-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-12-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Accuracy	On-Chip Reference	Maximum I²C Speed	Package Description	Package Option	Marking Code
AD5625BCPZ-R2	−40°C to +105°C	±1 LSB INL	None	400 kHz	10-Lead LFCSP	CP-10-9	D8V
AD5625BCPZ-REEL7	−40°C to +105°C	±1 LSB INL	None	400 kHz	10-Lead LFCSP	CP-10-9	D8V
AD5625BRUZ	−40°C to +105°C	±1 LSB INL	None	400 kHz	14-Lead TSSOP	RU-14	
AD5625BRUZ-REEL7	−40°C to +105°C	±1 LSB INL	None	400 kHz	14-Lead TSSOP	RU-14	
AD5625RBCPZ-R2	−40°C to +105°C	±1 LSB INL	1.25 V	400 kHz	10-Lead LFCSP	CP-10-9	D8S
AD5625RBCPZ-REEL7	−40°C to +105°C	±1 LSB INL	1.25 V	400 kHz	10-Lead LFCSP	CP-10-9	D8S
AD5625RACPZ-REEL7	−40°C to +105°C	±4 LSB INL	1.25 V	400 kHz	10-Lead LFCSP	CP-10-9	DEU
AD5625RBRUZ-1	−40°C to +105°C	±1 LSB INL	2.5 V	400 kHz	14-Lead TSSOP	RU-14	
AD5625RBRUZ-1REEL7	−40°C to +105°C	±1 LSB INL	2.5 V	400 kHz	14-Lead TSSOP	RU-14	
AD5625RBRUZ-2	−40°C to +105°C	±1 LSB INL	2.5 V	3.4 MHz	14-Lead TSSOP	RU-14	
AD5625RBRUZ-2REEL7	−40°C to +105°C	±1 LSB INL	2.5 V	3.4 MHz	14-Lead TSSOP	RU-14	
AD5645RBCPZ-R2	−40°C to +105°C	±4 LSB INL	1.25 V	400 kHz	10-Lead LFCSP	CP-10-9	D89
AD5645RBCPZ-REEL7	−40°C to +105°C	±4 LSB INL	1.25 V	400 kHz	10-Lead LFCSP	CP-10-9	D89
AD5645RBRUZ	−40°C to +105°C	±4 LSB INL	2.5 V	400 kHz	14-Lead TSSOP	RU-14	
AD5645RBRUZ-REEL7	−40°C to +105°C	±4 LSB INL	2.5 V	400 kHz	14-Lead TSSOP	RU-14	
AD5665BCPZ-R2	−40°C to +105°C	±16 LSB INL	None	400 kHz	10-Lead LFCSP	CP-10-9	D6U
AD5665BCPZ-REEL7	−40°C to +105°C	±16 LSB INL	None	400 kHz	10-Lead LFCSP	CP-10-9	D6U
AD5665BRUZ	−40°C to +105°C	±16 LSB INL	None	400 kHz	14-Lead TSSOP	RU-14	
AD5665BRUZ-REEL7	−40°C to +105°C	±16 LSB INL	None	400 kHz	14-Lead TSSOP	RU-14	
AD5665RBCBZ-1-RL7	−40°C to +105°C	±16 LSB INL	1.25 V	400 kHz	12-Ball WLCSP	CB-12-9	
AD5665RBCPZ-R2	−40°C to +105°C	±16 LSB INL	1.25 V	400 kHz	10-Lead LFCSP	CP-10-9	DA2
AD5665RBCPZ-REEL7	−40°C to +105°C	±16 LSB INL	1.25 V	400 kHz	10-Lead LFCSP	CP-10-9	DA2
AD5665RBRUZ-1	−40°C to +105°C	±16 LSB INL	2.5 V	400 kHz	14-Lead TSSOP	RU-14	
AD5665RBRUZ-1REEL7	−40°C to +105°C	±16 LSB INL	2.5 V	400 kHz	14-Lead TSSOP	RU-14	
AD5665RBRUZ-2	−40°C to +105°C	±16 LSB INL	2.5 V	3.4 MHz	14-Lead TSSOP	RU-14	
AD5665RBRUZ-2REEL7	−40°C to +105°C	±16 LSB INL	2.5 V	3.4 MHz	14-Lead TSSOP	RU-14	

[1] Z = RoHS Compliant Part.

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NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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