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REVISION HISTORY

8/2016—Rev. 0 to Rev. A

Change to Minimum $\overline{\text{SYNC}}$ High Times (Single Channel Update) Parameter and Minimum $\overline{\text{SYNC}}$ High Time (All Channel Update) Parameter, Table 4 ... 5

10/2008—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 4.5 V to 5.5 V, R_L = 5 kΩ to GND, C_L = 200 pF to GND, 2.5 V ≤ V_{REFIN} ≤ V_{DD}, unless otherwise specified. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

	B Grade[1]			A Grade[1, 2]				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
STATIC PERFORMANCE[3]								
Resolution								
AD5065	16			16			Bits	
AD5045	14							
AD5025	12							
Relative Accuracy								
AD5065		±0.4	±1		±0.5	±4	LSB	T_A = −40°C to +105°C
AD5065		+0.4	±2		±0.5	±4		T_A = −40°C to +125°C
AD5045		±0.1	±0.5				LSB	T_A = −40°C to +105°C
AD5045		±0.1	±1					T_A = −40°C to +125°C
AD5025		±0.05	±0.25				LSB	T_A = −40°C to +105°C
AD5025		±0.05	±0.5					T_A = −40°C to +125°C
Differential Nonlinearity		±0.2	±1		±0.2	±1	LSB	
Total Unadjusted Error		±0.2	±2.5		±0.2	±2.5	mV	V_{REF} = 2.5 V; V_{DD} = 5.5 V
Offset Error		±0.2	±1.8		±0.2	±1.8	mV	Code 512 (AD5065), Code 128 (AD5045), Code 32 (AD5025) loaded to DAC register
Offset Error Drift[4]		±2			±2		µV/°C	
Full-Scale Error		±0.01	±0.07		±0.01	±0.07	% FSR	All 1s loaded to DAC register, $V_{REF} < V_{DD}$
Gain Error		±0.005	±0.05		±0.005	±0.05	% FSR	
Gain Temperature Coefficient[4]		±1			±1		ppm	Of FSR/°C
DC Crosstalk[4]			40			40	µV	Due to single channel full-scale output change, R_L = 5 kΩ to GND or V_{DD}
			40			40	µV/mA	Due to load current change
			40			40	µV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS[4]								
Output Voltage Range	0		V_{DD}	0		V_{DD}	V	
Capacitive Load Stability			1			1	nF	R_L = 5 kΩ, R_L = 100 kΩ, and R_L = ∞
DC Output Impedance								
Normal Mode		0.5			0.5		Ω	
Power-Down Mode								
Output Connected to 100 kΩ Network		100			100		kΩ	Output impedance tolerance ± 400 Ω
Output Connected to 1 kΩ Network		1			1		kΩ	Output impedance tolerance ± 20 Ω
Short-Circuit Current		60			60		mA	DAC = full scale, output shorted to GND
		45			45		mA	DAC = zero-scale, output shorted to V_{DD}
Power-Up Time		4.5			4.5		µs	Time to exit power-down mode to normal mode of AD5024/AD5044/AD5064, 32nd clock edge to 90% of DAC midscale value, output unloaded
DC PSRR		−92			−92		dB	V_{DD} ± 10%, DAC = full scale, $V_{REF} < V_{DD}$
REFERENCE INPUTS								
Reference Input Range	2.2		V_{DD}	2.2		V_{DD}	V	
Reference Current		35	50		35	50	µA	Per DAC channel
Reference Input Impedance		120			120		kΩ	

Parameter	B Grade[1] Min	B Grade[1] Typ	B Grade[1] Max	A Grade[1, 2] Min	A Grade[1, 2] Typ	A Grade[1, 2] Max	Unit	Conditions/Comments
LOGIC INPUTS								
Input Current[5]			±1			±1	μA	
Input Low Voltage, V_{INL}			0.8			0.8	V	
Input High Voltage, V_{INH}	2.2			2.2			V	
Pin Capacitance[4]		4			4		pF	
LOGIC OUTPUTS (SDO)[3, 4]								
Output Low Voltage, V_{OL}			0.4			0.4	V	I_{SINK} = 2 mA
Output High Voltage, V_{OH}	V_{DD} − 1			V_{DD} − 1				I_{SOURCE} = 2 mA
High Impedance Leakage Current[4]		±0.002	±1		±0.002	±1	μA	
High Impedance Output Capacitance		7			7		pF	
POWER REQUIREMENTS								
V_{DD}	4.5		5.5	4.5		5.5	V	
I_{DD}[6]								DAC active, excludes load current
Normal Mode		2.2	2.7		2.2	2.7	mA	$V_{IH} = V_{DD}$ and V_{IL} = GND
All Power-Down Modes[7]		0.4	2		0.4	2	μA	T_A = −40°C to +105°C
			30			30	μA	T_A = −40°C to +125°C

[1] Temperature range is −40°C to +125°C, typical at 25°C.
[2] A grade offered in AD5065 only.
[3] Linearity calculated using a reduced code range—AD5065: Code 512 to Code 65,024; AD5045: Code 128 to Code 16,256; AD5025: Code 32 to Code 4064. Output unloaded.
[4] Guaranteed by design and characterization; not production tested.
[5] Current flowing into or out of individual digital pins.
[6] Interface inactive. All DACs active. DAC outputs unloaded.
[7] Both DACs powered down.

AC CHARACTERISTICS

V_{DD} = 4.5 V to 5.5 V, R_L = 5 kΩ to GND, C_L = 200 pF to GND, 2.5 V ≤ V_{REFIN} ≤ V_{DD}. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments[2]
Output Voltage Settling Time		5.8	8	μs	¼ to ¾ scale settling to ±1 LSB, R_L = 5 kΩ single-channel update including DAC calibration sequence
Output Voltage Settling Time		10.7	13	μs	¼ to ¾ scale settling to ±1 LSB, R_L = 5 kΩ all channel update including DAC calibration sequence
Slew Rate		1.5		V/μs	
Digital-to-Analog Glitch Impulse[3]		4		nV-sec	1 LSB change around major carry
Reference Feedthrough[3]		−90		dB	V_{REF} = 3 V ± 0.86 V p-p, frequency = 100 Hz to 100 kHz
SDO Feedthrough		0.07		nV-sec	Daisy-chain mode; SDO load is 10 pF
Digital Feedthrough[3]		0.1		nV-sec	
Digital Crosstalk[3]		1.9		nV-sec	
Analog Crosstalk[3]		1.2		nV-sec	
DAC-to-DAC Crosstalk[3]		2.1		nV-sec	
Multiplying Bandwidth[3]		340		kHz	V_{REF} = 3 V ± 0.86 V p-p
Total Harmonic Distortion[3]		−80		dB	V_{REF} = 3 V ± 0.86 V p-p, frequency = 10 kHz
Output Noise Spectral Density		64		nV/√Hz	DAC code = 0x8400, 1 kHz
		60		nV/√Hz	DAC code = 0x8400, 10 kHz
Output Noise		6		μV p-p	0.1 Hz to 10 Hz

[1] Guaranteed by design and characterization; not production tested.
[2] Temperature range is −40°C to + 125°C, typical at 25°C.
[3] See the Terminology section.

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 3 and Figure 4. V_{DD} = 4.5 V to 5.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Cycle Time	t_1[1]	20			ns
SCLK High Time	t_2	10			ns
SCLK Low Time	t_3	10			ns
$\overline{SYNC}$ to SCLK Falling Edge Setup Time	t_4	16.5			ns
Data Setup Time	t_5	5			ns
Data Hold Time	t_6	5			ns
SCLK Falling Edge to $\overline{SYNC}$ Rising Edge	t_7	0		30	ns
Minimum $\overline{SYNC}$ High Time (Single Channel Update)	t_8	3			µs
Minimum $\overline{SYNC}$ High Time (All Channel Update)	t_8	8			µs
$\overline{SYNC}$ Rising Edge to SCLK Fall Ignore	t_9	17			ns
$\overline{LDAC}$ Pulse Width Low	t_{10}	20			ns
SCLK Falling Edge to $\overline{LDAC}$ Rising Edge	t_{11}	20			ns
$\overline{CLR}$ Pulse Width Low	t_{12}	10			ns
SCLK Falling Edge to $\overline{LDAC}$ Falling Edge	t_{13}	10			ns
$\overline{CLR}$ Pulse Activation Time	t_{14}	10.6			µs
SCLK Rising Edge to SDO Valid	t_{15}[2, 3]			22	ns
SCLK Falling Edge to $\overline{SYNC}$ Rising Edge	t_{16}[2]	5		30	ns
$\overline{SYNC}$ Rising Edge to SCLK Rising Edge	t_{17}[2]	8			ns
$\overline{SYNC}$ Rising Edge to $\overline{LDAC}$/$\overline{CLR}$/$\overline{PDL}$ Falling Edge (Single Channel Update)	t_{18}[2]	2			µs
$\overline{SYNC}$ Rising Edge to $\overline{LDAC}$/$\overline{CLR}$/$\overline{PDL}$ Falling Edge (All Channel Update)	t_{18}[2]	4			µs
$\overline{PDL}$ Minimum Pulse Width	t_{19}	20			ns

[1] Maximum SCLK frequency is 50 MHz at V_{DD} = 4.5 V to 5.5 V. Guaranteed by design and characterization; not production tested.
[2] Daisy-chain mode only.
[3] Measured with the load circuit of Figure 2. t_{15} determines the maximum SCLK frequency in daisy-chain mode.

Circuit and Timing Diagrams

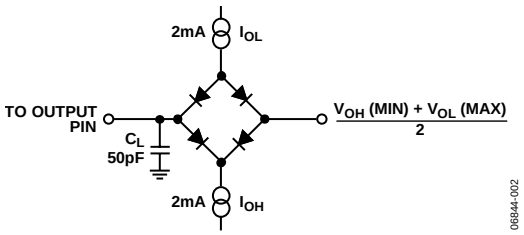
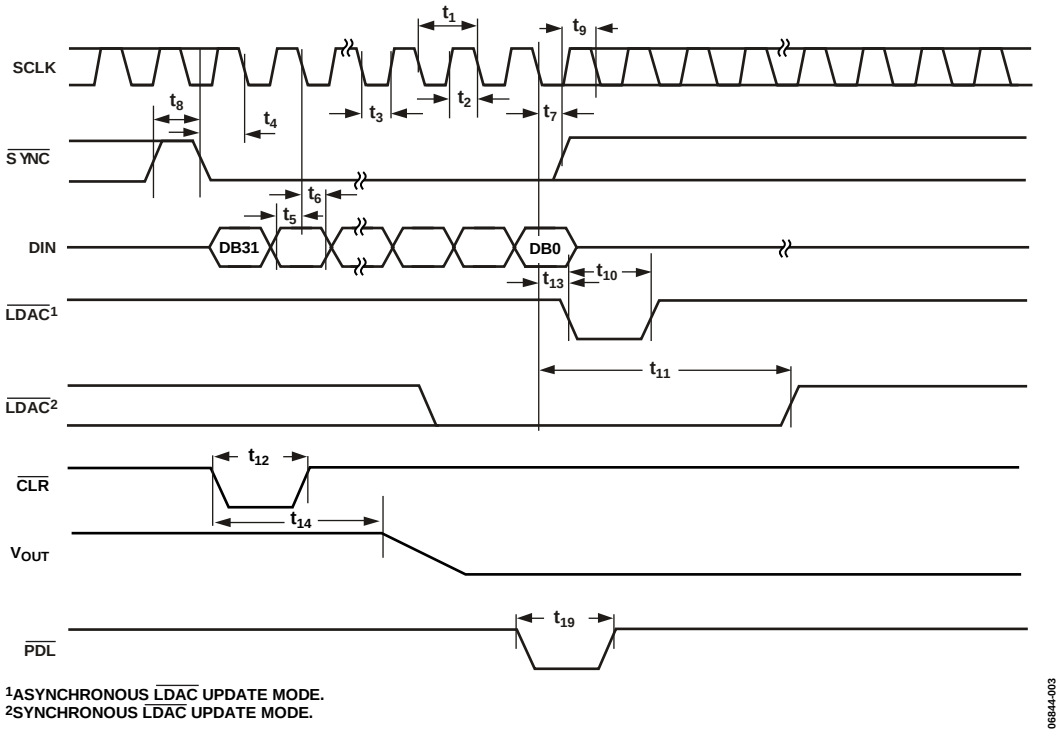
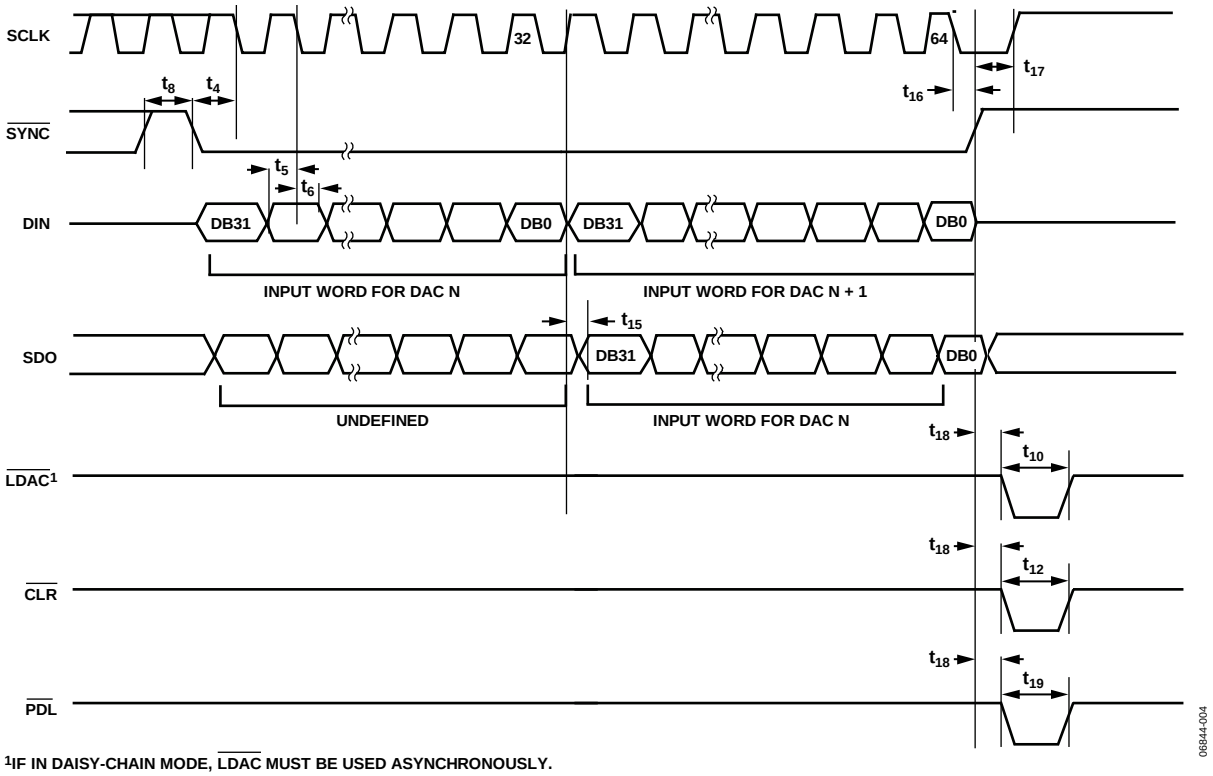


Figure 2. Load Circuit for Digital Output (SDO) Timing Specifications



[1]ASYNCHRONOUS LDAC UPDATE MODE.
[2]SYNCHRONOUS LDAC UPDATE MODE.

Figure 3. Serial Write Operation



[1]IF IN DAISY-CHAIN MODE, LDAC MUST BE USED ASYNCHRONOUSLY.

Figure 4. Daisy-Chain Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
$V_{OUT}A$ or $V_{OUT}B$ to GND	−0.3 V to V_{DD} + 0.3 V
$V_{REF}A$ or $V_{REF}B$ to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range, Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\ MAX}$)	150°C
Power Dissipation	$(T_{J\ MAX} - T_A)/\theta_{JA}$
θ_{JA} Thermal Impedance	150.4°C/W
Reflow Soldering Peak Temperature	
SnPb	240°C
Pb-Free	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

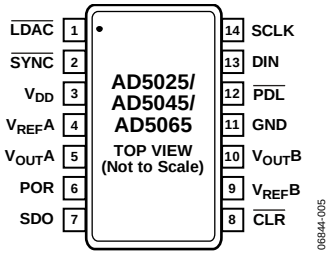


Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{LDAC}}$	Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to simultaneously update. This pin can be tied permanently low in standalone mode. When daisy-chain mode is enabled, this pin cannot be tied permanently low. The $\overline{\text{LDAC}}$ pin should be used in asynchronous $\overline{\text{LDAC}}$ update mode, as shown in Figure 3, and the $\overline{\text{LDAC}}$ pin must be brought high after pulsing. This allows all DAC outputs to simultaneously update.
2	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and enables the input register. Data is transferred in on the falling edges of the next 32 clocks. If $\overline{\text{SYNC}}$ is taken high before the 32nd falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the device.
3	V_{DD}	Power Supply Input. These parts can be operated from 4.5 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	$V_{REF}A$	DAC A Reference Input. This is the reference voltage input pin for DAC A.
5	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
6	POR	Power-On Reset Pin. Tying this pin to GND powers up the part to 0 V. Tying this pin to V_{DD} powers up the part to midscale.
7	SDO	Serial Data Output. Can be used for daisy-chaining a number of these devices together or for reading back the data in the shift register for diagnostic purposes. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock.
8	$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling edge sensitive. When $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, the input register and the DAC register are updated with the data contained in the clear code register—zero, midscale, or full scale. Default setting clears the output to 0 V.
9	$V_{REF}B$	DAC B Reference Input. This is the reference voltage input pin for DAC B.
10	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
11	GND	Ground Reference Point for All Circuitry on the Part.
12	$\overline{\text{PDL}}$	The $\overline{\text{PDL}}$ pin is used to ensure hardware shutdown lockout of the device under any circumstance. A Logic 1 at the $\overline{\text{PLO}}$ pin causes the device to behave as normal. The user may successfully enter software power-down over the serial interface while Logic 1 is applied to the $\overline{\text{PDL}}$ pin. If a Logic 0 is applied to this pin, it ensures that the device cannot enter software power-down under any circumstances. If the device had previously been placed in software power-down mode, a high-to-low transition at the $\overline{\text{PDL}}$ pin causes the DAC(s) to exit power-down and output a voltage corresponding to the previous code in the DAC register before the device entered software power-down.
13	DIN	Serial Data Input. This device has a 32-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
14	SCLK	Serial Clock Input. Data is clocked into the input register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.

TYPICAL PERFORMANCE CHARACTERISTICS

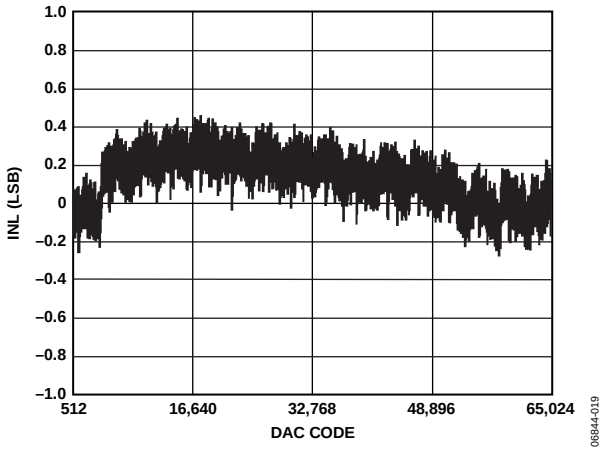


Figure 6. AD5065 INL

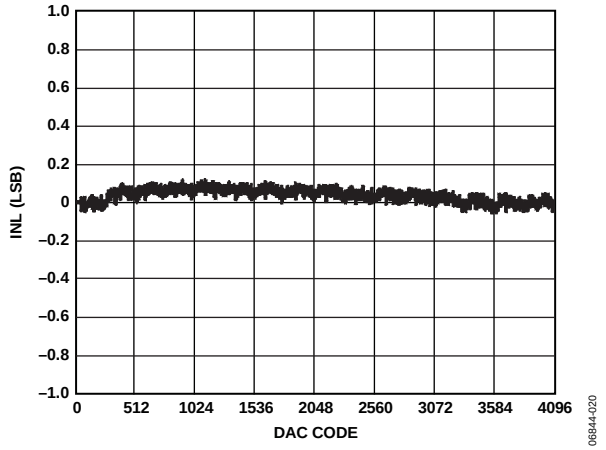


Figure 7. AD5045 INL

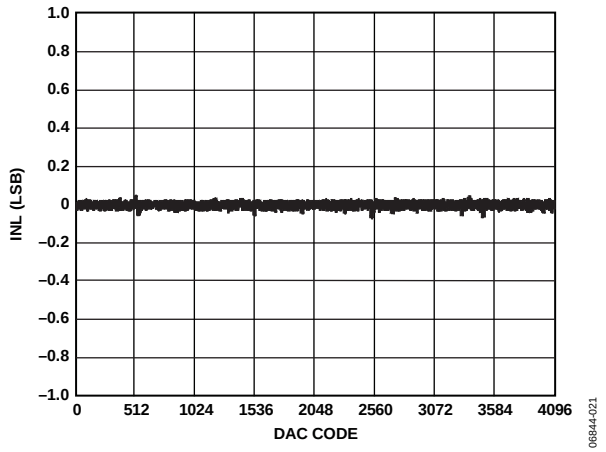


Figure 8. AD5025 INL

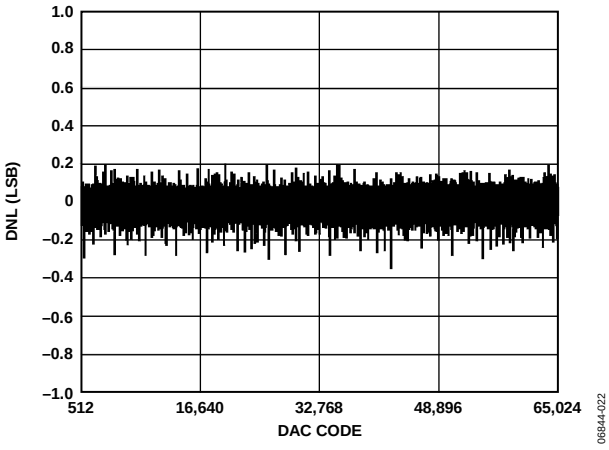


Figure 9. AD5065 DNL

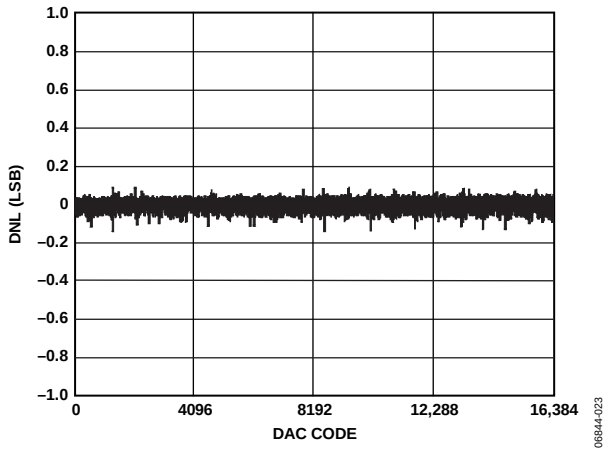


Figure 10. AD5045 DNL

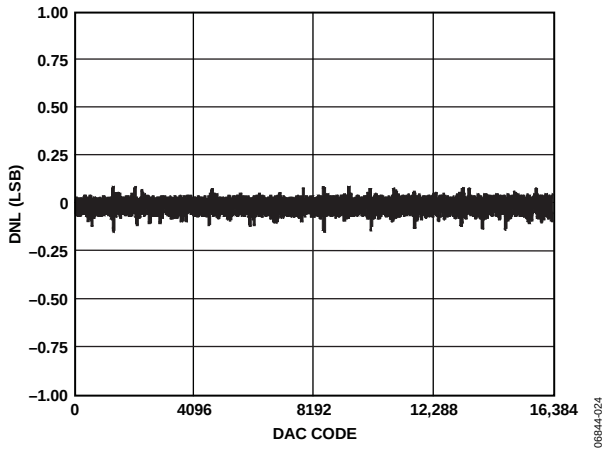


Figure 11. AD5025 DNL

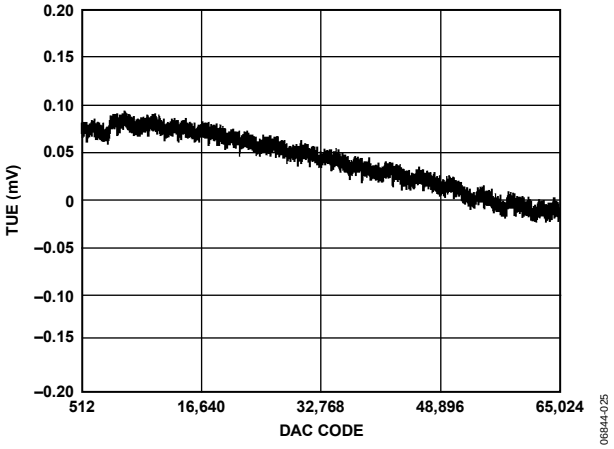


Figure 12. Total Unadjusted Error (TUE) vs. DAC Code

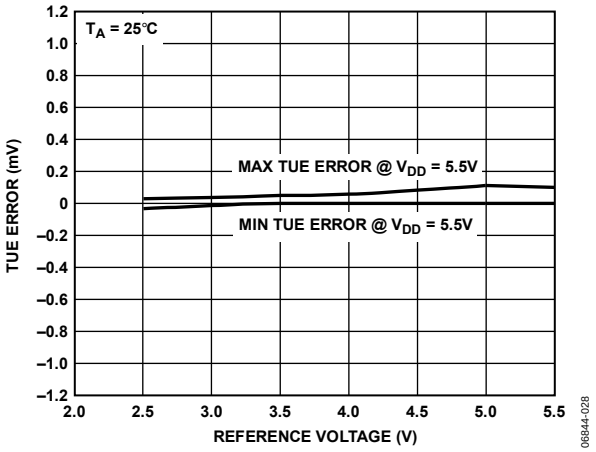


Figure 15. Total Unadjusted Error (TUE) vs. Reference Input Voltage

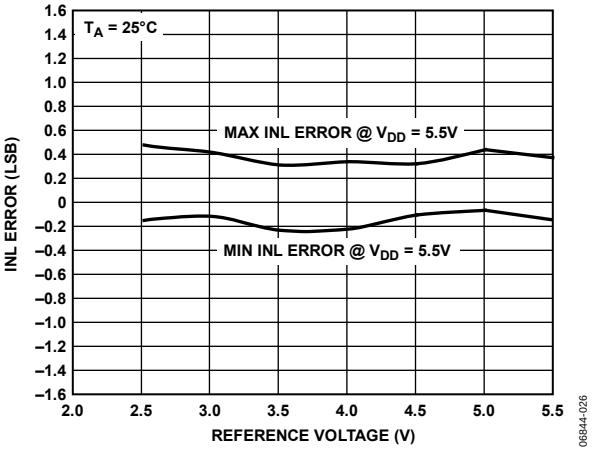


Figure 13. INL vs. Reference Input Voltage

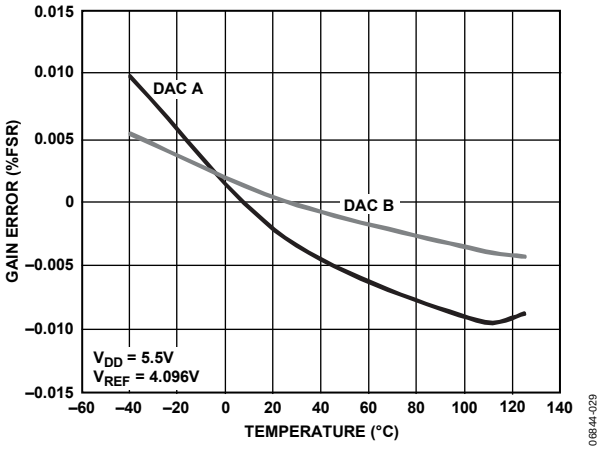


Figure 16. Gain Error vs. Temperature

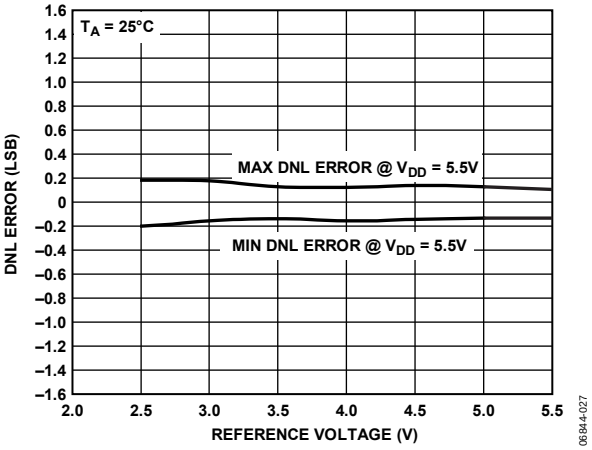


Figure 14. DNL vs. Reference Input Voltage

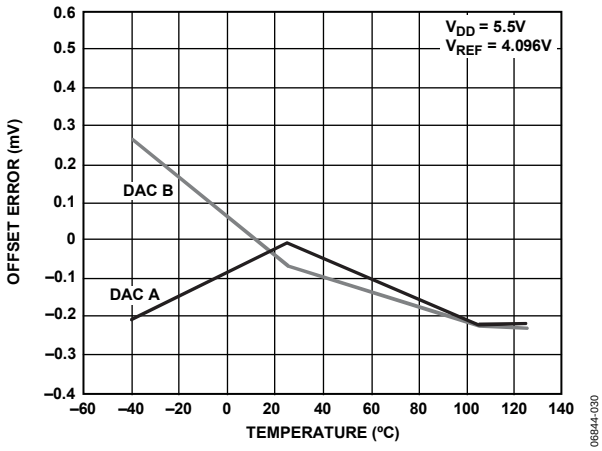


Figure 17. Offset Error vs. Temperature

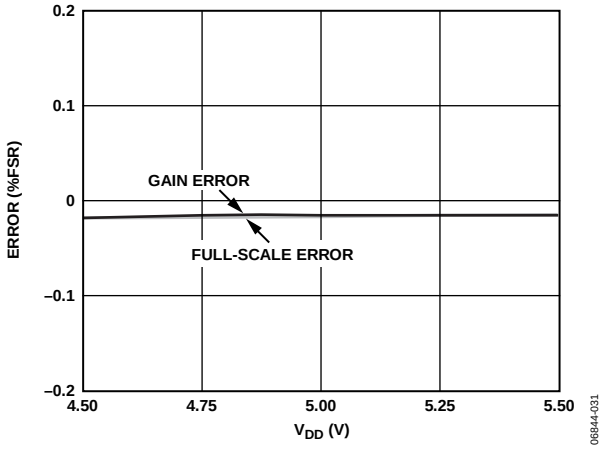


Figure 18. Gain Error and Full-Scale Error vs. Supply Voltage

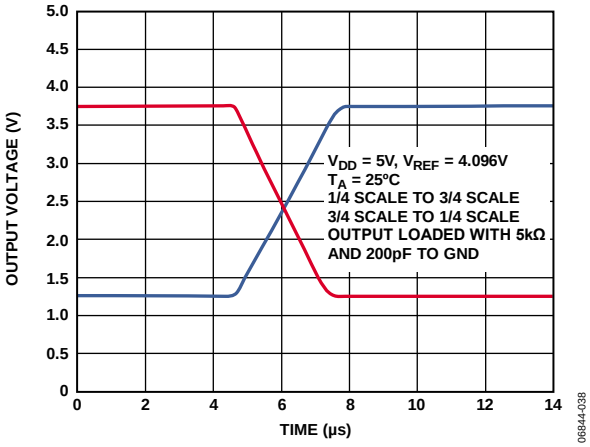


Figure 21. Settling Time and Typical Output Slew Rate

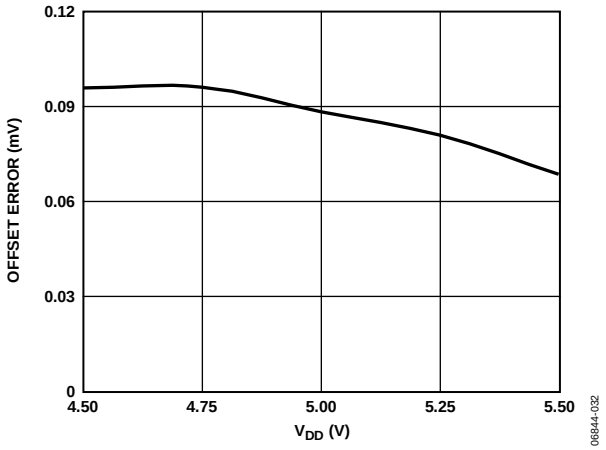


Figure 19. Offset Error Voltage vs. Supply Voltage

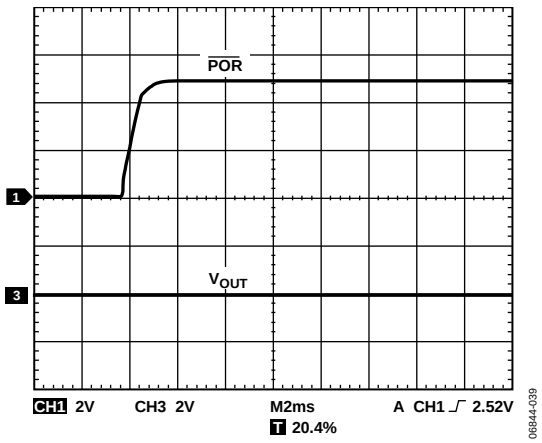


Figure 22. Power-On Reset to 0 V

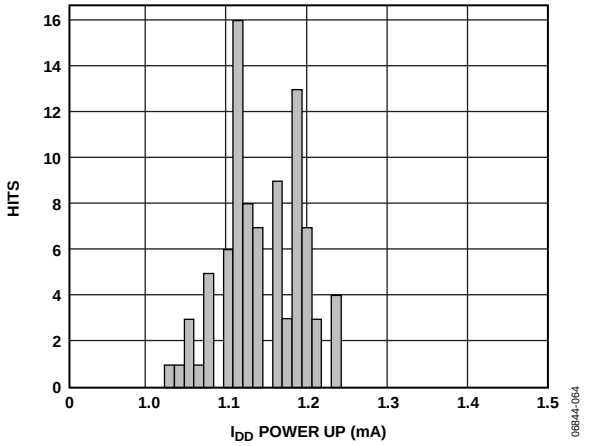


Figure 20. I_{DD} Histogram, V_{DD} = 5.0 V

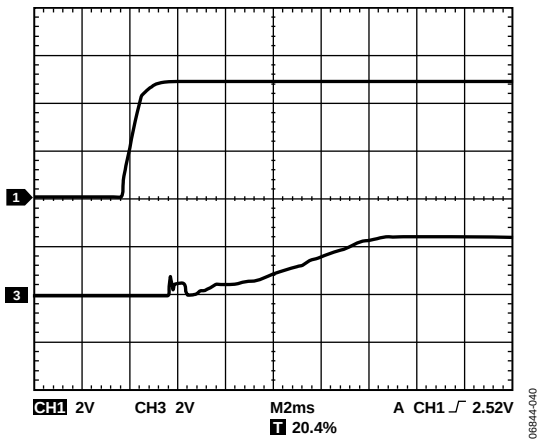


Figure 23. Power-On Reset to Midscale

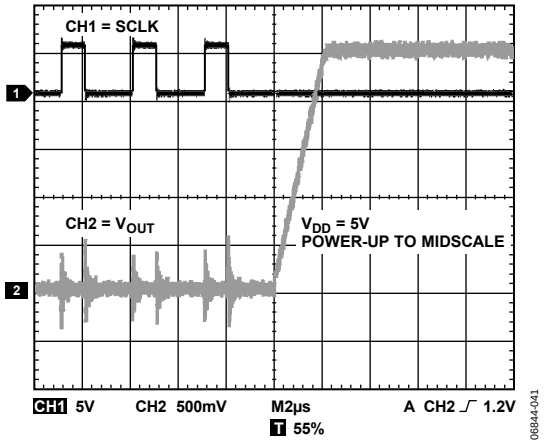


Figure 24. Exiting Power-Down to Midscale

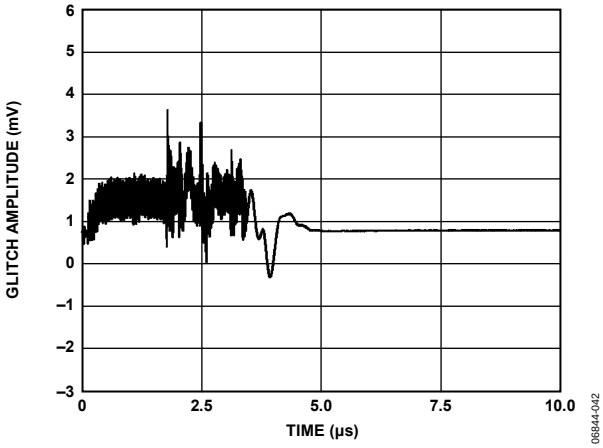


Figure 25. Digital-to-Analog Glitch Impulse

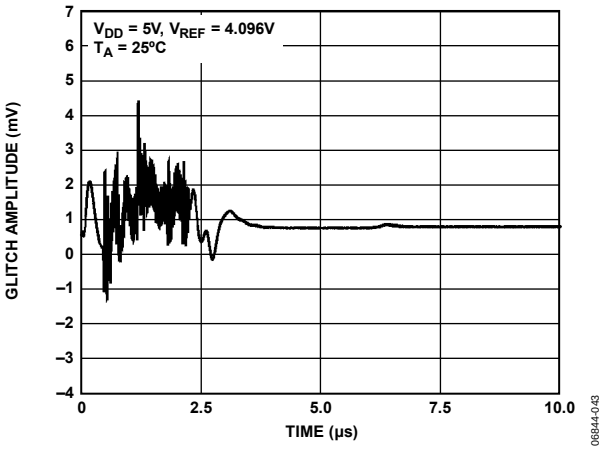


Figure 26. Analog Crosstalk

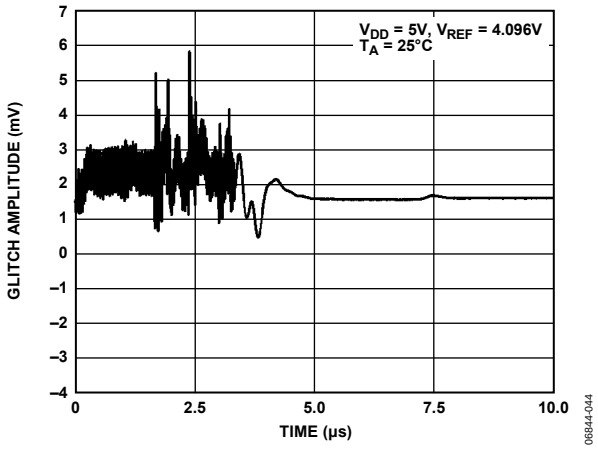


Figure 27. DAC-to-DAC Crosstalk

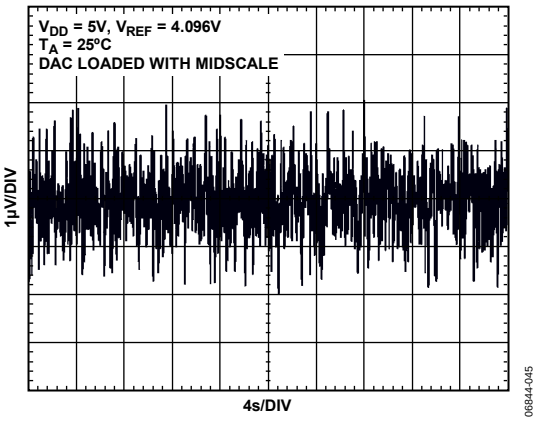


Figure 28. 0.1 Hz to 10 Hz Output Noise Plot

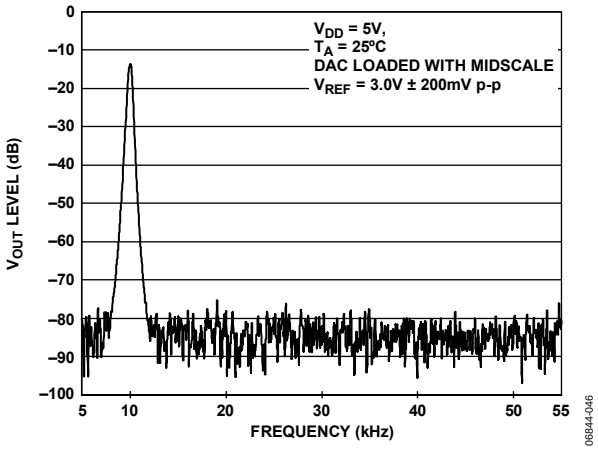


Figure 29. Total Harmonic Distortion

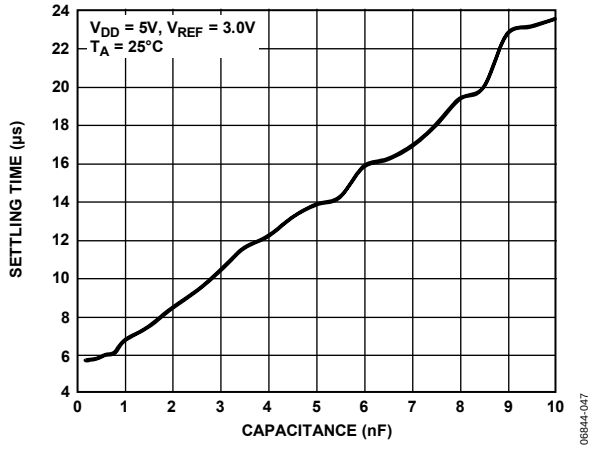


Figure 30. Settling Time vs. Capacitive Load

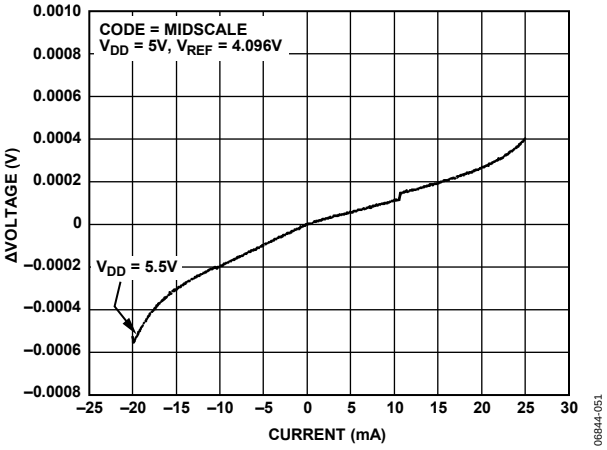


Figure 33. Typical Output Load Regulation

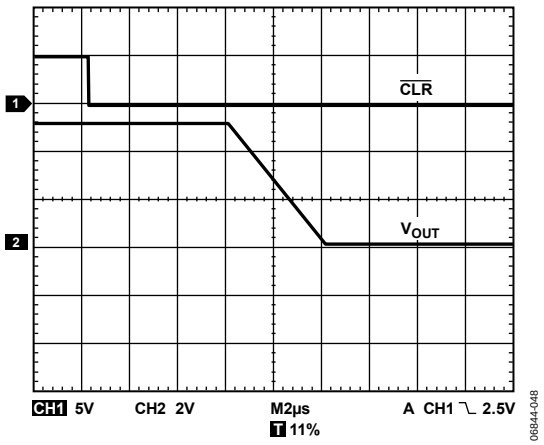


Figure 31. Hardware $\overline{CLR}$

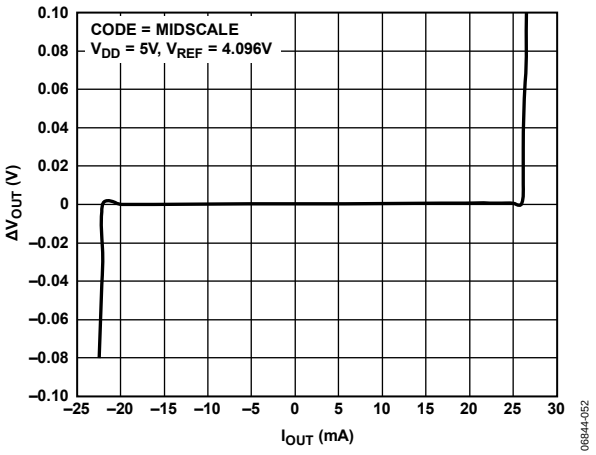


Figure 34. Typical Current Limiting Plot

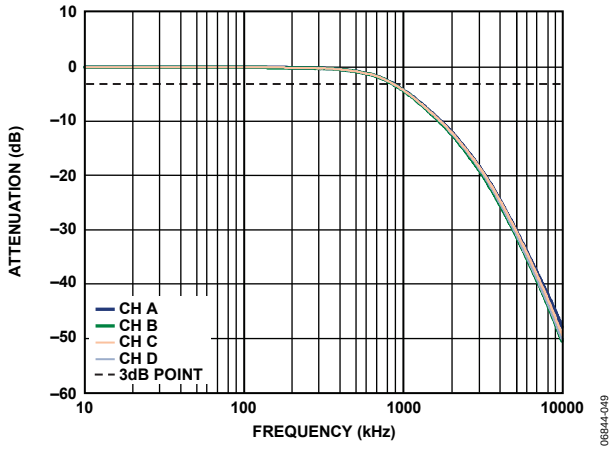


Figure 32. Multiplying Bandwidth

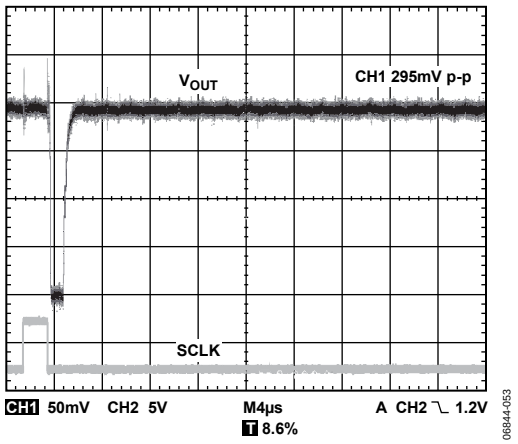


Figure 35. Glitch Upon Entering Power-Down (1 kΩ to GND) from Zero Scale, No Load

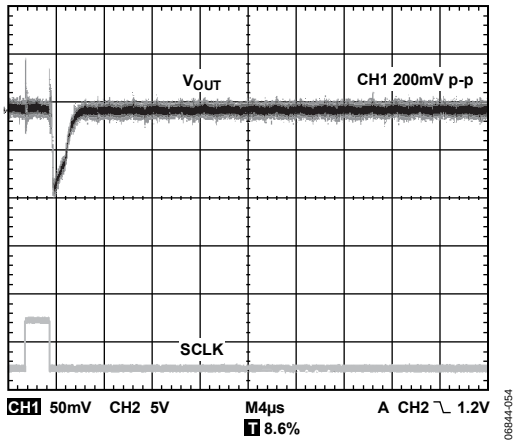


Figure 36. Glitch Upon Entering Power-Down (1 kΩ to GND) from Zero Scale, 5 kΩ/200 pF Load

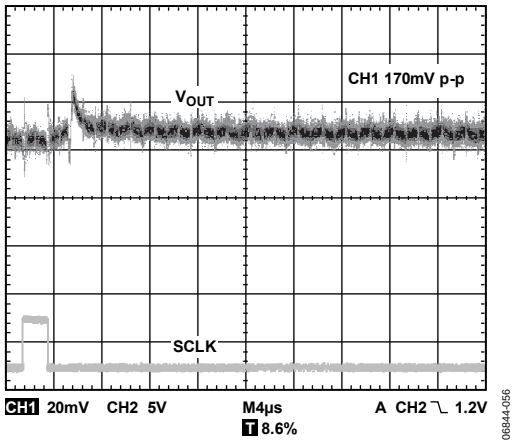


Figure 38. Glitch Upon Exiting Power-Down (1 kΩ to GND) to Zero Scale, 5 kΩ/200 pF Load

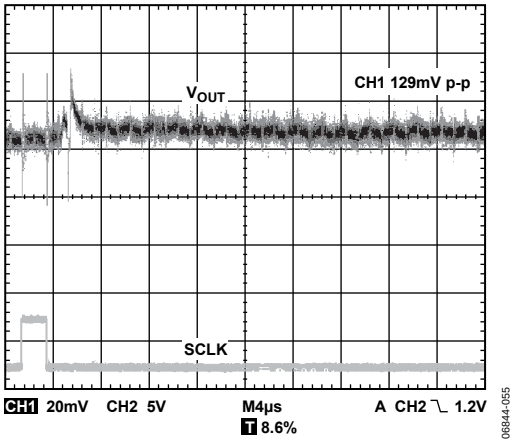


Figure 37. Glitch Upon Exiting Power-Down (1 kΩ to GND) to Zero Scale, No Load

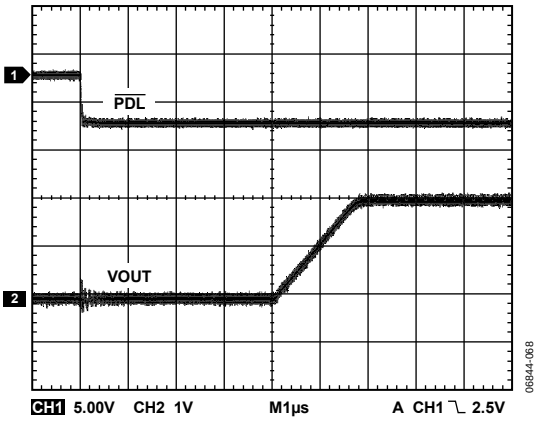


Figure 39. $\overline{PDL}$ Activation Time

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation in LSBs from a straight line passing through the endpoints of the DAC transfer function. Figure 6, Figure 7, and Figure 8 show plots of typical INL vs. code.

Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Figure 9, Figure 10, and Figure 11 show plots of typical DNL vs. code.

Offset Error
Offset error is a measure of the difference between the actual V_{OUT} and the ideal V_{OUT}, expressed in millivolts in the linear region of the transfer function. Offset error is measured on the part with Code 512 (AD5065), Code 128 (AD5045), and Code 32 (AD5025) loaded into the DAC register. It can be negative or positive and is expressed in millivolts.

Offset Error Drift
Offset error drift is a measure of the change in offset error with a change in temperature. It is expressed in microvolts per degree Celsius.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percentage of the full-scale range.

Gain Temperature Coefficient
Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in parts per million of full-scale range per degree Celsius. Measured with $V_{REF} < V_{DD}$.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (0xFFFF) is loaded into the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed as a percentage of the full-scale range.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nanovolt-seconds and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 25.

DC Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in decibels. V_{REF} is held at 2.5 V, and V_{DD} is varied ±10%. Measured with $V_{REF} < V_{DD}$.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in microvolts.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in microvolts per milliamp.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (that is, $\overline{\text{LDAC}}$ is high). It is expressed in decibels.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device but is measured when the DAC is not being written to ($\overline{\text{SYNC}}$ held high). It is specified in nanovolt-seconds. It is measured with one simultaneous data and clock pulse loaded to the DAC.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s or vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nanovolt-seconds.

Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s or vice versa) while keeping $\overline{\text{LDAC}}$ high, and then pulsing $\overline{\text{LDAC}}$ low and monitoring the output of the DAC whose digital code has not changed. The area of the glitch is expressed in nanovolt-seconds.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s or vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nanovolt-seconds.

Multiplying Bandwidth
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)
Total harmonic distortion is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output. It is measured in decibels.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER

The AD5025/AD5045/AD5065 are single 12-/14-/16-bit, serial input, voltage output DACs. The parts operate from supply voltages of 4.5 V to 5.5 V. Data is written to the AD5025/AD5045/AD5065 in a 32-bit word format via a 3-wire serial interface. The AD5025/AD5045/AD5065 incorporate a power-on reset circuit that ensures the DAC output powers up to a known output state. The devices also have a software power-down mode that reduces the typical current consumption to typically 400 nA.

Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by

$$V_{OUT} = V_{REFIN} \times \left(\frac{D}{2^N} \right)$$

where:
D is the decimal equivalent of the binary code that is loaded to the DAC register (0 to 65,535 for the 16-bit AD5065).
N is the DAC resolution.

DAC ARCHITECTURE

The DAC architecture of the AD5025/AD5045/AD5065 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 40. The four MSBs of the 16-bit data-word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either GND or a V_{REF} buffer output. The remaining 12 bits of the data-word drive Switch S0 to Switch S11 of a 12-bit voltage mode R-2R ladder network.

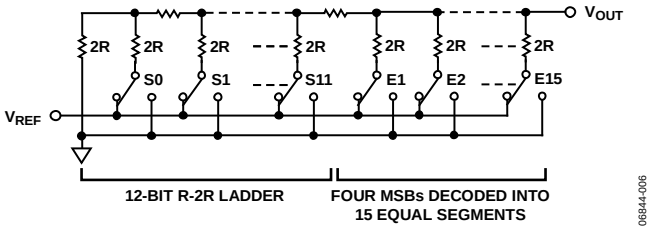


Figure 40. DAC Ladder Structure

REFERENCE BUFFER

The AD5025/AD5045/AD5065 operate with an external reference. Each DAC has a dedicated voltage reference pin and an on-chip reference buffer. The reference input pin has an input range of 2.5 V to V_{DD}. This input voltage is then used to provide a buffered reference for the DAC core.

OUTPUT AMPLIFIER

The on-chip output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. The amplifier is capable of driving a load of 5 k Ω parallel with 200 pF to GND. The slew rate is 1.5 V/µs with a ¼ to ¾ scale settling time of 13 µs.

SERIAL INTERFACE

The AD5025/AD5045/AD5065 have a 3-wire serial interface ($\overline{SYNC}$, SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards as well as most DSPs. See Figure 3 for a timing diagram of a typical write sequence.

INPUT REGISTER

The AD5025/AD5045/AD5065 input register is 32 bits wide (see Figure 41). The first four bits are don't cares. The next four bits are the command bits, C3 to C0 (see Table 8), followed by the 4-bit DAC address bits, A3 to A0 (see Table 7) and finally the data bits. These data bits comprise the 12-bit, 14-bit, or 16-bit input code, followed by eight, six, or four don't care bits for the AD5025/AD5045/AD5065, respectively (see Figure 41, Figure 42, and Figure 43). These data bits are transferred to the DAC register on the 32nd falling edge of SCLK.

Table 7. Address Commands

Address (n)				Selected DAC Channel
A3	A2	A1	A0	
0	0	0	0	DAC A
0	0	1	1	DAC B
0	0	0	1	Reserved
0	0	1	0	Reserved
1	1	1	1	Both DACs

Table 8. Command Definitions

Command				
C3	C2	C1	C0	Description
0	0	0	0	Write to Input Register n[1]
0	0	0	1	Update DAC Register n[1]
0	0	1	0	Write to Input Register n, update all (software $\overline{LDAC}$)
0	0	1	1	Write to and update DAC Channel n[1]
0	1	0	0	Power down/power up DAC
0	1	0	1	Load clear code register
0	1	1	0	Load $\overline{LDAC}$ register
0	1	1	1	Reset (power-on reset)
1	0	0	0	Set up DCEN register (daisy-chain enable)
1	0	0	1	Reserved
1	1	1	1	Reserved

[1] See Table 7.

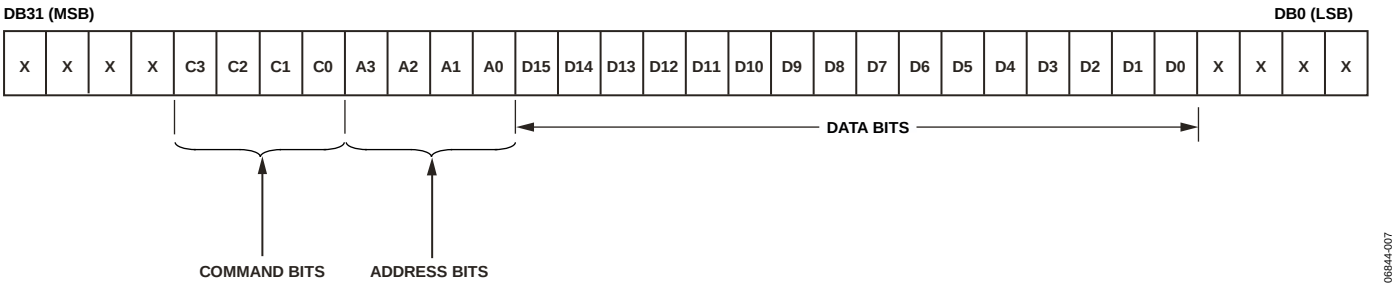


Figure 41. AD5065 Input Register Content

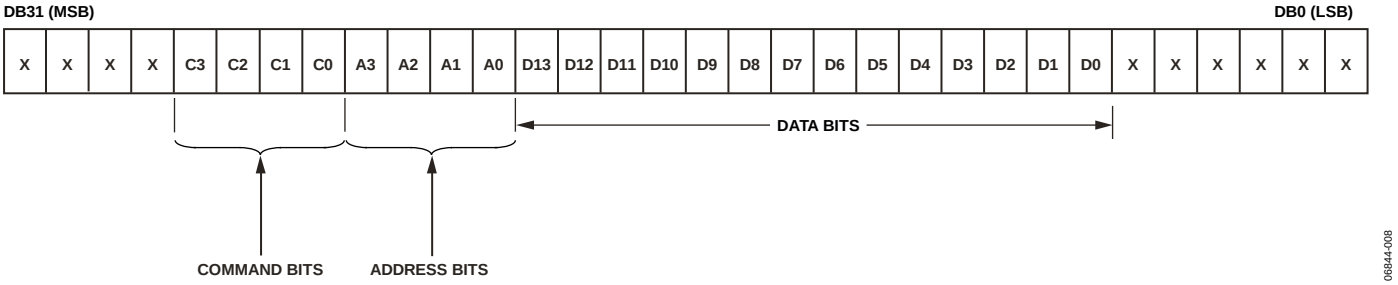


Figure 42. AD5045 Input Register Content

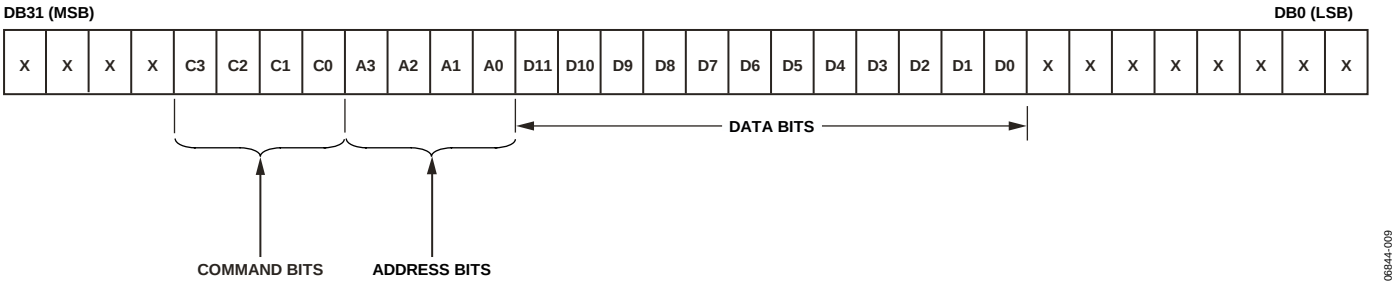


Figure 43. AD5025 Input Register Content

STANDALONE MODE

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the DIN line is clocked into the 32-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the AD5025/AD5045/AD5065 compatible with high speed DSPs. On the 32nd falling clock edge, the last data bit is clocked in and the programmed function is executed, that is, a change in DAC register contents and/or a change in the mode of operation. The $\overline{\text{SYNC}}$ line must be brought high within 30 ns of the 32nd falling edge of SCLK. In either case, it must be brought high for a minimum of 1.9 µs before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence. Because the $\overline{\text{SYNC}}$ buffer draws more current when $V_{IN} = V_{DD}$ than it does when $V_{IN} = 0$ V, $\overline{\text{SYNC}}$ should be idled low between write sequences for even lower power operation of the part. As mentioned previously, however, $\overline{\text{SYNC}}$ must be brought high again just before the next write sequence.

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 32 falling edges of SCLK, and the DAC is updated on the 32nd falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 32nd falling edge, this acts as an interrupt to the write sequence. The input register is reset, and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 44).

DAISY-CHAINING

For systems that contain several DACs, or where the user wishes to read back the DAC contents for diagnostic purposes, the SDO pin can be used to daisy-chain several devices together and provide serial readback.

The daisy-chain mode is enabled through a software executable daisy-chain enable (DCEN) command. Command 1000 is reserved for this DCEN function (see Table 8). The daisy-chain mode is enabled by setting a bit (DB1) in the DCEN register. The default setting is standalone mode, where DB1 = 0.

Table 9 shows how the state of the bit corresponds to the mode of operation of the device.

Table 9. DCEN (Daisy-Chain Enable) Register

DB1	DB0	Description
0	X	Standalone mode (default)
1	X	DCEN mode

The SCLK is continuously applied to the input register when $\overline{\text{SYNC}}$ is low. If more than 32 clock pulses are applied, the data ripples out of the input shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting this line to the DIN input on the next DAC in the chain, a multiDAC interface is constructed. Each DAC in the system requires 32 clock pulses; therefore, the total number of clock cycles must equal 32N, where N is the total number of devices in the chain.

If $\overline{\text{SYNC}}$ is taken high before 32N clocks are clocked into the part, it is considered an invalid frame and the data is discarded.

When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ is taken high. This prevents any further data from being clocked into the input register.

The serial clock can be continuous or a gated clock. A continuous SCLK source can be used only if $\overline{\text{SYNC}}$ can be held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data.

In daisy-chain mode, the $\overline{\text{LDAC}}$ pin cannot be tied permanently low. The $\overline{\text{LDAC}}$ pin must be used in asynchronous $\overline{\text{LDAC}}$ update mode, as shown in Figure 3. The $\overline{\text{LDAC}}$ pin must be brought high after pulsing. This allows all DAC outputs to simultaneously update.

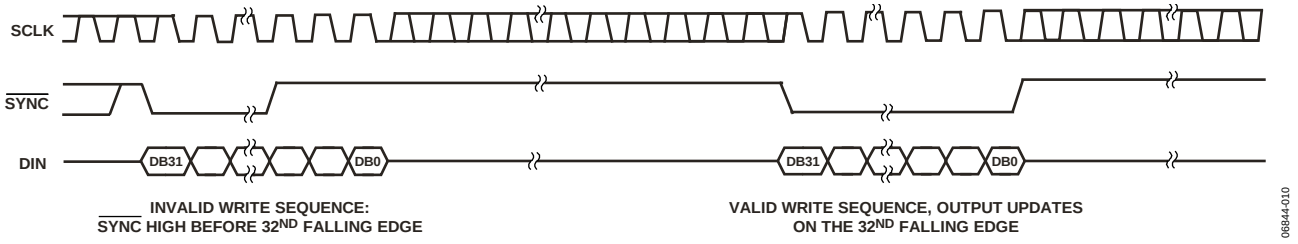


Figure 44. $\overline{\text{SYNC}}$ Interrupt Facility

Table 10. 32-Bit Input Register Contents for Daisy-Chain Enable

MSB											LSB
DB31 to DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB2 to DB19	DB1	DB0
X	1	0	0	0	X	X	X	X	X	1/0	X
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0)				Don't cares	DCEN register	

POWER-ON RESET AND SOFTWARE RESET

The AD5025/AD5045/AD5065 contain a power-on reset (POR) circuit that controls the output voltage during power-up. By connecting the POR pin low, the AD5025/AD5045/AD5065 output powers up to zero scale. Note that this is outside the linear region of the DAC; by connecting the POR pin high, the AD5025/AD5045/AD5065 output powers up to midscale. The output remains powered up at this level until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up. There is also a software executable reset function that resets the DAC to the power-on reset code selected by the POR pin. Command 0111 is reserved for this reset function (see Table 8).

POWER-DOWN MODES

The AD5025/AD5045/AD5065 contain four separate modes of operation. Command 0100 is reserved for the power-down function (see Table 8). These modes are software-programmable by setting two bits, Bit DB9 and Bit DB8, in the input register (see Table 12). Table 11 shows how the state of the bits corresponds to the mode of operation of the device.

Table 11. Modes of Operation

DB9	DB8	Operating Mode
0	0	Normal operation, power-down modes
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Three-state

When both Bit DB9 and Bit DB8 in the input register are set to 0, the part works normally with its normal power consumption of 2.2 mA at 5 V. However, for the three power-down modes, the supply current falls to 0.4 μV at 5 V. Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND through either a 1 kΩ or a 100 kΩ resistor, or it is left open-circuited (three-state). The output stage is illustrated in Figure 45.

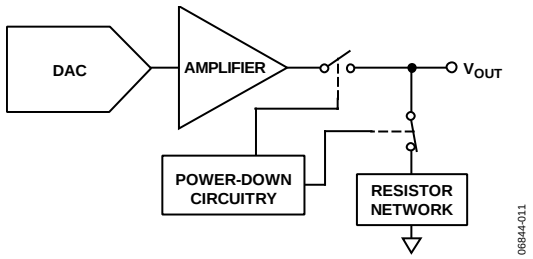


Figure 45. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry are shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 4.5 μs for V_{DD} = 5 V (see Figure 24).

Either or both DACs (DAC A and DAC B) can be powered down to the selected mode by setting the corresponding bits (DB3 and DB0) to 1. See Table 12 for the contents of the input register during power-down/power-up operation.

Any combination of DACs can be powered up by setting PD1 = 0 and PD0 = 0 (normal operation). The output powers up to the value in the input register ($\overline{\text{LDAC}}$ low) or to the value in the DAC register before powering down ($\overline{\text{LDAC}}$ high).

Table 12. 32-Bit Input Register Contents for Power-Up/Power-Down Function

MSB **LSB**

DB31 to DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB10 to DB19	DB9	DB8	DB4 to DB7	DB3	DB2	DB1	DB0
X	0	1	0	0	X	X	X	X	X	PD1	PD0	X	DAC B	DAC B	DAC A	DAC A
Don't cares	Command bits (C2 to C0)				Address bits (A3 to A0)—don't cares				Don't cares	Power-down mode		Don't cares	Power-down/power-up channel selection—set bits to 1 to select			

CLEAR CODE REGISTER

The AD5025/AD5045/AD5065 have a hardware $\overline{CLR}$ pin that is an asynchronous clear input. The $\overline{CLR}$ input is falling edge sensitive. Bringing the $\overline{CLR}$ line low clears the contents of the input register and the DAC registers to the data contained in the user-configurable $\overline{CLR}$ register, and sets the analog outputs accordingly (see Table 13). This function can be used in system calibration to load zero scale, midscale, or full scale to all channels together. These clear code values are user-programmable by setting two bits, Bit DB1 and Bit DB0, in the input register (see Table 13). The default setting clears the outputs to 0 V. Command 0101 is reserved for loading the clear code register (see Table 8).

Table 13. Clear Code Register

Clear Code Register		
DB1 (CR1)	**DB0 (CR0)**	**Clears to Code**
0	0	0x0000
0	1	0x8000
1	0	0xFFFF
1	1	No operation

The part exits clear code mode on the 32nd falling edge of the next write to the part. If $\overline{CLR}$ is activated during a write sequence, the write is aborted.

The $\overline{CLR}$ pulse activation time, the falling edge of $\overline{CLR}$ to when the output starts to change, is typically 10.6 µs (see Figure 31).

See Table 14 for contents of the input register during the loading clear code register operation.

$\overline{LDAC}$ FUNCTION

Hardware $\overline{LDAC}$ Pin

The outputs of all DACs can be updated simultaneously using the hardware $\overline{LDAC}$ pin. The $\overline{LDAC}$ pin can be used in synchronous or asynchronous mode, as shown in Figure 3.

Synchronous $\overline{LDAC}$: $\overline{LDAC}$ is held low. After new data is read, the DAC registers are updated on the falling edge of the 32nd SCLK pulse. $\overline{LDAC}$ can be permanently low or pulsed in standalone mode. $\overline{LDAC}$ cannot be tied permanently low in daisy-chain mode.

Asynchronous $\overline{LDAC}$: $\overline{LDAC}$ is held high and pulsed. The outputs are not updated at the same time that the input registers are written to. When $\overline{LDAC}$ goes low, the DAC registers are updated with the contents of the input register.

Software $\overline{LDAC}$ Function

Alternatively, the outputs of all DACs can be updated simultaneously using the software $\overline{LDAC}$ function by writing to Input Register n (see Table 7) and updating all DAC registers. Command 0010 is reserved for this software $\overline{LDAC}$ function.

The $\overline{LDAC}$ register gives the user extra flexibility and control over the hardware $\overline{LDAC}$ pin (see Table 16). Setting the $\overline{LDAC}$ bit register (DB0 to DB3) to 0 for a DAC channel means that this channel update is controlled by the hardware $\overline{LDAC}$ pin. If DB0 or DB3 is set to 1, this channel updates synchronously.

The part effectively sees the hardware $\overline{LDAC}$ pin as being tied low (see Table 15 for the $\overline{LDAC}$ register mode of operation). This flexibility is useful in applications where the user wants to simultaneously update select channels while the rest of the channels are synchronously updating.

Table 14. 32-Bit Input Register Contents for Clear Code Function

MSB **LSB**

DB31 to DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB2 to DB19	DB1	DB0
X	0	1	0	1	X	X	X	X	X	1/0	1/0
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0)				Don't cares	Clear code register (CR1 to CR0)	

Table 15. $\overline{LDAC}$ Overwrite Definitions

Load DAC Register		
$\overline{LDAC}$ Bits (DB3 and DB0)	**$\overline{LDAC}$ Pin**	**$\overline{LDAC}$ Operation**
0	1, 0	Determined by $\overline{LDAC}$ pin.
1	X[1]	DAC channels update, overrides the $\overline{LDAC}$ pin. DAC channels see $\overline{LDAC}$ as 0.

[1] X = don't care.

Table 16. 32-Bit Input Register Contents for $\overline{LDAC}$ Overwrite Function

MSB **LSB**

DB31 to DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB4 to DB19	DB3	DB2	DB1	DB0
X	0	1	1	0	X	X	X	X	X	DAC B	X	X	DAC A
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0)—don't cares				Don't cares	Set $\overline{LDAC}$ bits to 1 to override $\overline{LDAC}$ pin			

POWER-DOWN LOCKOUT

The AD5025/AD5045/AD5065 contain a digital input pin, $\overline{\text{PDL}}$. When activated, the power-down lockout pin ($\overline{\text{PDL}}$) disables software shutdown under any circumstances. The user should hardwire the $\overline{\text{PDL}}$ pin to a logic low (thus preventing subsequent software power-down) or logic high (the part can be placed in power-down mode over the serial interface). If the user transitions the $\overline{\text{PDL}}$ pin from logic high to a logic low during a valid write sequence, the device responds immediately and the current write sequence is aborted. Note the following $\overline{\text{PDL}}$ features.

$\overline{\text{PDL}}$ During a Write Sequence

If a $\overline{\text{PDL}}$ is generated (that is, a high-to-low transition) while a valid write sequence is ongoing, the write is aborted. The user must rewrite the current write command again.

$\overline{\text{PDL}}$ While DACs in Power-Down Mode

If a $\overline{\text{PDL}}$ is generated while the DAC(s) are in power-down mode, the DAC(s) come out of power-down (that is, all power-down bits are reset to 0000) to the last voltage output corresponding to the last valid stored DAC value. While $\overline{\text{PDL}}$ remains active, software power-down is disabled.

$\overline{\text{PDL}}$ Low to High Transition

After $\overline{\text{PDL}}$ is taken from a low to a high state, all DAC channels remain in normal mode, and the user must reissue a software power-down command to the control register to power down the required channels.

Transitioning $\overline{\text{PDL}}$ from a low to a high disables the feature immediately.

If $\overline{\text{PDL}}$ and $\overline{\text{CLR}}$ are generated at the same time, the $\overline{\text{CLR}}$ signal causes the DAC register to change as per the clear code register, and the DACs come out of power-down.

If $\overline{\text{PDL}}$, $\overline{\text{CLR}}$, and $\overline{\text{LDAC}}$ are generated at the same time, $\overline{\text{CLR}}$ has higher precedence over $\overline{\text{LDAC}}$ and $\overline{\text{PDL}}$.

The user is recommended to hardwire the pin to a logic high or low, thereby either enabling or disabling the feature.

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board (PCB) containing the AD5025/AD5045/AD5065 should have separate analog and digital sections. If the AD5025/AD5045/AD5065 are in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5025/AD5045/AD5065.

Bypass the power supply to the AD5025/AD5045/AD5065 with 10 µF and 0.1 µF capacitors. The capacitors should physically be as close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor has low effective series resistance (ESR) and low effective series inductance (ESI), which is typical of common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Shield clocks and other fast switching digital signals from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique, where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

MICROPROCESSOR INTERFACING

AD5025/AD5045/AD5065 to Blackfin ADSP-BF53x Interface

Figure 46 shows a serial interface between the AD5025/AD5045/AD5065 and the Blackfin® ADSP-BF53x microprocessor. The ADSP-BF53x processor family incorporates two dual-channel synchronous serial ports, SPORT1 and SPORT0, for serial and multiprocessor communications. Using SPORT0 to connect to the AD5025/AD5045/AD5065, the setup for the interface is as follows: DT0PRI drives the DIN pin of the AD5025/AD5045/AD5065, and TSCLK0 drives the SCLK of the parts. The $\overline{\text{SYNC}}$ is driven from TFS0.

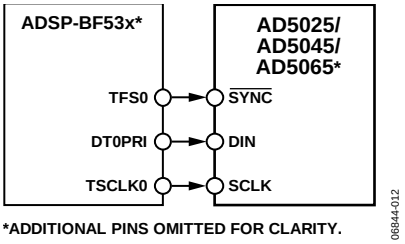


Figure 46. AD5025/AD5045/AD5065 to Blackfin ADSP-BF53x Interface

AD5025/AD5045/AD5065 to 68HC11/68L11 Interface

Figure 47 shows a serial interface between the AD5025/AD5045/AD5065 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5025/AD5045/AD5065, and the MOSI output drives the serial data line of the DAC.

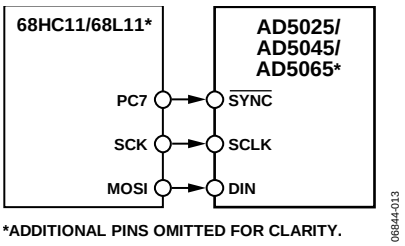


Figure 47. AD5025/AD5045/AD5065 to 68HC11/68L11 Interface

The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows: The 68HC11/68L11 is configured with its CPOL bit as 0, and its CPHA bit as 1. When data is being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is taken low (PC7). When the 68HC11/68L11 is configured as described previously, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data to the AD5025/AD5045/AD5065, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC. PC7 is taken high at the end of this procedure.

AD5025/AD5045/AD5065 to 80C51/80L51 Interface

Figure 48 shows a serial interface between the AD5025/AD5045/AD5065 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TxD of the 80C51/80L51 drives SCLK of the AD5025/AD5045/AD5065, and RxD drives the serial data line of the part. The $\overline{\text{SYNC}}$ signal is again derived from a bit-programmable pin on the port. In this case, Port Line P3.3 is used. When data is to be transmitted to the AD5025/AD5045/AD5065, P3.3 is taken low. The 80C51/80L51 transmits data in 8-bit bytes only; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is lept low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 outputs the serial data in LSB-first format. The AD5025/AD5045/AD5065 must receive data with the MSB first. The 80C51/80L51 transmit routine should take this into account.

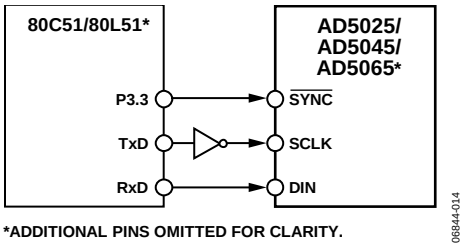


Figure 48. AD5025/AD5045/AD5065 to 80C51/80L51 Interface

AD5025/AD5045/AD5065 to MICROWIRE Interface

Figure 49 shows an interface between the AD5025/AD5045/AD5065 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5025/AD5045/AD5065 on the rising edge of SCLK.

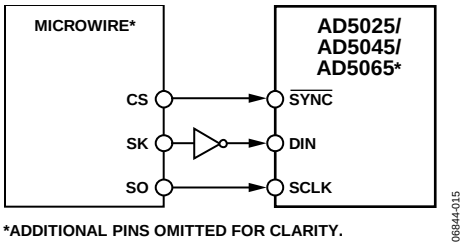


Figure 49. AD5025/AD5045/AD5065 to MICROWIRE Interface

APPLICATIONS INFORMATION

USING A REFERENCE AS A POWER SUPPLY FOR THE AD5025/AD5045/AD5065

Because the supply current required by the AD5025/AD5045/AD5065 is extremely low, an alternative option is to use a voltage reference to supply the required voltage to the parts (see Figure 50). This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V or 3 V, for example, 15 V. The voltage reference outputs a steady supply voltage for the AD5025/AD5045/AD5065. If the low dropout REF195 is used, it must supply 500 µA of current to the AD5025/AD5045/AD5065 with no load on the output of the DAC. When the DAC output is loaded, the REF195 also needs to supply the current to the load. The total current required (with a 5 kΩ load on the DAC output) is

500 µA + (5 V/5 kΩ) = 1.5 mA

The load regulation of the REF195 is typically 2 ppm/mA, which results in a 3 ppm (15 µV) error for the 1.5 mA current drawn from it. This corresponds to a 0.196 LSB error.

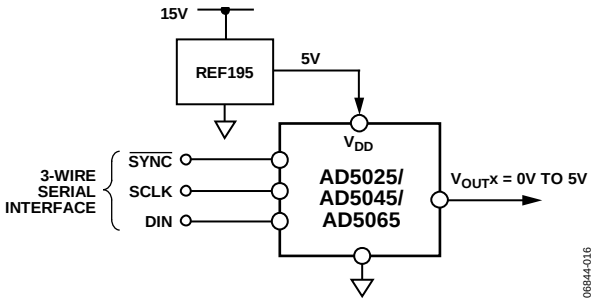


Figure 50. REF195 as Power Supply to the AD5025/AD5045/AD5065

BIPOLAR OPERATION USING THE AD5025/AD5045/AD5065

The AD5025/AD5045/AD5065 is designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 51. The circuit gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{DD} \times \left(\frac{D}{65{,}536} \right) \times \left(\frac{R1 + R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0 to 65,535).

With V_{DD} = 5 V, R1 = R2 = 10 kΩ,

$$V_O = \left(\frac{10 \times D}{65{,}536} \right) - 5 \text{ V}$$

This is an output voltage range of ±5 V, with 0x0000 corresponding to a −5 V output, and 0xFFFF corresponding to a +5 V output.

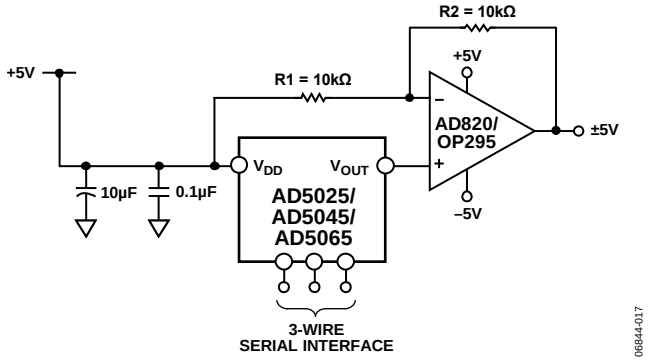


Figure 51. Bipolar Operation with the AD5025/AD5045/AD5065

USING THE AD5025/AD5045/AD5065 WITH A GALVANICALLY ISOLATED INTERFACE

In process control applications in industrial environments, it is often necessary to use a galvanically isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that can occur in the area where the DAC is functioning. *i*Coupler® provides isolation in excess of 2.5 kV. The AD5025/AD5045/AD5065 use a 3-wire serial logic interface, so the ADuM1300 three-channel digital isolator provides the required isolation (see Figure 52). The power supply to the part also needs to be isolated, which is achieved by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5025/AD5045/AD5065.

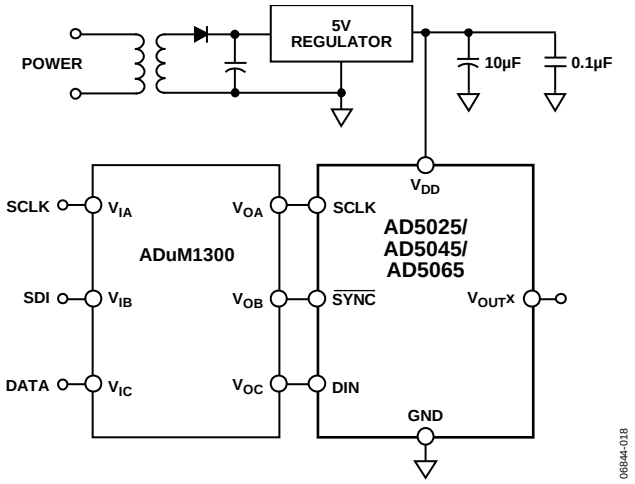


Figure 52. AD5025/AD5045/AD5065 with a Galvanically Isolated Interface

OUTLINE DIMENSIONS

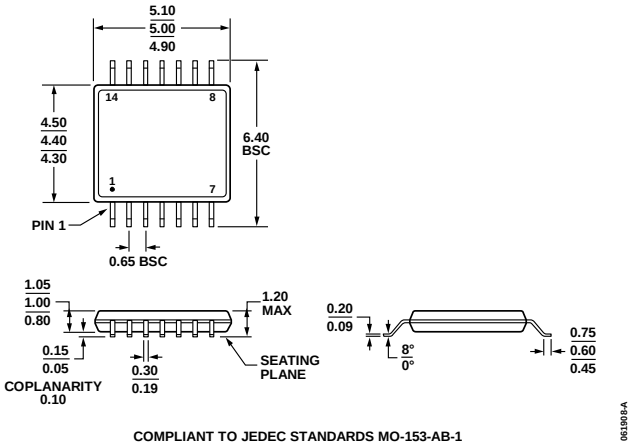


Figure 53. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Accuracy	Resolution
AD5025BRUZ	−40°C to +125°C	14-Lead TSSOP	RU-14	±0.25 LSB INL	12 bits
AD5025BRUZ-REEL7	−40°C to +125°C	14-Lead TSSOP	RU-14	±0.25 LSB INL	12 bits
AD5045BRUZ	−40°C to +125°C	14-Lead TSSOP	RU-14	±0.5 LSB INL	14 bits
AD5045BRUZ-REEL7	−40°C to +125°C	14-Lead TSSOP	RU-14	±0.5 LSB INL	14 bits
AD5065ARUZ	−40°C to +125°C	14-Lead TSSOP	RU-14	±4 LSB INL	16 bits
AD5065ARUZ-REEL7	−40°C to +125°C	14-Lead TSSOP	RU-14	±4 LSB INL	16 bits
AD5065BRUZ	−40°C to +125°C	14-Lead TSSOP	RU-14	±1 LSB INL	16 bits
AD5065BRUZ-REEL7	−40°C to +125°C	14-Lead TSSOP	RU-14	±1 LSB INL	16 bits

[1] Z = RoHS Compliant Part.

D06844-0-8/16(A)