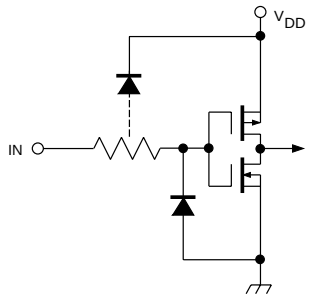
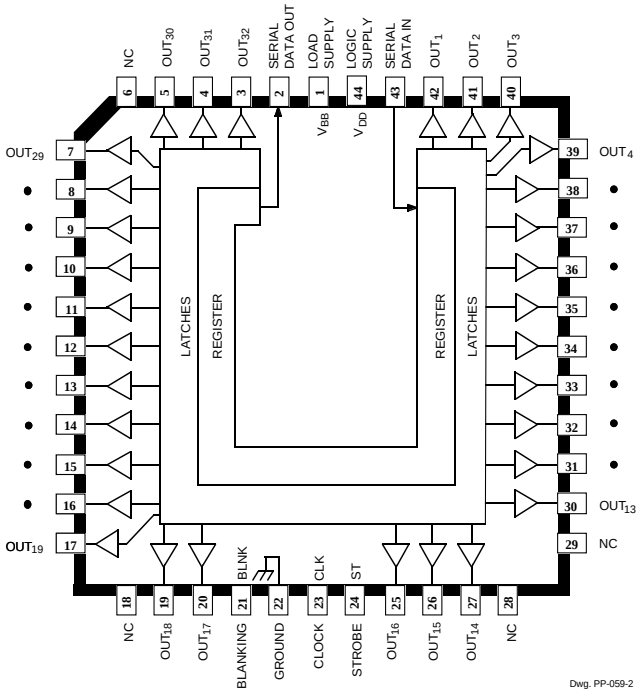
# 6818
## *32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER*

### TYPICAL INPUT CIRCUIT



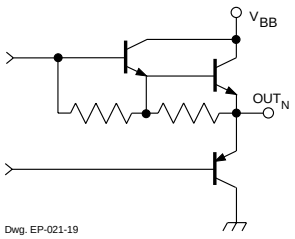

Dwg. EP-010-5

### A6818xEP

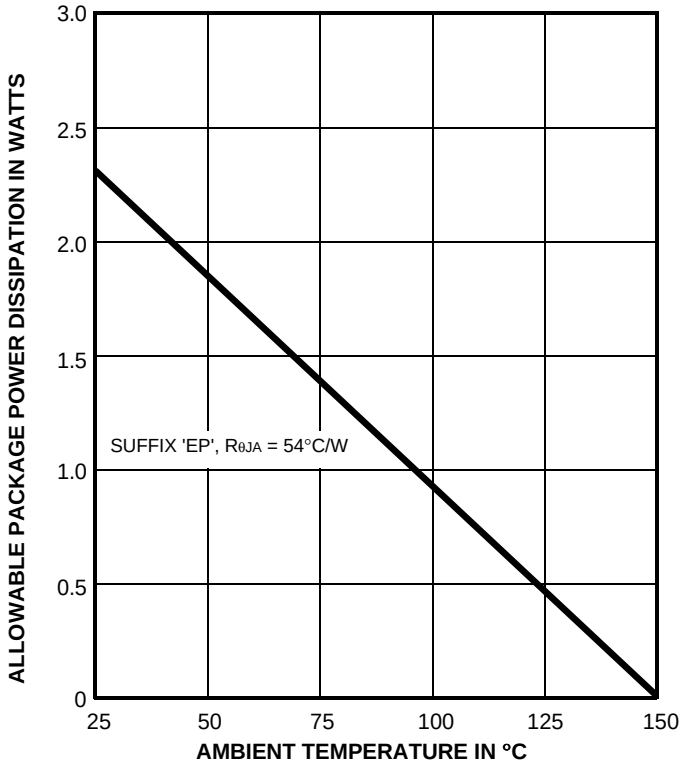



Dwg. PP-059-2

### TYPICAL OUTPUT DRIVER




Dwg. EP-021-19




Dwg. GP-025B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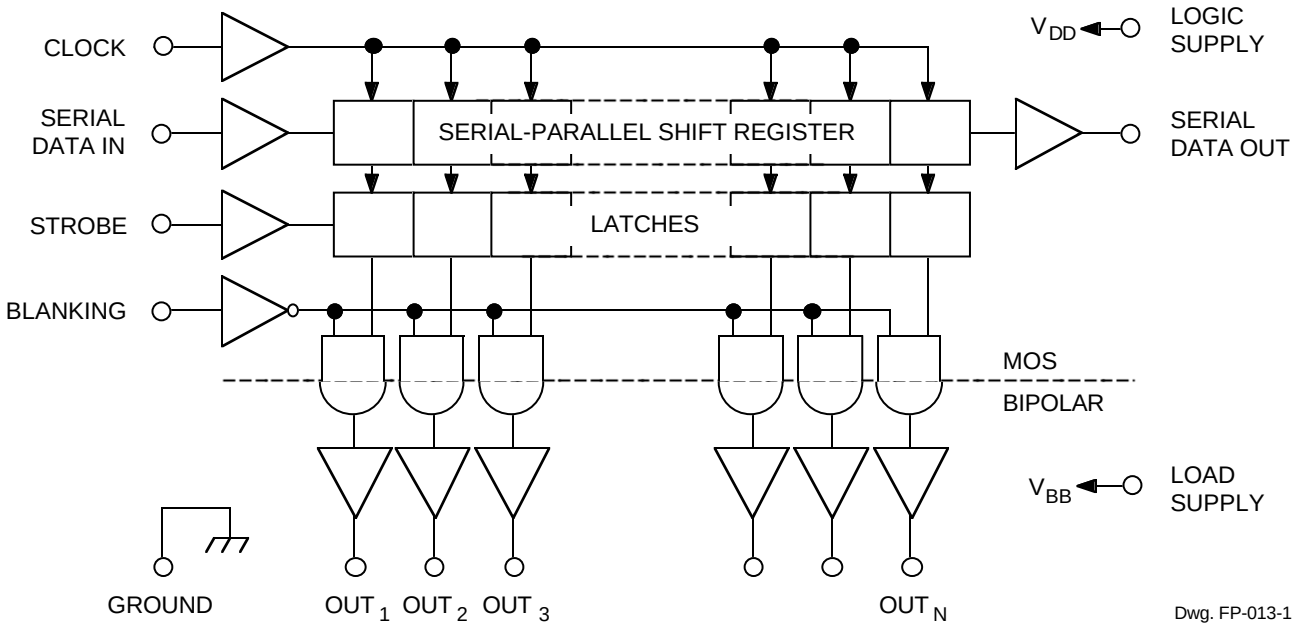
## FUNCTIONAL BLOCK DIAGRAM




## TRUTH TABLE

| Serial Data Input | Clock Input | Shift Register Contents | Serial Data Output | Strobe Input | Latch Contents | Blanking | Output Contents |
|---|---|---|---|---|---|---|---|
| | | $I_1$ $I_2$ $I_3$ ... $I_{N-1}$ $I_N$ | | | $I_1$ $I_2$ $I_3$ ... $I_{N-1}$ $I_N$ | | $I_1$ $I_2$ $I_3$ ... $I_{N-1}$ $I_N$ |
| H | ⌐ | H $R_1$ $R_2$ ... $R_{N-2}$ $R_{N-1}$ | $R_{N-1}$ | | | | |
| L | ⌐ | L $R_1$ $R_2$ ... $R_{N-2}$ $R_{N-1}$ | $R_{N-1}$ | | | | |
| X | ⌐ | $R_1$ $R_2$ $R_3$ ... $R_{N-1}$ $R_N$ | $R_N$ | | | | |
| | | X X X ... X X | X | L | $R_1$ $R_2$ $R_3$ ... $R_{N-1}$ $R_N$ | | |
| | | $P_1$ $P_2$ $P_3$ ... $P_{N-1}$ $P_N$ | $P_N$ | H | $P_1$ $P_2$ $P_3$ ... $P_{N-1}$ $P_N$ | L | $P_1$ $P_2$ $P_3$ ... $P_{N-1}$ $P_N$ |
| | | | | | X X X ... X X | H | L L L ... L L |

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

## ELECTRICAL CHARACTERISTICS at $T_A$ = +25°C (A6818S-) or over operating temperature range (A6818E- and A6818K-), $V_{BB}$ = 60 V unless otherwise noted.

| Characteristic | Symbol | Test Conditions | Limits @ $V_{DD}$ = 3.3 V | | | Limits @ $V_{DD}$ = 5 V | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Mln. | Typ. | Max. | Min. | Typ. | Max. | |
| Output Leakage Current | $I_{CEX}$ | $V_{OUT}$ = 0 V | — | <-0.1 | -15 | — | <-0.1 | -15 | µA |
| Output Voltage | $V_{OUT(1)}$ | $I_{OUT}$ = -25 mA | 57.5 | 58.3 | — | 57.5 | 58.3 | — | V |
| | $V_{OUT(0)}$ | $I_{OUT}$ = 1 mA | — | 1.0 | 1.5 | — | 1.0 | 1.5 | V |
| Output Pull-Down Current | $I_{OUT(0)}$ | $V_{OUT}$ = 5 V to $V_{BB}$ | 2.5 | 5.0 | — | 2.5 | 5.0 | — | mA |
| Input Voltage | $V_{IN(1)}$ | | 2.2 | — | — | 3.3 | — | — | V |
| | $V_{IN(0)}$ | | — | — | 1.1 | — | — | 1.7 | V |
| Input Current | $I_{IN(1)}$ | $V_{IN}$ = $V_{DD}$ | — | <0.01 | 1.0 | — | <0.01 | 1.0 | µA |
| | $I_{IN(0)}$ | $V_{IN}$ = 0.8 V | — | <-0.01 | -1.0 | — | <-0.01 | -1.0 | µA |
| Input Clamp Voltage | $V_{IK}$ | $I_{IN}$ = -200 µA | — | -0.8 | -1.5 | — | -0.8 | -1.5 | V |
| Serial Data Output Voltage | $V_{OUT(1)}$ | $I_{OUT}$ = -200 µA | 2.8 | 3.05 | — | 4.5 | 4.75 | — | V |
| | $V_{OUT(0)}$ | $I_{OUT}$ = 200 µA | — | 0.15 | 0.3 | — | 0.15 | 0.3 | V |
| Maximum Clock Frequency | $f_c$ | | 10 | 33 | — | 10 | 33 | — | MHz |
| Logic Supply Current | $I_{DD(1)}$ | All Outputs High | — | 0.25 | 0.75 | — | 0.3 | 1.0 | mA |
| | $I_{DD(0)}$ | All Outputs Low | — | 0.25 | 0.75 | — | 0.3 | 1.0 | mA |
| Load Supply Current | $I_{BB(1)}$ | All Outputs High, No Load | — | 4.5 | 9.0 | — | 4.5 | 9.0 | mA |
| | $I_{BB(0)}$ | All Outputs Low | — | 0.2 | 20 | — | 0.2 | 20 | µA |
| Blanking-to-Output Delay | $t_{dis(BQ)}$ | $C_L$ = 30 pF, 50% to 50% | — | 0.7 | 2.0 | — | 0.7 | 2.0 | µs |
| | $t_{en(BQ)}$ | $C_L$ = 30 pF, 50% to 50% | — | 1.8 | 3.0 | — | 1.8 | 3.0 | µs |
| Strobe-to-Output Delay | $t_{p(STH-QL)}$ | $R_L$ = 2.3 kΩ, $C_L$ ≤ 30 pF | — | 0.7 | 2.0 | — | 0.7 | 2.0 | µs |
| | $t_{p(STH-QH)}$ | $R_L$ = 2.3 kΩ, $C_L$ ≤ 30 pF | — | 1.8 | 3.0 | — | 1.8 | 3.0 | µs |
| Output Fall Time | $t_f$ | $R_L$ = 2.3 kΩ, $C_L$ ≤ 30 pF | 2.4 | — | 12 | 2.4 | — | 12 | µs |
| Output Rise Time | $t_r$ | $R_L$ = 2.3 kΩ, $C_L$ ≤ 30 pF | 2.4 | — | 12 | 2.4 | — | 12 | µs |
| Output Slew Rate | dV/dt | $R_L$ = 2.3 kΩ, $C_L$ ≤ 30 pF | 4.0 | — | 20 | 4.0 | — | 20 | V/µs |
| Clock-to-Serial Data Out Delay | $t_{p(CH-SQX)}$ | $I_{OUT}$ = ±200 µA | — | 50 | — | — | 50 | — | ns |

Negative current is defined as coming out of (sourcing) the specified device terminal.

Typical data is is for design information only and is at $T_A$ = +25°C.

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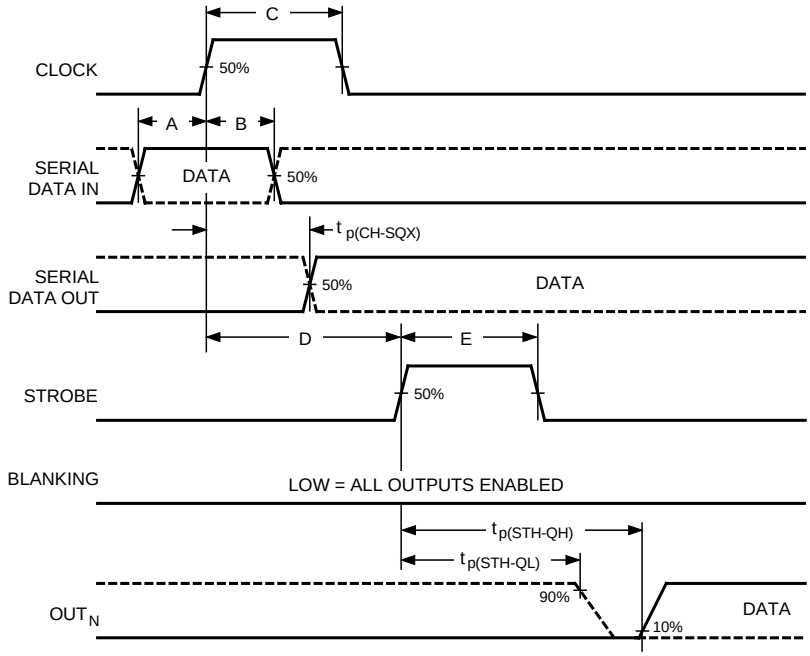
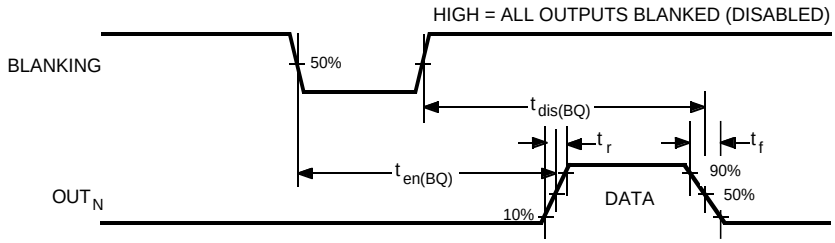
## TIMING REQUIREMENTS and SPECIFICATIONS

(Logic Levels are $V_{DD}$ and Ground)




Dwg. WP-029




Dwg. WP-030A

**A.** Data Active Time Before Clock Pulse (Data Set-Up Time), $t_{su(D)}$ ..... **25 ns**

**B.** Data Active Time After Clock Pulse (Data Hold Time), $t_{h(D)}$ ..... **25 ns**

**C.** Clock Pulse Width, $t_{w(CH)}$ ..... **50 ns**

**D.** Time Between Clock Activation and Strobe, $t_{su(C)}$ ..... **100 ns**

**E.** Strobe Pulse Width, $t_{w(STH)}$ ..... **50 ns**

NOTE – Timing is representative of a 10 MHz clock. Significantly higher speeds are attainable.

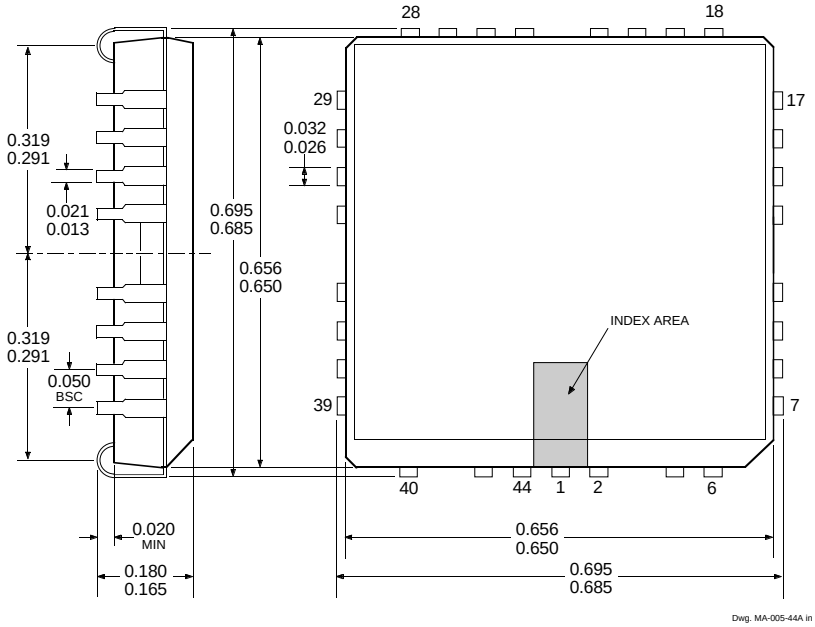
Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

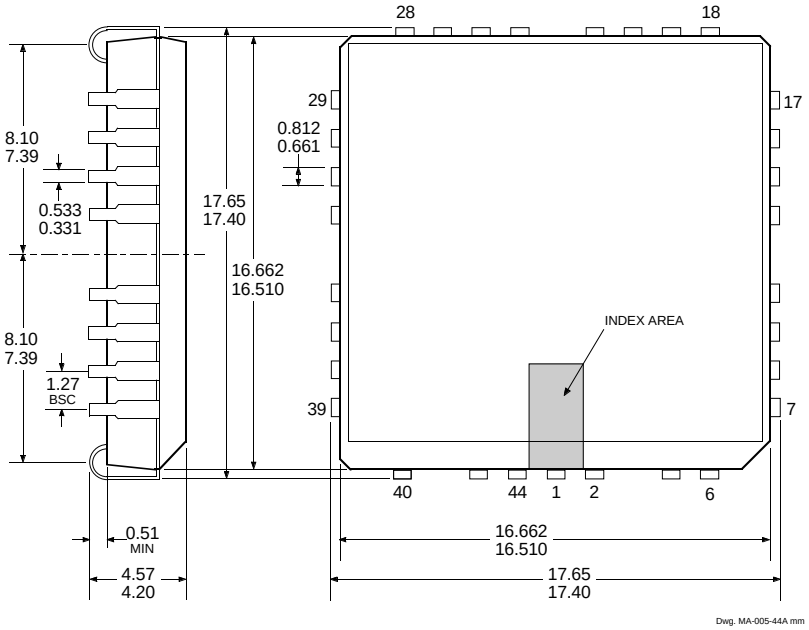
When the BLANKING input is high, the output source drivers are disabled (OFF); the pnp active pull-down sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

## A6818EEP & A6818SEP

Dimensions in Inches
(controlling dimensions)




Dimensions in Millimeters
(for reference only)




NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.

# 6818
## *32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER*

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