HARDWARE DESCRIPTION

The 73M2901CE is designed to operate from a +3.6 to +2.7 volt supply with low power consumption (~30mW @3.0 volts). The modem supports automatic standby idle mode. The modem will also accept a request to power down from the DTE via hardware control. No additional major components are required to complete the modem core logic. The modem provides direct firmware LED support via port pins.

HARDWARE FEATURES

- Fully self-contained. "AT" Command interpreter and data pump
- User pins available
- Synchronous serial data I/O available
- Asynchronous serial port
- On-chip hybrid and line driver.
- Autobaud capability from 300bps to 9600bps
- Reduced external hardware support required with energy incoming ring detection.

POWER SUPPLY

Power is supplied to the 73M2901CE via the VPD and VPA pins. The 73M2901CE is designed for a single +3.6 to +2.7 volt supply and for low power consumption (~30mW @ 3.0 volts). Ground is supplied to the 73M2901CE via VND and VNA pins.

The 73M2901CE has been designed with separated analog and digital supplies to insure the best performance of the part by using separately filtered power supplies. It is recommended that separate locally bypassed traces be used to apply power to the analog supply VPA and the digital supply VPD.

LOW POWER MODE

The TERIDIAN 73M2901CE supports a low power standby mode. If the low power standby option is enabled the 73M2901CE will go into a power saving mode when idle. The oscillator will be running, clocks will be supplied to the UART, timers and interrupt blocks; but no clocks will be supplied to the CPU. Instruction processing and activity on the internal busses is halted. Normal operation is resumed when an interruption such as assertion of $\overline{\text{DTR}}$ or $\overline{\text{RING}}$, a character is sent to the 73M2901CE TXD input, or a reset occurs.

ANALOG LINE / HYBRID INTERFACE

The 73M2901CE provides a differential analog output (TXAP and TXAN) and a single-ended analog input (RXA) with internal A/D and D/A converters. A driver is provided for an internal hybrid function.

The internal hybrid driver is capable of driving an external load matching impedance and a line-coupling transformer. The internal hybrid/line driver senses the load and adapts itself to its requirements.

The 73M2901CE provides firmware control for a hook relay driver ($\overline{\text{RELAY}}$) as well as interrupt support for a ring detect opto-coupler ($\overline{\text{RING}}$).

INTERRUPT PINS

The external interrupt sources, $\overline{\text{DTR}}$ and $\overline{\text{RING}}$, come from dedicated input pins of the same name.

$\overline{\text{DTR}}$ informs the 73M2901CE that the host has requested the 73M2901CE perform a specific function. The function of $\overline{\text{DTR}}$ can be changed by "AT" commands (described in full in the TERIDIAN 73M2901CE User's Guide).

$\overline{\text{RING}}$ is used to inform the 73M2901CE that the external DAA circuitry or ring energy detector has detected a ring signal. It will go active when each "RING" message is sent on RXD.

In addition, sending any character on the TXD line also generates an internal interrupt.

CRYSTAL OSCILLATOR

The TERIDIAN 73M2901CE single chip modem can use an external 11.0592 MHz reference clock or can generate a clock using only a crystal and two capacitors. If an external clock is used, it should be applied to OSCIN.

SPECIFYING A CRYSTAL

The manufacturer of a crystal resonator verifies its frequency of oscillation in a test set-up, but to ensure that the same frequency is obtained in the application, the circuit conditions must be the same. The TERIDIAN 73M2901CE modem requires a parallel mode (anti-resonant) crystal, the important specifications of which are as follows:

Mode: Parallel (anti-resonant)

Frequency: 11.0592 MHz

Frequency tolerance: ±50 ppm at initial temperature.

Temp. drift: An additional ±50 ppm over full range.

Load capacitance: 18pF to 22pF

ESR: 75Ω max.

Drive level: Less than 1mW.

The peak voltage level of the oscillator should be checked to assure it will not violate the maximum voltage levels allowed on the oscillator pins. A resistor in series with the crystal can be used, if necessary, to reduce the oscillator's peak voltage levels.

Crystals with low ESRs may oscillate at higher than specified voltage levels.

RESET

A reset is accomplished by holding the RESET pin high. To ensure a proper power-on reset, the reset pin must be held high for a minimum of 3μs. At power on, the voltage at VPD, VPA, and RESET must come up at the same time for a proper reset. The signals $\overline{DCD}$, $\overline{CTS}$ and $\overline{DSR}$ will be held inactive for 25ms, acknowledging the reset operation, within a 250ms time window after the reset-triggering event. The 73M2901CE is ready for operation after the 250ms window and/or after the signals $\overline{DCD}$, $\overline{CTS}$ and $\overline{DSR}$ become active.

ASYNCHRONOUS AND SYNCHRONOUS SERIAL DATA INTERFACE

The serial data interface consists of the TXD and RXD data paths (LSB shifted in and out first) and the TXCLK and RXCLK serial synchronous clock outputs associated with the data pins; $\overline{CTS}$/$\overline{RTS}$ flow control; $\overline{DCD}$, $\overline{DSR}$ and $\overline{DTR}$. In asynchronous mode, the data is passed at the bit rate (tolerance is +1%, -2.5%).

PIN DESCRIPTIONS

POWER PIN DESCRIPTION

PIN NAME	PIN	TYPE	DESCRIPTION
VPA	10	I	Positive analog voltage (Analog supply)
VNA	16	I	Negative analog voltage (Analog ground)
VPD	2, 20, 25	I	Positive digital voltage (Digital supply)
VND	1, 17, 22	I	Negative digital voltage (Digital ground)

ANALOG INTERFACE PIN DESCRIPTION

PIN NAME	PIN	TYPE	DESCRIPTION
RXA	15	I	Receive Analog input
TXAN	11	O	Transmit Analog - output
TXAP	12	O	Transmit Analog + output
VBG	14	O	Analog Band Gap voltage reference (0.1μF to VNA). This pin must not be connected to external circuitry other than the decoupling capacitor.
VREF	13	O	Analog reference voltage (0.1μF to VNA)

DIGITAL INTERFACE PIN DESCRIPTION

PIN NAME	PIN	TYPE	DESCRIPTION
RESET	9	I	Reset
RXCLK	27	O	Receive data synchronous clock valid on rising edge
TXCLK	24	O	Transmit data synchronous clock valid on rising edge
TXD	23	I	Serial data input from DTE
RXD	26	O	Serial output to DTE
USR10	8	I/O	Programmable I/O port. This pin optionally be used to control an external switch for external Line In Use circuitry.
USR11	7	I/O	Programmable I/O port. This pin can optionally be used to control an external switch for caller ID operation.
$\overline{\text{RTS}}$	6	I	Request to send
$\overline{\text{CTS}}$	5	O	Clear to send
$\overline{\text{DSR}}$	4	O	Data set ready
$\overline{\text{DCD}}$	3	O	Data carrier detect
$\overline{\text{RI}}$	32	O	Ring indicator
$\overline{\text{RELAY}}$	31	O	Relay driver output
USR20	29	I/O	Programmable I/O port

EXTERNAL INTERRUPTS PIN DESCRIPTION

PIN NAME	PIN	TYPE	DESCRIPTION
$\overline{\text{RING}}$	30	I	External interrupt – Line interface ring detection circuitry input
$\overline{\text{DTR}}$	28	I	External interrupt – DTE $\overline{\text{DTR}}$ signal input

OSCILLATOR PIN DESCRIPTION

PIN NAME	PIN	TYPE	DESCRIPTION
OSCIN	19	I	Crystal input for internal oscillator, also input for external source
OSCOUT	18	O	Crystal oscillator output

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Supply Voltage	-0.5V to +4.0V
Pin Input Voltage (except OSCIN)	-0.5V to + 6.0V
Pin Input Voltage (OSCIN)	-0.5V to VPD + 0.5V
Storage Temperature	-55ºC to 150ºC

NOTE: This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING
Supply Voltage	2.7V – 3.6V
Oscillator Frequency	11.0592MHz +/- 50ppm
Operating Temperature	-40ºC to 85ºC

RECEIVER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Carrier detect On	Tip and Ring	-43			dBm0*
Carrier detect Off	Tip and Ring	-48			dBm0*
Carrier Detect Hysteresis	Tip and Ring		2		dB
Receive Level	Tip and Ring	-43		-9	dBm0*
Idle channel noise	0.2KHz – 4.0KHz		-70	-65	dB
Input impedance	RXA	150			kΩ
Receive Gain Boost	S110 bit 5=1, CID mode	18.8	19.3	19.8	dB
Max Input Level at RXA	Vref=1.25V	0.587	0.622	0.658	Vpk
Total Harmonic Distortion (THD)	1KHz 450mVpk on RXA THD=2nd and 3rd harmonic		-70	-50	dB

* dBm0 refers to the TERIDIAN recommended line interface (8dB loss from transmit pins to the line and 5dB loss from the line to the receiver pin). Results may vary depending on the selected DAA components. 0dBm=0.775mV$_{rms}$; dBm=10log(V$_{rms}^2$/(1mW)(600Ω))

TRANSMITTER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ITU Guard tone power	550Hz (relative to carrier)	-5	-3.5	-2	dB
	1800Hz (relative to carrier)	-8	-6.5	-5	dB
Calling Tone	1300Hz	-11	-10	-9	dBm0*
Answer Tone power	2225Hz/2100Hz	-11	-10	-9	dBm0*
DTMF Transmit power	High band tones	-12	-11.5	-11	dBm0*
	Low band tones	-13.7	-13.2	-12.7	dBm0*
Gain adjust tolerance	By step	-0.3	0	0.3	dBm0*
Total Harmonic Distortion (THD)	1KHz sine wave at output (TXAP-TXAN) 1.5Vpk(2.7dBm) for Vref=1.25V THD=2nd and 3rd harmonic			-50	dB
Intermod Distortion	At output (TXAP-TXAN) 1KHz, 1.2KHz sine waves summed 2Vpk for Vref=1.25V	Each unwanted frequency component		-33	dBm
		Sum of unwanted frequency components in pass band		-20	dB below low tone
Power supply rejection ratio	-30dBm signal at VPA 300Hz-30KHz. Measured TXAP to TXAN			30	dB

MAXIMUM TRANSMIT LEVEL

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
QAM	Vref=1.25V VPA=3.3V			-9.6	dBm0*
DPSK	Vref=1.25V VPA=3.3V			-7.4	dBm0*
FSK	Vref=1.25V VPA=3.3V			-5.3	dBm0*
DTMF (HIGH TONE)	Vref=1.25V S13=$20, VPA=3.3V S85=80	-8		-7	dBm0*
DTMF (LOW TONE)	Vref=1.25V S13=$20, VPA=3.3V S85=80	-9.7		-8.7	dBm0*

* dBm0 refers to the TERIDIAN recommended line interface (8dB loss from transmit pins to the line and 5dB loss from the line to the receiver pin). Results may vary depending on the selected DAA components. 0dBm=0.775mv$_{rms}$; dBm=20log(V$_{rms}$/(0.775mv$_{rms}$)

DC CHARACTERISTICS VCC=3.3V (Vdd stands for VPD and VPA)

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Input low voltage (except OSCIN)	VIL		-0.5		0.8	V
Input low voltage OSCIN	VIL		-0.5		0.2Vdd	V
Input high voltage (except OSCIN)	VIH		0.7Vdd		+5.5	V
Input high voltage OSCIN	VIH		0.7Vdd		Vdd+0.5	V
Output low voltage (except OSCOUT)	VOL	IOL=4mA			0.45	V
Output low voltage OSCOUT	VOLOSC	IOL=3mA			0.7	V
Output high voltage (except OSCOUT)	VOH	IOH=-4mA	Vdd-0.45			V
Output high voltage OSCOUT	VOHOSC	IOH=-3mA	Vdd-0.9			V
Input leakage current (except OSCIN)	IIH	Vss<Vin<Vdd			1	µA
Input leakage current OSCIN	IIH	Vss<Vin<Vdd	1		30	µA

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VBG	Vdd=3.3V	1.19	1.25	1.31	V
VREF	Vdd=3.3V	1.19	1.25	1.31	V
TXAP to TXAN offset	Vdd=3.3V, steady state			50	mV

DC SUPPLY CURRENT VDD = 2.7V (BATTERY EOL)

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Maximum Power supply, normal operation	IDD1	30pF/pin		9.5	10.5	mA
Maximum power supply Idle mode	IDD2	30pF/pin		900	1500	µA
Maximum power supply Power down mode	IDD3	30pF/pin			10	µA

DC SUPPLY CURRENT VDD = 3.0V

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Maximum Power supply, normal operation	IDD1	30pF/pin		10.6	11.9	mA
Maximum power supply Idle mode	IDD2	30pF/pin		1.1	1.7	mA
Maximum power supply Power down mode	IDD3	30pF/pin			10	µA

DC SUPPLY CURRENT VDD = 3.3V

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Maximum Power supply, normal operation	IDD1	30pF/pin		11.8	13.6	mA
Maximum power supply Idle mode	IDD2	30pF/pin		1.25	1.85	mA
Maximum power supply Power down mode	IDD3	30pF/pin			10	μA

DC SUPPLY CURRENT VDD = 3.6V

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Maximum Power supply, normal operation	IDD1	30pF/pin		13.4	15.5	mA
Maximum power supply Idle mode	IDD2	30pF/pin		1.4	2.0	mA
Maximum power supply Power down mode	IDD3	30pF/pin			10	μA

FIRMWARE DESCRIPTION*

An "AT" command interpreter provides command and configuration of the 73M2901CE. This provides the user a uniform interface to control the modem in embedded applications.

The signal processing is performed to provide data to the DAC and process data from the A/D converter. A MAC hardware coprocessor is provided for computation.

To provide maximum flexibility, the system host processor can access the internal RAM and Control Register space in the modem. This will allow the OEM user to modify parameters such as filter response, transmit levels through the AT command set using proprietary commands. The host processor can also access the modem I/O port pins, providing extended I/O capability.

FIRMWARE REQUIREMENTS

The modem always powers up in the idle (on hook) mode. "AT" commands are issued via the serial interface from the host. All modem configuration commands are received in this manner. The data modem firmware is contained in an internal ROM. The firmware will automatically enter a power saving idle mode if the modem is on hook and there are no incoming host commands. The modem automatically powers up upon receiving the next command. This power up sequence occurs without delay to the host. This function, while saving power, is transparent to the host processor and can be disabled by the host via an "AT" command. The host can also program the modem to power down via external pin ($\overline{DTR}$) or via a firmware command.

FIRMWARE FEATURES

- "AT" command set
- Supports data standards through V.22bis
- Provides DAA control firmware (e.g. ring detect, hook control)
- Multinational Call progress support (FCC part 68, ITU CTR21, Japan JATE, etc.)
- Caller ID capability
    - FSK demodulation (V23 or Bell202)
    - DTMF demodulation
    - Selectable number of rings and line reversal for CID data operation
    - On or off hook CID data operation
- On hook Line-In-Use detection support (No line seizure will occur when a Line-In-Use condition is detected)
    - Tip/Ring voltage sensing
    - Energy on the line validation
- Off hook Parallel Pick-Up detection support (Line seizure will be aborted as soon as a Parallel Pick-Up condition is detected)
    - Off hook voltage change detection
    - Receive energy change detection
- Directly interfaces with standard V.24/EIA-232 bus drivers (3.3V inverted level) serial interface using the built in serial port and firmware control of port pins
- Provides tone generation and detection including four imprecise and four precise call progress detect filters with programmable frequency and detection threshold
- Blacklisting capability
- Long Space disconnect support
- Inactivity timeout
- Host access to program RAM provided
- User programmable general purpose I/O

* Refer to the TERIDIAN 73M2901CE User Guide for a complete description of the software.

TERIDIAN Semiconductor's 73M2901CE single chip modem includes all the basic modem functions. Programmable configuration options make this device highly adaptable to a wide variety of applications.

Unlike digital logic circuitry, modem designs must contend with precise frequency tolerances and verify low-level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. The crystal oscillator should be held to a 50ppm tolerance. The following recommendations should be taken into consideration when starting new designs.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain high performance in modem designs. The more digital circuitry present in the application, the more attention to noise control is needed.

High speed, digital devices should be locally bypassed, and the telephone line interface and the modem should be located next to each other near where the telephone line connection is accessed. It is recommended that power supplies and ground traces should be routed separately to the analog and digital portions on the board. Digital signals should not be routed near low-level or high impedance analog traces.

The 73M2901CE should be considered a high performance analog device. A 3.3μF electrolytic capacitor in parallel with a 0.1μF Ceramic capacitor should be placed between each VPD and VND pin and a 10μF and 0.1μF between VPA and VNA. A 0.1μF ceramic capacitor should be placed between VREF and VNA as well as VBG and VNA. Use of ground planes and large traces on power is recommended.

73M2901CE DESIGN COMPATIBILITY

The TERIDIAN 73M2901CE is an enhanced version of the TERIDIAN 73M2901CL and has a number of new features. These parts are highly compatible with the earlier 73M2901 however special attention should be paid when changing an existing 73M2901 design to use the 73M2901CE or 73M2901CL. From a hardware standpoint, the key differences involve the User I/O pins USR10, USR11, the ASRCH pin and the HBDEN pin. An additional user I/O pin USR20 replaces the ASRCH pin on the 73M2901CE. This pin may remain safely connected to TXD as long as the host software does not reconfigure USR20 as an output (S104 bit0=0). The 73M2901CE contains a high efficiency low power hybrid driver. Due to this enhancement HBDEN is no longer required. This pin is an internal no-connect and can safely remain connected to its previous VPD or GND. The functions of USR10 and USR11 are related to Caller ID and Line In Use/Parallel Pickup support.

Software enhancements to the 73M2901CE are typically achieved by the addition of new AT commands. The device can be considered a superset of the 73M2901CL and 73M2901C. When converting a design to the 73M2901CE it is recommended that the user check the commands and register settings for backward compatibility to the earlier parts*.

TELEPHONE LINE INTERFACE

Transmit levels at the line are dependent on the interface used between the pins and the line. The internal hybrid line drivers eliminate the need for additional active circuitry to drive the line-coupling transformer. The analog outputs (TXAP and TXAN) can be connected directly to the transformer (with the required impedance matching series resistor or network) however some low cost transformers may be affected by the limited amount of DC current generated by the analog outputs (DC offset); hence it is recommended to use a coupling capacitor with those transformers to insure maximum performance. The line interface circuit shown on the following page represents the basic components and values for interfacing the TERIDIAN 73M2901CE analog pins to the telephone line. The values of these components have been calculated to minimize the transmission and reception path hybrid losses and are linked by the following equation: R15=0.242 x R13.

* (refer to the TERIDIAN 73M2901CE User Guide for complete details)

MODEM PERFORMANCE CHARACTERISTICS

The curves presented in this data sheet define modem IC performance under a variety of line conditions typical of those encountered over Public Switched Telephone Network.

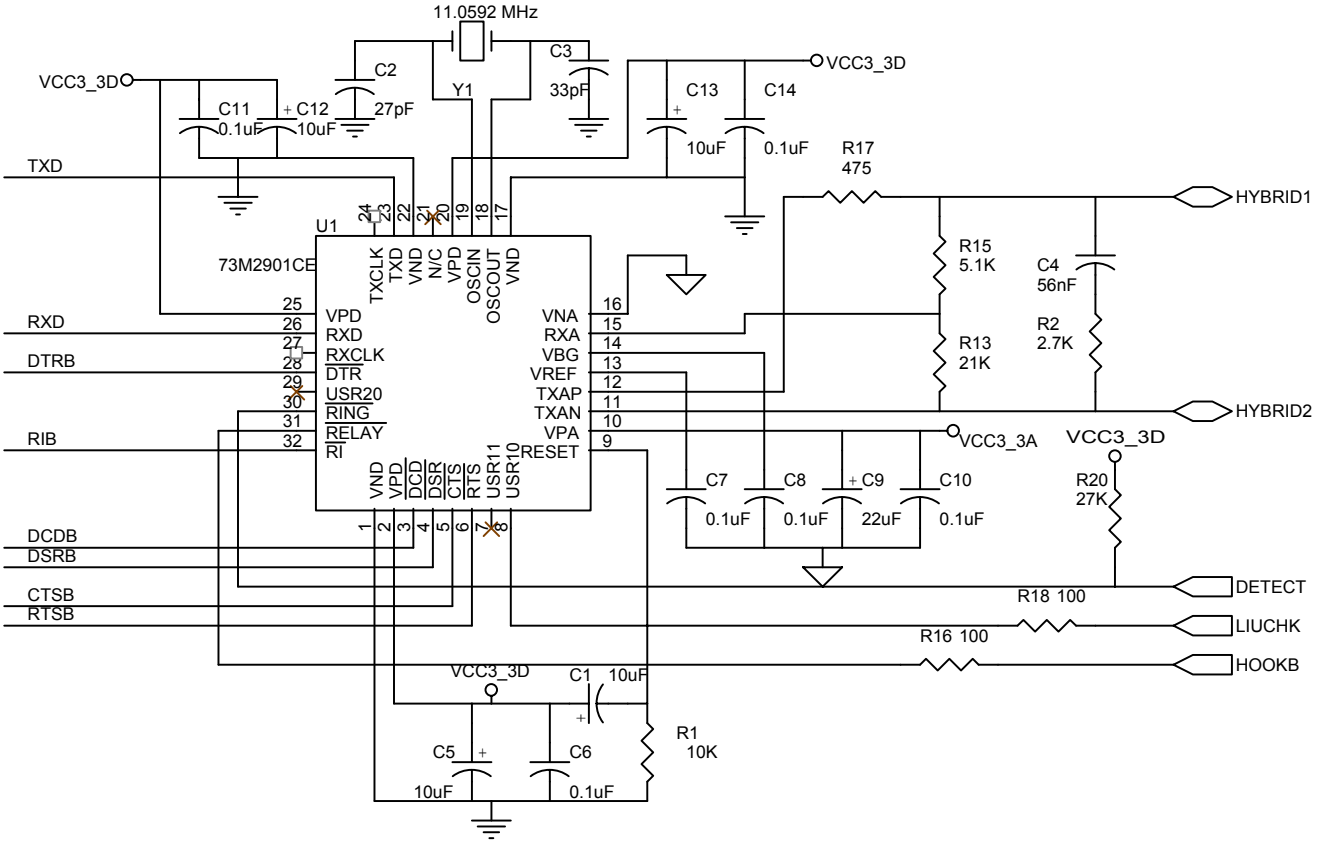
BER VS. SNR

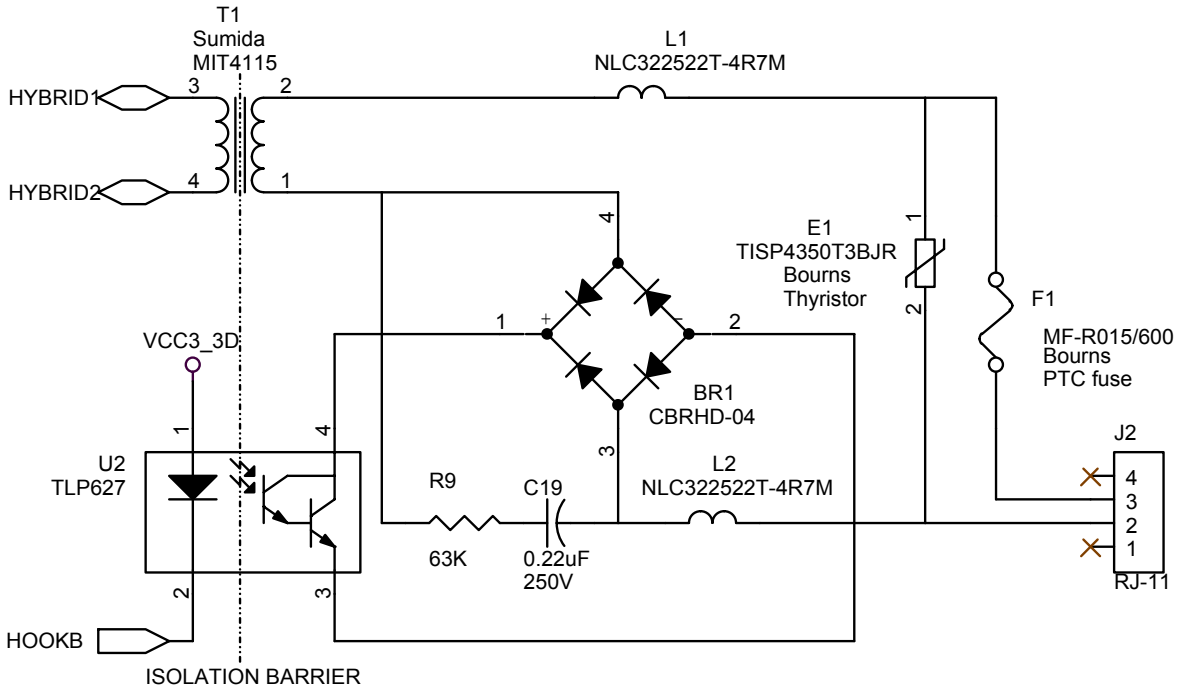
This test represents the ability of the modem to operate over noisy lines with a minimum amount of data transfer errors. Since some noise is generated in the best dial up lines, the modem must operate with the lowest signal to noise ratio (SNR) possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of typical operating conditions. A DPSK or QAM modem will exhibit better BER performance test curves receiving in the low band (answer mode) than in the high band (originate mode).

BER VS. RECEIVE LEVEL

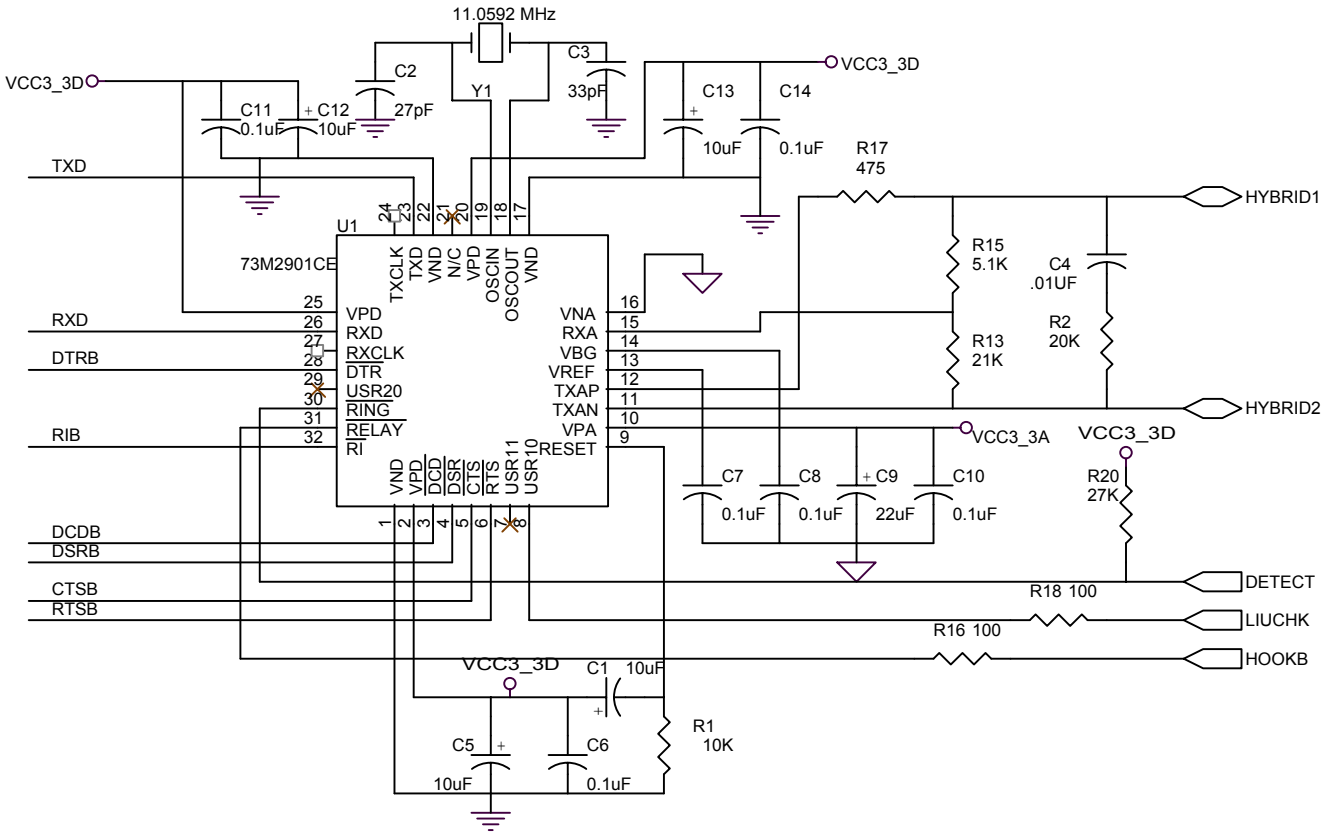
This test measures the dynamic range of the modem. Because signal levels vary widely over dial up lines, the widest possible dynamic range is desirable. The SNR is held constant at the indicated values as the Receive level is lowered from a very high to a very low signal level. The width of the bowl of these curves, taken at the BER break points is the measure of the dynamic range.

LOW COST DESIGN USING DSP RING AND STATUS MONITORING

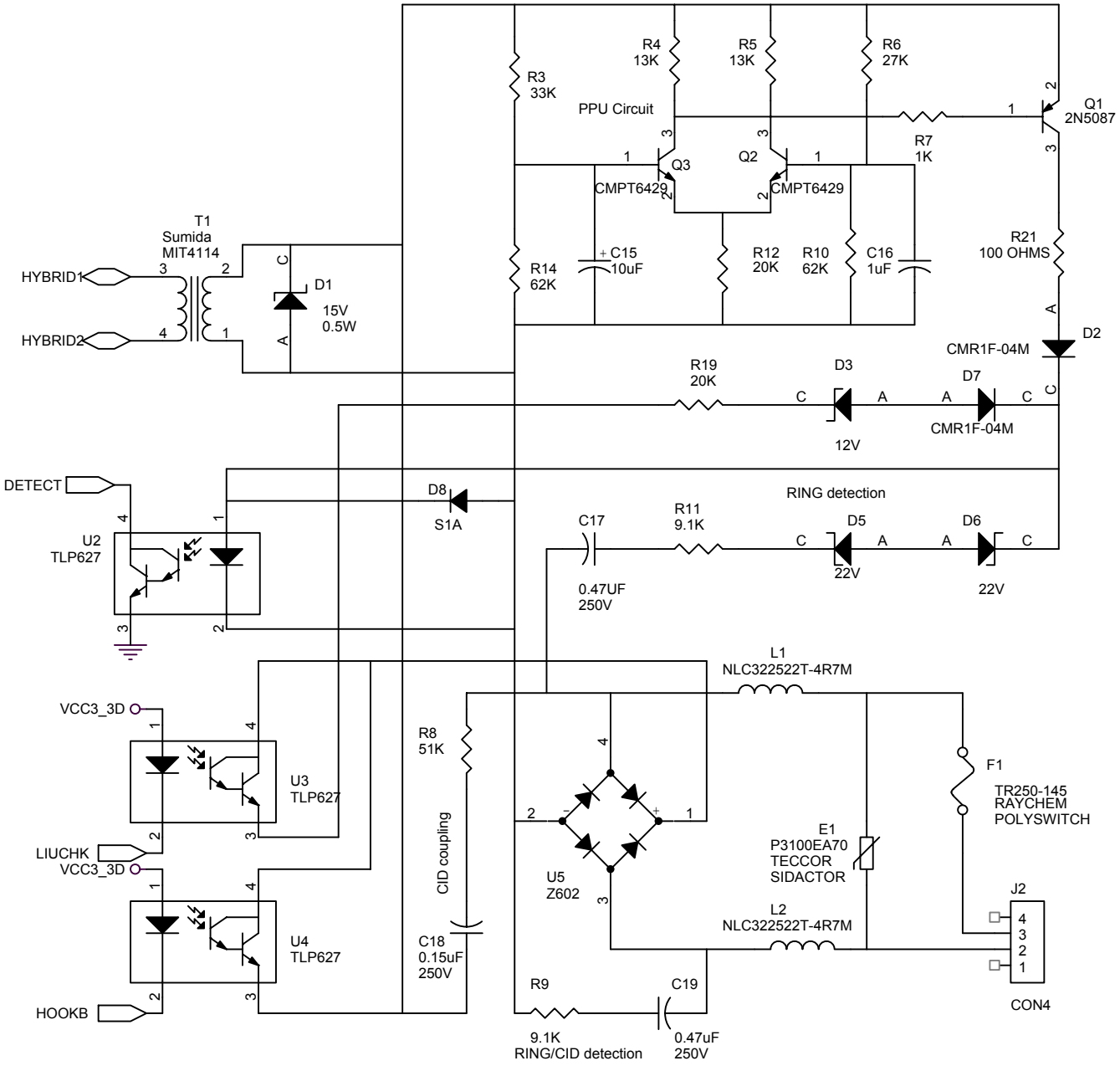




REFERENCE DESIGN USING TRADITIONAL HARDWARE LINE MONITORING



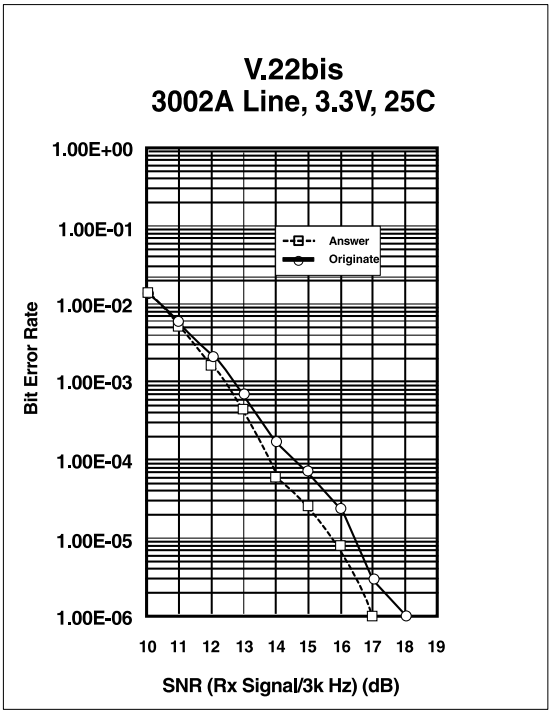
Modem and Hybrid Circuitry



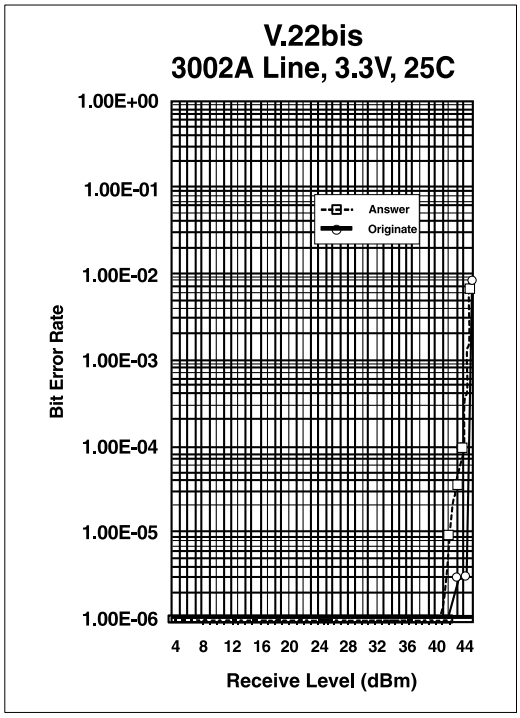
DAA Circuit Showing Hardware Detection Circuitry

BER CURVES

BER vs. SNR



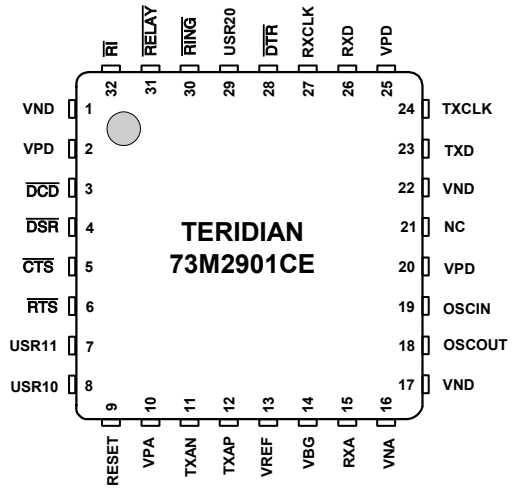
BER vs. Receive Level



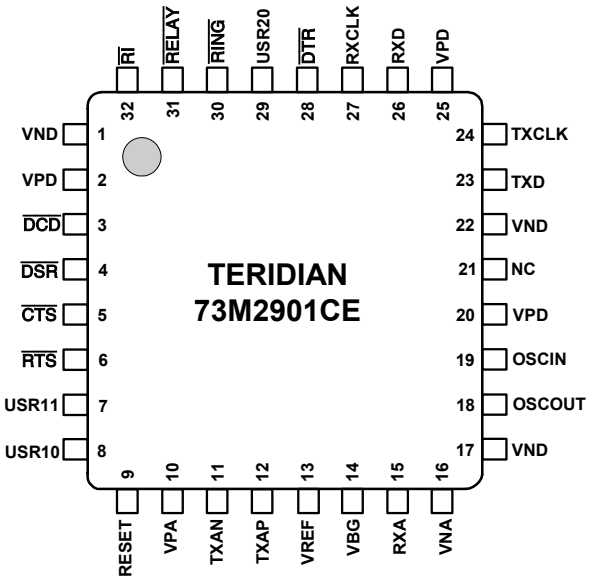
QFN AND TQFP PACKAGE PIN-OUT

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	VND	9	RESET	17	VND	25	VPD
2	VPD	10	VPA	18	OSCOUT	26	RXD
3	$\overline{\text{DCD}}$	11	TXAN	19	OSCIN	27	RXCLK
4	$\overline{\text{DSR}}$	12	TXAP	20	VPD	28	$\overline{\text{DTR}}$
5	$\overline{\text{CTS}}$	13	VREF	21	NC	29	USR20
6	$\overline{\text{RTS}}$	14	VBG	22	VND	30	$\overline{\text{RING}}$
7	USR11	15	RXA	23	TXD	31	$\overline{\text{RELAY}}$
8	USR10	16	VNA	24	TXCLK	32	$\overline{\text{RI}}$

PACKAGE PIN DESIGNATIONS (Top View)

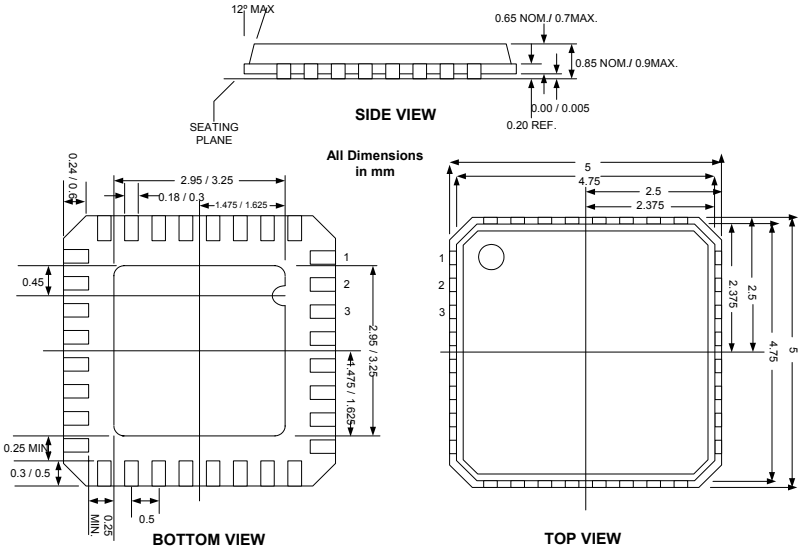


32-Pin QFN
73M2901CE-IM

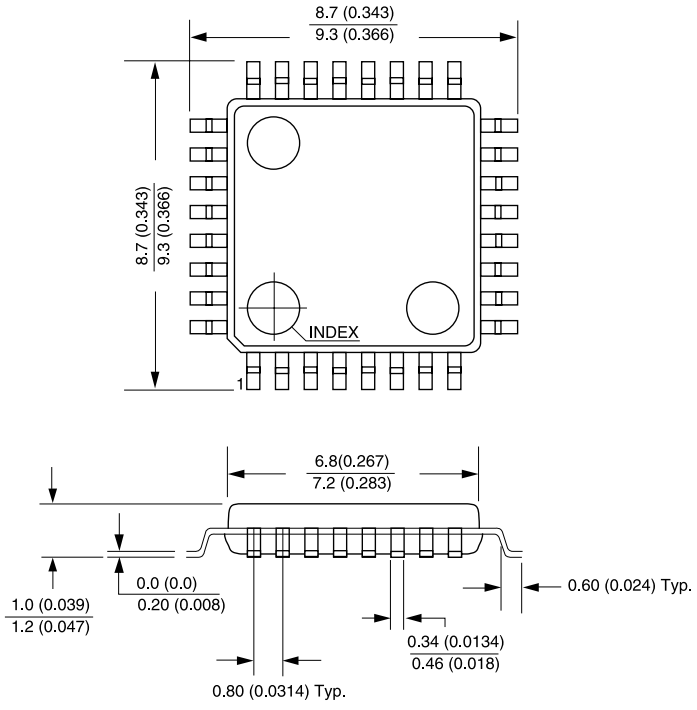


32-Pin TQFP
73M2901CE-IGV

MECHANICAL DRAWINGS



32 Pin QFN
73M2901CE-IM



32 Pin TQFP
73M2901CE-IGV

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGING MARK
73M2901CE 32-Pin QFN	73M2901CE-IM	73M2901CEIM
73M2901CE 32-Pin QFN Lead free	73M2901CE-IM/F	73M2901CEIM/F
73M2901CE 32-Pin Thin Quad Flat Pack	73M2901CE-IGV	73M2901CEIGV
73M2901CE 32-Pin Thin Quad Flat Pack Lead Free	73M2901CE-IGV/F	73M2901CEIGV/F

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