

## Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Maximum Rating condition for extended periods may affect device reliability and lifetime.

Supply Voltage.....+4.2V

Input Voltage.....-0.5V to VCC + 0.5V

Output Voltage.....-0.5V to VCC + 0.5V

Reference Frequency/Input Crystal.....10MHz to 60MHz

Storage Temperature.....-55°C to +125°C

Lead Temperature (Soldering, 10 sec).....300°C

ESD Rating (HBM - Human Body Model).....2kV

## Operating Conditions

Operating Temperature Range.....-40°C to +85°C

## Electrical Characteristics

Unless otherwise noted:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 5\%$  or  $2.5\text{V} \pm 5\%$ ,  $V_{EE} = 0\text{V}$

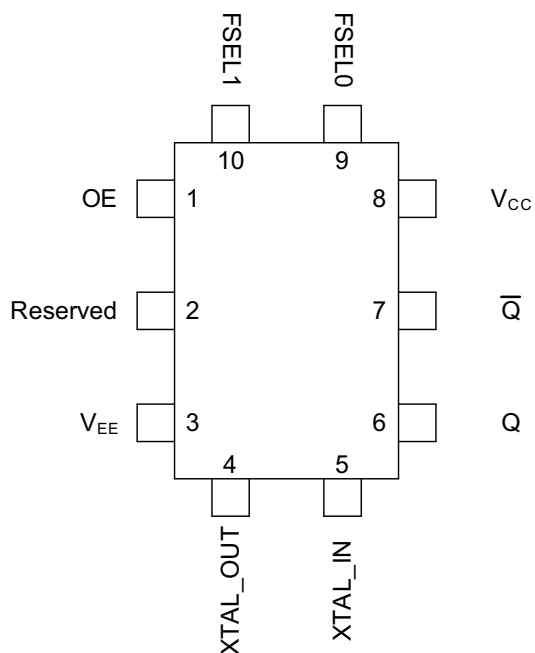
Symbol	Parameter	Conditions	*	Min	Typ	Max	Units
3.3V Power Supply DC Characteristics							
$V_{CC}$	Power Supply Voltage		•	3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current	Measured at 156.25MHz and includes the output load current			68		mA
2.5V Power Supply DC Characteristics							
$V_{CC}$	Power Supply Voltage		•	2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current	Measured at 156.25MHz and includes the output load current			58		mA

Symbol	Parameter	Conditions	*	Min	Typ	Max	Units
LVCMOS/LVTTL DC Characteristics							
$V_{IH}$	Input High Voltage	$V_{CC} = 3.465\text{V}$	•	2.42		$V_{CC} + 0.3$	V
		$V_{CC} = 2.625\text{V}$	•	1.83		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{CC} = 3.465\text{V}$	•	-0.3		1.03	V
		$V_{CC} = 2.625\text{V}$	•	-0.3		0.785	V
$I_{IH}$	Input High Current (OE, FSEL[1:0])	$V_{IN} = V_{CC} = 3.465\text{V}$ or $2.625\text{V}$	•			15	$\mu\text{A}$
$I_{IL}$	Input Low Current (OE, FSEL[1:0])	$V_{IN} = 0\text{V}$ , $V_{CC} = 3.465\text{V}$ or $2.625\text{V}$	•	-10			$\mu\text{A}$
LVPECL DC Characteristics							
$V_{OH}$	Output High Voltage		•	$V_{CC} - 1.3$		$V_{CC} - 0.4$	V
$V_{OL}$	Output Low Voltage		•	$V_{CC} - 2.0$		$V_{CC} - 1.6$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		•	0.6		1.2	V
Crystal Characteristics							
$X_{Mode}$	Mode of Oscillations			Fundamental			
$X_f$	Frequency				25		MHz
ESR	Equivalent Series Resistance					50	$\Omega$
$C_S$	Shunt Capacitance					7	pF
AC Characteristics							
$f_{OUT}$	Output Frequency	See Table 1.		100		156.25	MHz

Symbol	Parameter	Conditions	*	Min	Typ	Max	Units
$t_{jit}(\phi)$	RMS Phase Jitter	156.25MHz Integration Range 12kHz-20MHz			0.6		pS
		150MHz Integration Range 12kHz-20MHz			0.6		pS
		125MHz Integration Range 12kHz-20MHz			0.6		pS
		100MHz Integration Range 12kHz-20MHz			0.6		pS
$t_{jit}(cc)$	Cycle-to-Cycle Jitter	Using 25MHz, 18pF resonant crystal	•			10	pS
$t_R/t_F$	Output Rise/Fall Time	20% to 80%	•	100		450	pS
Odc	Output Duty Cycle		•	48		52	%

\* Limits applying over the full operating temperature range are denoted by a “•”.

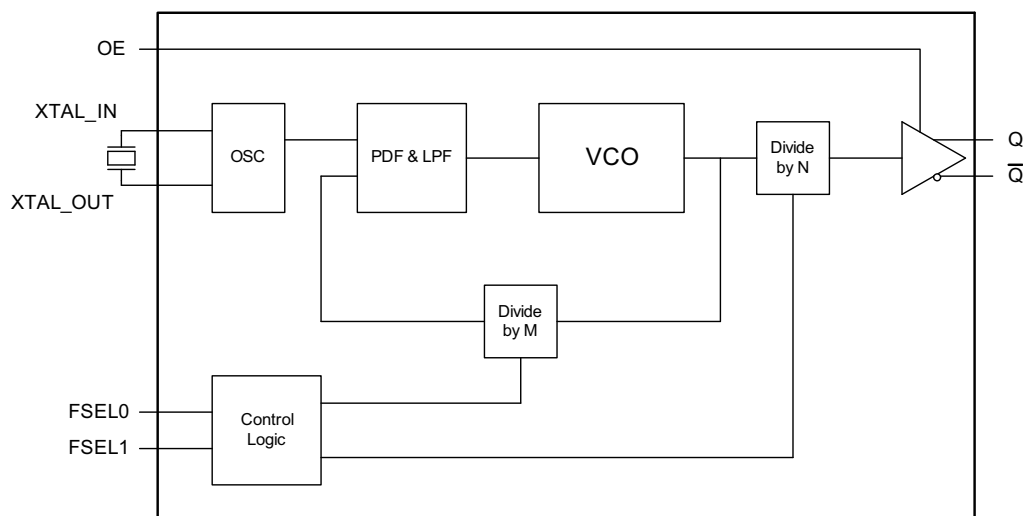
## Pin Configuration



## Pin Assignments

Pin No.	Pin Name	Type	Description
1	OE	Input (900K $\Omega$ pull-up)	Output enable pin - LVCMOS/LVTTL active high input. Outputs are enabled when OE = high. Outputs are disabled when OE = low.
2	Reserved		Reserved, leave this pin unconnected.
3	V <sub>EE</sub>	Supply	Negative supply pin.
4	XTAL_OUT	Output	Crystal oscillator output.
5	XTAL_IN	Input	Crystal oscillator input.
6	Q	Output	Positive LVPECL output.
7	$\bar{Q}$	Output	Inverted LVPECL output.
8	V <sub>CC</sub>	Supply	Power supply pin.
9	FSEL0	Input (900K $\Omega$ pull-dwn)	Output frequency select pin, LSB (LVCMOS/LVTTL input).
10	FSEL1	Input (900K $\Omega$ pull-dwn)	Output frequency select pin, MSB (LVCMOS/LVTTL input).

## Functional Block Diagram



## Typical Performance Characteristics

Figures 1,2,3 and 4 show typical phase noise performance plots for 156.25 MHz, 150MHz, 125M, and 100MHz clock outputs respectively. The data was taken using the industry standard Agilent E5052B instrument. The integration range is the widely referenced 12KHz to 20MHz range most often used in WAN applications.

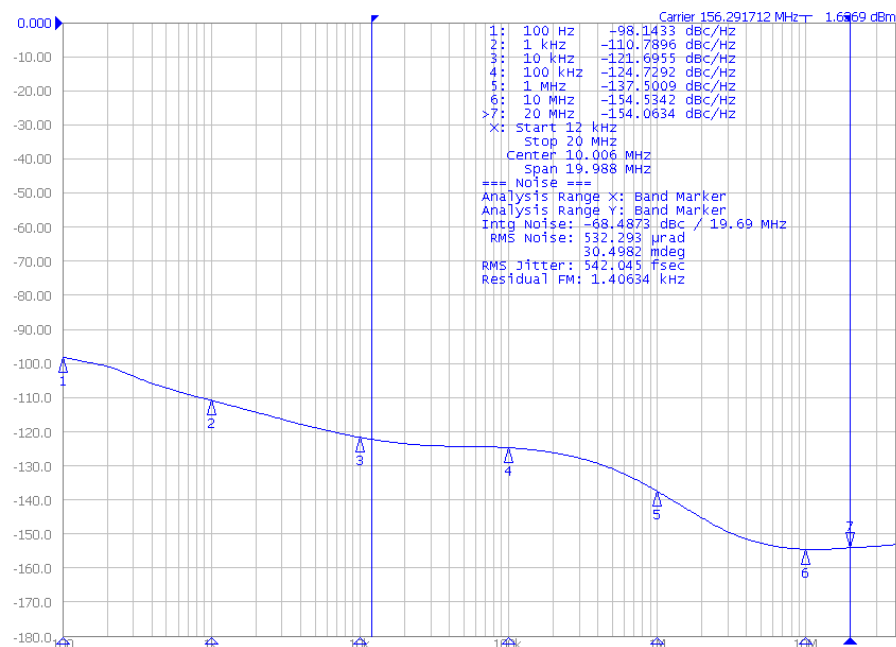


Figure 1: 156.25MHz Operation, Phase Noise at 3.3V

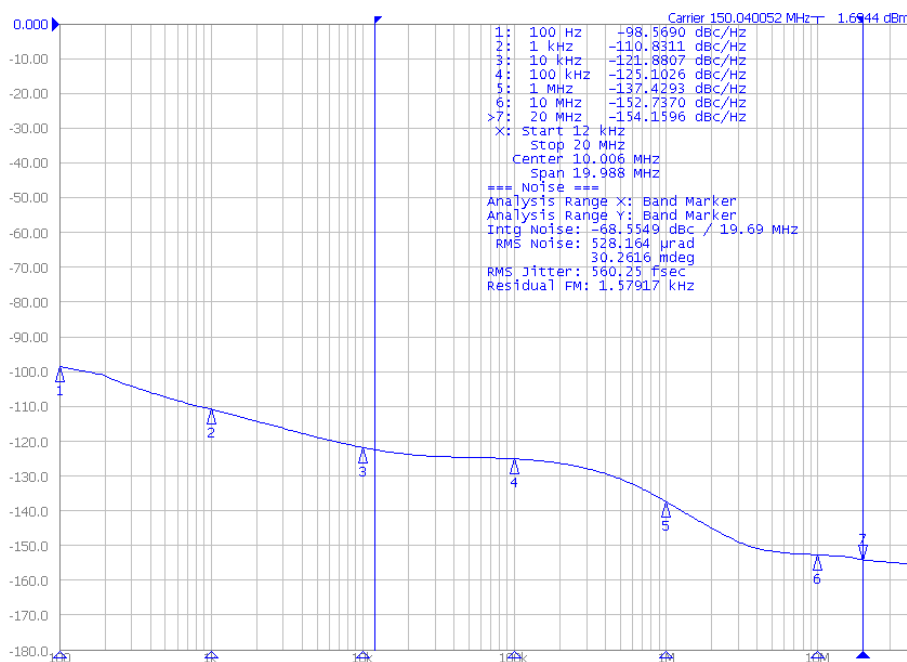


Figure 2: 150MHz Operation, Phase Noise at 3.3V)

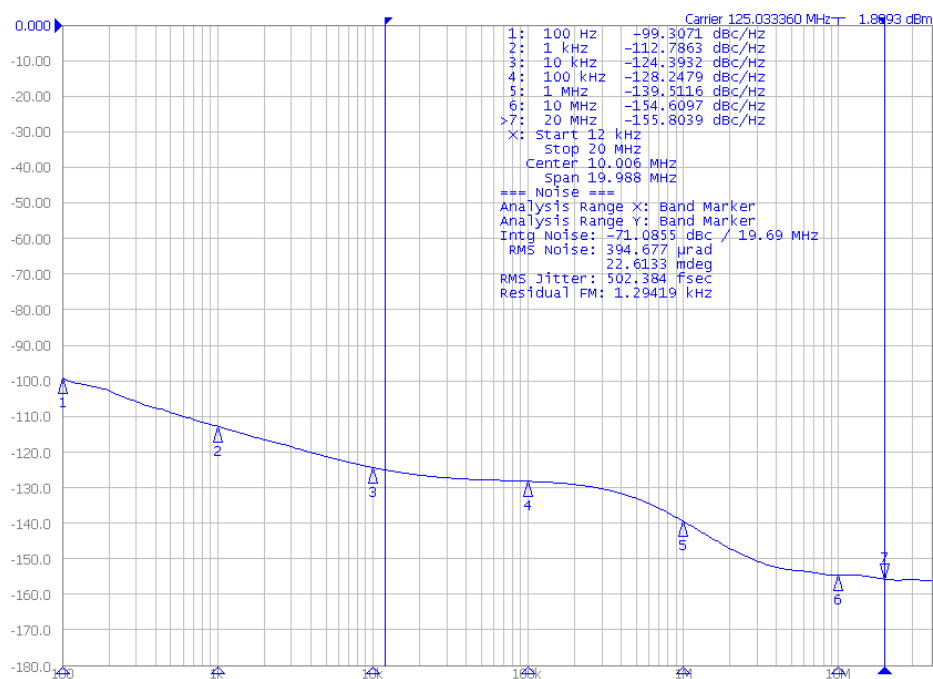


Figure 3: 125MHz Operation, Phase Noise at 3.3V

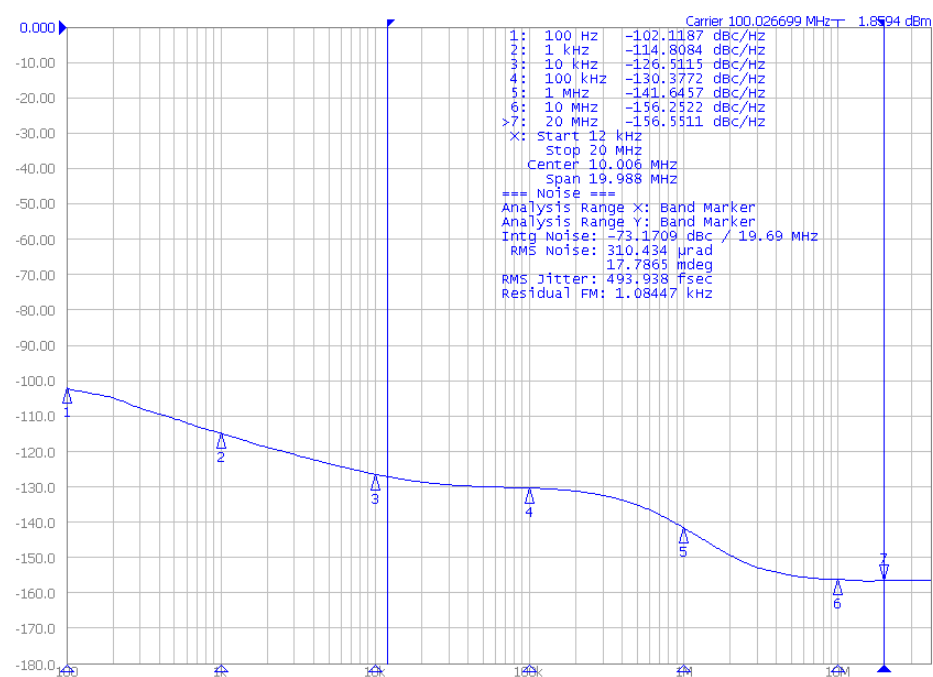


Figure 4: 100MHz Operation, Phase Noise at 3.3V

## Application Information

### Functional Truth Table

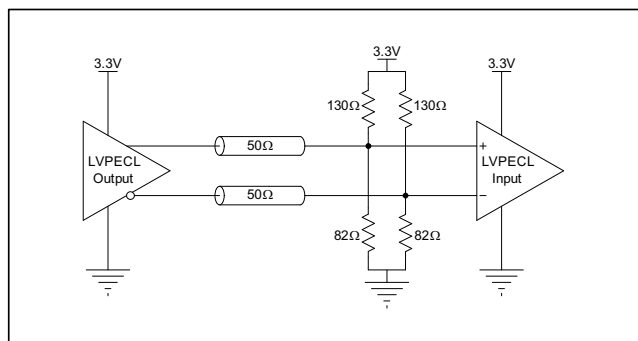
The XR81111-CA04 has two frequency select pins, FSLEL[1:0], that determine the output frequency from the device. With the two FSEL inputs, one of 4 different clock rates can be selected. This allows the XR81111-CA04 to support a variety of applications such as PCI Express, Ethernet, SAS and 10GE for example. If the FSEL pins are left floating, the XR81111-CA04 will default (with internal pull-down resistors on the FSEL inputs) to the 100MHz output configuration.

**Table 1: Output Frequency Selection**

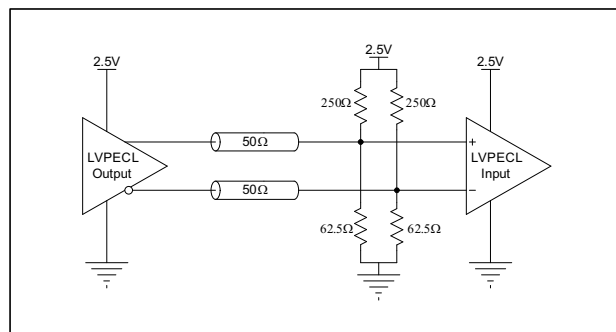
FSEL[1:0]	XTAL (MHz)	Output Frequency (MHz)	Applications
00	25	100	PCI Express
01	25	125	Ethernet
10	25	150	SAS
11	25	156.25	10GE, XAUI

### Termination for LVPECL Outputs

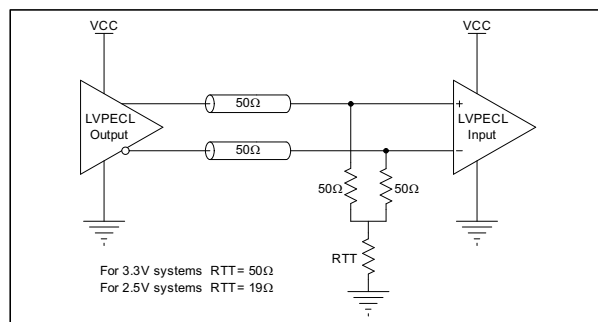
The termination schemes shown in Figure 5 and Figure 6 are typical for LVPECL outputs. Matched impedance layout techniques should be used for the LVPECL output pairs to minimize any distortion that could impact your maximum operating frequency. Figure 7 is an alternate termination scheme that uses a Y-termination approach.



**Figure 5: XR81111 3.3V LVPECL Output Termination**



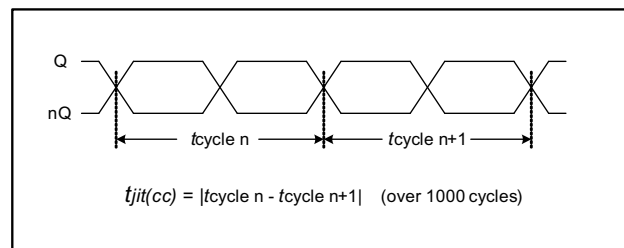
**Figure 6: XR81111 2.5V LVPECL Output Termination**



**Figure 7: XR81111 Alternate LVPECL Output Termination Using Y-termination**

### Output Signal Timing Definitions

The following diagrams clarify the common definitions of the AC timing measurements.



**Figure 8: Cycle-to-Cycle Jitter**



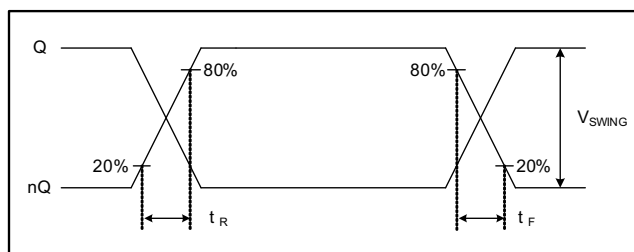


Figure 9: Output Rise/Fall Time and Swing

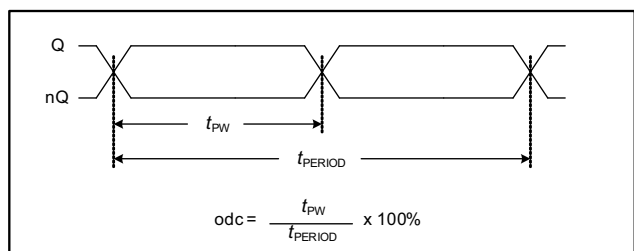
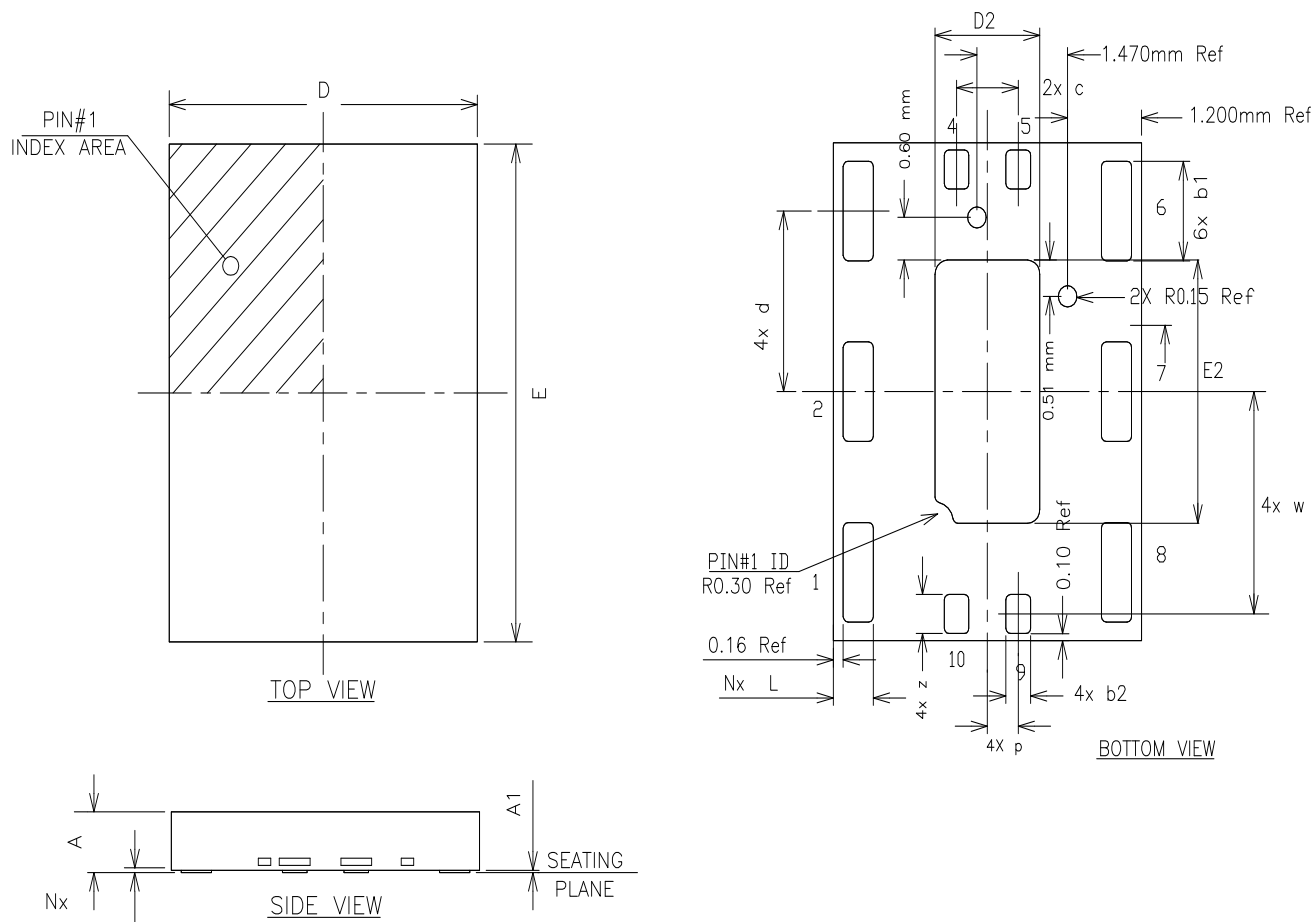


Figure 10: Output Period and Duty Cycle

## Mechanical Dimensions

### 10-Pin QFN



10LD 5x7mm QFN 1.00/2.54 PITCH						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
b1	1.35	1.40	1.45	0.053	0.055	0.057
b2	0.35	0.40	0.45	0.014	0.016	0.018
c	1.00 REF			0.039 REF		
d	2.54 REF			0.100 REF		
D	5.00 BSC			0.200 BSC		
E	7.00 BSC			0.280 BSC		
D2	1.55	1.70	1.80	0.061	0.067	0.071
E2	3.55	3.70	3.80	0.140	0.146	0.150
L	0.55	0.65	0.75	0.022	0.026	0.030
w	3.125 REF			0.123 BSC		
p	0.50 REF			0.020 BSC		
z	0.55 REF			0.022 BSC		
N	10			10		
ND	2			2		
NE	3			3		

## Ordering Information

Part Number	Package	Green	Operating Temperature Range	Shipping Packaging	Marking
XR81111-CA04-F	10-pin QFN	Yes	-40°C to +85°C	Tube/Tray	T111
XR81111-CA04TR-F	10-pin QFN	Yes	-40°C to +85°C	Tape & Reel	T111
XR81111EVB	Eval Board	N/A	N/A	N/A	N/A

## Revision History

Revision	Date	Description
1A	April 2014	Initial release.
1B	April 28, 2014	Updates to general description and package drawing. [ECN1421-15   05/25/2014]

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