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1 Block diagram and pin configuration

Figure 1. Block diagram

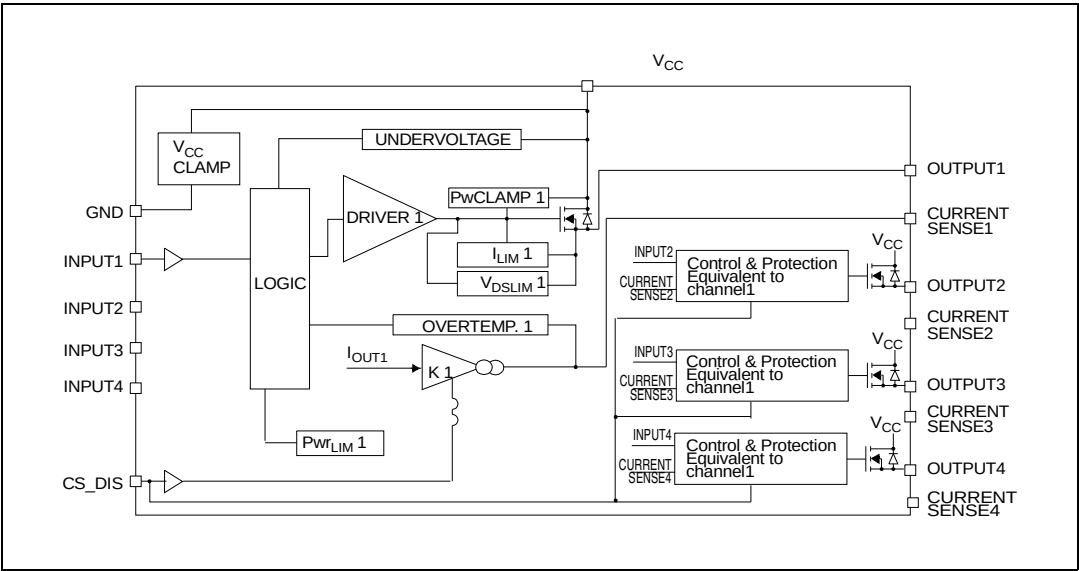


Table 2. Pin functions

Name	Function
V _{CC}	Battery connection.
OUTPUT _n	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode / resistor network.
INPUT _n	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
CURRENT SENSE _n	Analog current sense pin, delivers a current proportional to the load current.
CS_DIS	Active high CMOS compatible pin to disable the current sense pin.

Figure 2. Configuration diagram (top view)

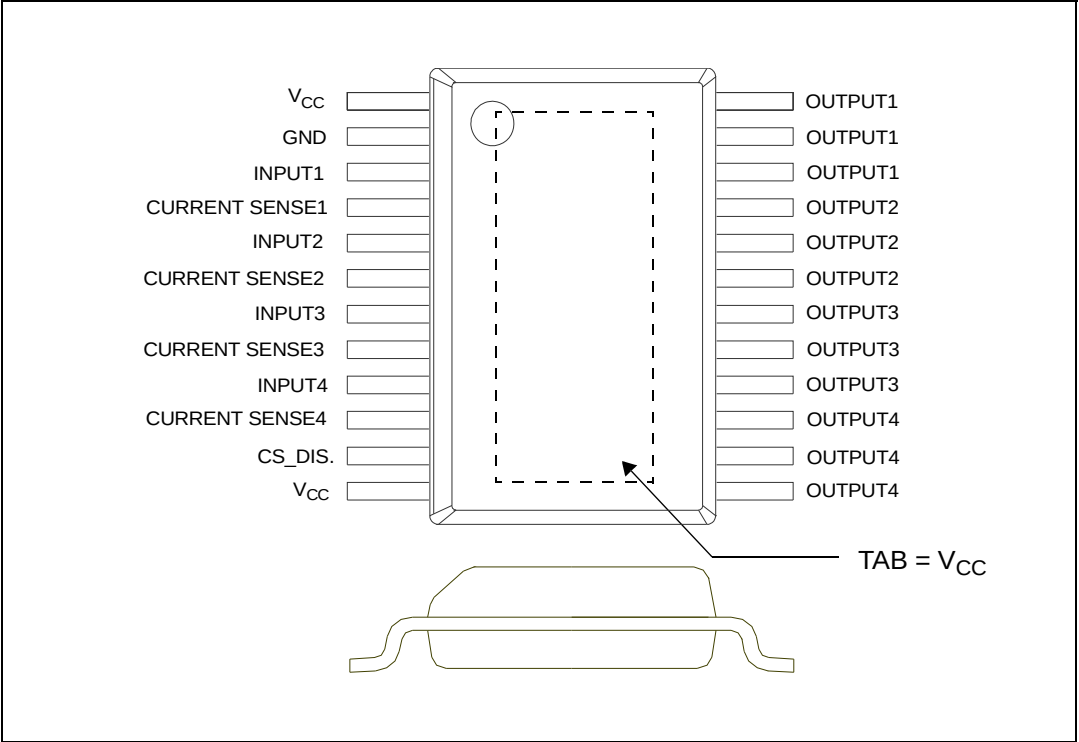


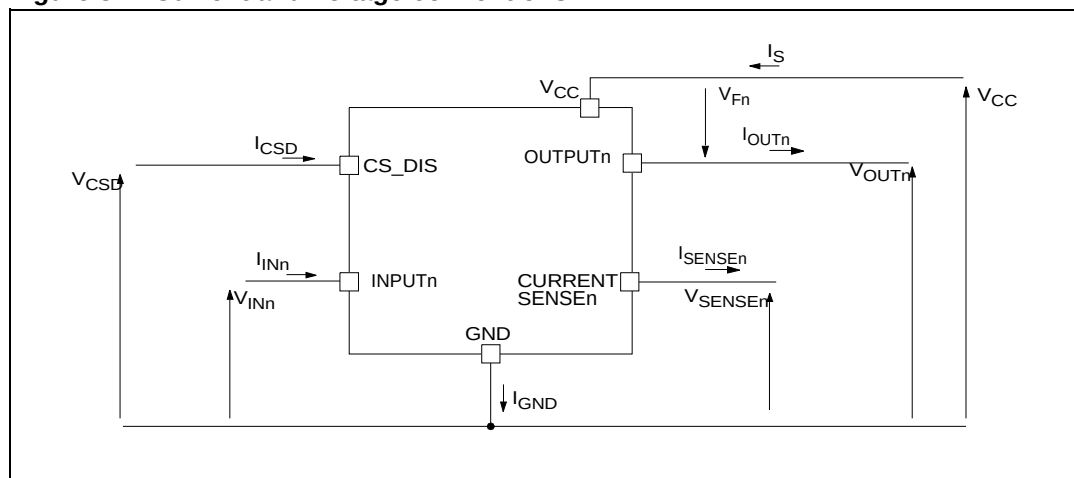
Table 3. Suggested connections for unused and not connected pins

Connection / pin	Current Sense	N.C.	Output	Input	CS_DIS
Floating	N.R. ⁽¹⁾	X	X	X	X
To ground	Through 1 kΩ resistor	X	N.R.	Through 10 kΩ resistor	Through 10 kΩ resistor

1. Not recommended.

2 Electrical specifications

Figure 3. Current and voltage conventions



Note: $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the “Absolute maximum ratings” tables may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in this section for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	24	A
I_{IN}	DC Input current	-1 to 10	mA
I_{CSD}	DC Current Sense disable Input current	-1 to 10	mA
$-I_{CSENSE}$	DC Reverse CS pin current	200	mA
V_{CSENSE}	Current Sense maximum voltage	$V_{CC}-41$ $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) ($L=0.8$ mH; $R_L=0\Omega$; $V_{bat}=13.5V$; $T_{jstart}=150^\circ C$; $I_{OUT} = I_{limL}(Typ.)$)	140	mJ

Table 4. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (human body model: $R=1.5K\Omega$; $C=100pF$)		
	– Input	4000	V
	– Current sense	2000	V
	– CS_DIS	4000	V
	– Output	5000	V
	– V_{CC}	5000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	- 40 to 150	°C
T_{stg}	Storage temperature	- 55 to 150	°C

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max value	Unit
$R_{thj-case}$	Thermal resistance junction-case (with one channel ON)	1.35	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	See Figure 29 .	°C/W

2.3 Electrical characteristics

Values specified in this section are for $8\text{ V} < V_{CC} < 36\text{ V}$, $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$, unless otherwise stated.

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	36	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shut-down hysteresis			0.5		V
R_{ON}	On-state resistance	$I_{OUT} = 3\text{ A}$; $T_j = 25^{\circ}\text{C}$ $I_{OUT} = 3\text{ A}$; $T_j = 150^{\circ}\text{C}$ $I_{OUT} = 3\text{ A}$; $V_{CC} = 5\text{ V}$; $T_j = 25^{\circ}\text{C}$			27 54 37	$\text{m}\Omega$ $\text{m}\Omega$ $\text{m}\Omega$
V_{clamp}	Clamp voltage	$I_S = 20\text{ mA}$	41	46	52	V
I_S	Supply current	Off-state; $V_{CC} = 13\text{ V}$; $T_j = 25^{\circ}\text{C}$; $V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0\text{ V}$ On-state; $V_{CC} = 13\text{ V}$; $V_{IN} = 5\text{ V}$; $I_{OUT} = 0\text{ A}$		2 ⁽¹⁾ 8	5 ⁽¹⁾ 14	μA mA
$I_{L(off)}$	Off-state output current ⁽²⁾	$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 25^{\circ}\text{C}$ $V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 125^{\circ}\text{C}$	0 0	0.01	3 5	μA
V_F	Output - V_{CC} diode voltage ⁽²⁾	$-I_{OUT} = 3\text{ A}$; $T_j = 150^{\circ}\text{C}$			0.7	V

1. PowerMOS leakage included.

2. For each channel.

Table 7. Switching ($V_{CC} = 13\text{ V}$; $T_j = 25^{\circ}\text{C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 4.3\Omega$ (see Figure 6.)		40		μs
$t_{d(off)}$	Turn-off delay time	$R_L = 4.3\Omega$ (see Figure 6.)		40		μs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L = 4.3\Omega$		See Figure 19.		$\text{V}/\mu\text{s}$
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L = 4.3\Omega$		See Figure 21.		$\text{V}/\mu\text{s}$
W_{ON}	Switching energy losses during t_{won}	$R_L = 4.3\Omega$ (see Figure 6.)		0.2		mJ
W_{OFF}	Switching energy losses during t_{woff}	$R_L = 4.3\Omega$ (see Figure 6.)		0.3		mJ

Table 8. Current Sense ($8V < V_{CC} < 16V$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	$I_{OUT} = 0.5A$; $V_{SENSE} = 0.5V$; $V_{CSD} = 0V$; $T_J = -40^{\circ}C \dots 150^{\circ}C$	1680	2910	4120	
$dK_0/K_0^{(1)}$	Current sense ratio drift	$I_{OUT} = 0.5A$; $V_{SENSE} = 0.5V$; $V_{CSD} = 0V$; $T_J = -40^{\circ}C$ to $150^{\circ}C$	-12		12	%
K_1	I_{OUT}/I_{SENSE}	$I_{OUT} = 2A$; $V_{SENSE} = 4V$; $V_{CSD} = 0V$; $T_J = -40^{\circ}C \dots 150^{\circ}C$ $T_J = 25^{\circ}C \dots 150^{\circ}C$	2050 2190	2700 2700	3410 3210	
$dK_1/K_1^{(1)}$	Current sense ratio drift	$I_{OUT} = 2A$; $V_{SENSE} = 4V$; $V_{CSD} = 0V$; $T_J = -40^{\circ}C$ to $150^{\circ}C$	-10		10	%
K_2	I_{OUT}/I_{SENSE}	$I_{OUT} = 3A$; $V_{SENSE} = 4V$; $V_{CSD} = 0V$; $T_J = -40^{\circ}C \dots 150^{\circ}C$ $T_J = 25^{\circ}C \dots 150^{\circ}C$	2260 2350	2690 2690	3160 3030	
$dK_2/K_2^{(1)}$	Current sense ratio drift	$I_{OUT} = 3A$; $V_{SENSE} = 4V$; $V_{CSD} = 0V$; $T_J = -40^{\circ}C$ to $150^{\circ}C$	-7		7	%
K_3	I_{OUT} / I_{SENSE}	$I_{OUT} = 10A$; $V_{SENSE} = 4V$; $V_{CSD} = 0V$; $T_J = -40^{\circ}C \dots 150^{\circ}C$ $T_J = 25^{\circ}C \dots 150^{\circ}C$	2490 2590	2700 2700	2870 2800	
$dK_3/K_3^{(1)}$	Current sense ratio drift	$I_{OUT} = 10A$; $V_{SENSE} = 4V$; $V_{CSD} = 0V$; $T_J = -40^{\circ}C$ to $150^{\circ}C$	-4		4	%
I_{SENSE0}	Analog sense leakage current	$I_{OUT} = 0A$; $V_{SENSE} = 0V$; $V_{CSD} = 5V$; $V_{IN} = 0V$; $T_J = -40^{\circ}C \dots 150^{\circ}C$ $V_{CSD} = 0V$; $V_{IN} = 5V$; $T_J = -40^{\circ}C \dots 150^{\circ}C$ $I_{OUT} = 2A$; $V_{SENSE} = 0V$; $V_{CSD} = 5V$; $V_{IN} = 5V$; $T_J = -40^{\circ}C \dots 150^{\circ}C$	0 0 0		1 2 1	μA μA μA
I_{OL}	open load on-state current detection threshold	$V_{IN} = 5V$, $I_{SENSE} = 5\mu A$	5		30	mA
V_{SENSE}	Max analog sense output voltage	$I_{OUT} = 3A$; $V_{CSD} = 0V$	5			V

Table 8. Current Sense (8V<V_{CC}<16V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SENSEH}	Analog sense output voltage in over temperature condition	V _{CC} = 13V; R _{SENSE} = 3.9KΩ		9		V
I _{SENSEH}	Analog sense output current in over temperature condition	V _{CC} = 13V; V _{SENSE} = 5V		8		mA
t _{DSENSE1H}	Delay response time from falling edge of CS_DIS pin	V _{SENSE} <4V, 0.5A<I _{out} <10A I _{SENSE} = 90% of I _{SENSE max} (see Figure 4.)		50	100	μs
t _{DSENSE1L}	Delay response time from rising edge of CS_DIS pin	V _{SENSE} <4V, 0.5A<I _{out} <10A I _{SENSE} =10% of I _{SENSE max} (see Figure 4.)		5	20	μs
t _{DSENSE2H}	Delay response time from rising edge of INPUT pin	V _{SENSE} <4V, 0.5A<I _{out} <10A I _{SENSE} =90% of I _{SENSE max} (see Figure 4.)		70	300	μs
Δt _{DSENSE2H}	Delay response time between rising edge of output current and rising edge of current sense	V _{SENSE} < 4V, I _{SENSE} = 90% of I _{SENSEMAX} , I _{OUT} = 90% of I _{OUTMAX} I _{OUTMAX} =2A (see Figure 5)			200	□□μs
t _{DSENSE2L}	Delay response time from falling edge of input pin	V _{SENSE} <4V, 0.5A<I _{out} <10A I _{SENSE} =10% of I _{SENSE max} (see Figure 4.)		100	250	μs

1. Parameter guaranteed by design; it is not tested.

Table 9. Protection⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{limH}	DC short circuit current	V _{CC} =13V 5V<V _{CC} <36V	29	42	59 59	A A
I _{limL}	Short circuit current during thermal cycling	V _{CC} =13V; T _R <T _J <T _{TSD}		16		A
T _{TSD}	Shutdown temperature		150	175	200	°C
T _R	Reset temperature		T _{RS} + 1	T _{RS} + 5		°C
T _{RS}	Thermal reset of STATUS		135			°C
T _{HYST}	Thermal hysteresis (T _{TSD} -T _R)			7		°C
V _{DEMAG}	Turn-off output voltage clamp	I _{OUT} = 2A; V _{IN} =0; L=6mH	V _{CC} -41	V _{CC} -46	V _{CC} -52	V
V _{ON}	Output voltage drop limitation	I _{OUT} =0.2A; T _J =-40°C...150°C (see Figure 9.)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	$V_{IN}=0.9V$	1			μA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	$V_{IN}=2.1V$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	$I_{IN}=1mA$ $I_{IN}=-1mA$	5.5	-0.7	7	V V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	$V_{CSD}=0.9V$	1			μA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	$V_{CSD}=2.1V$			10	μA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	$I_{CSD}=1mA$ $I_{CSD}=-1mA$	5.5	-0.7	7	V V

Figure 4. Current sense delay characteristics

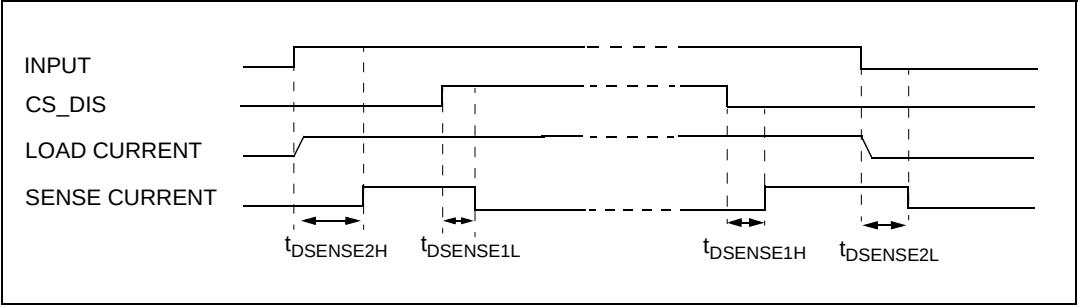


Figure 5. Delay response time between rising edge of output current and rising edge of Current Sense (CS enabled)

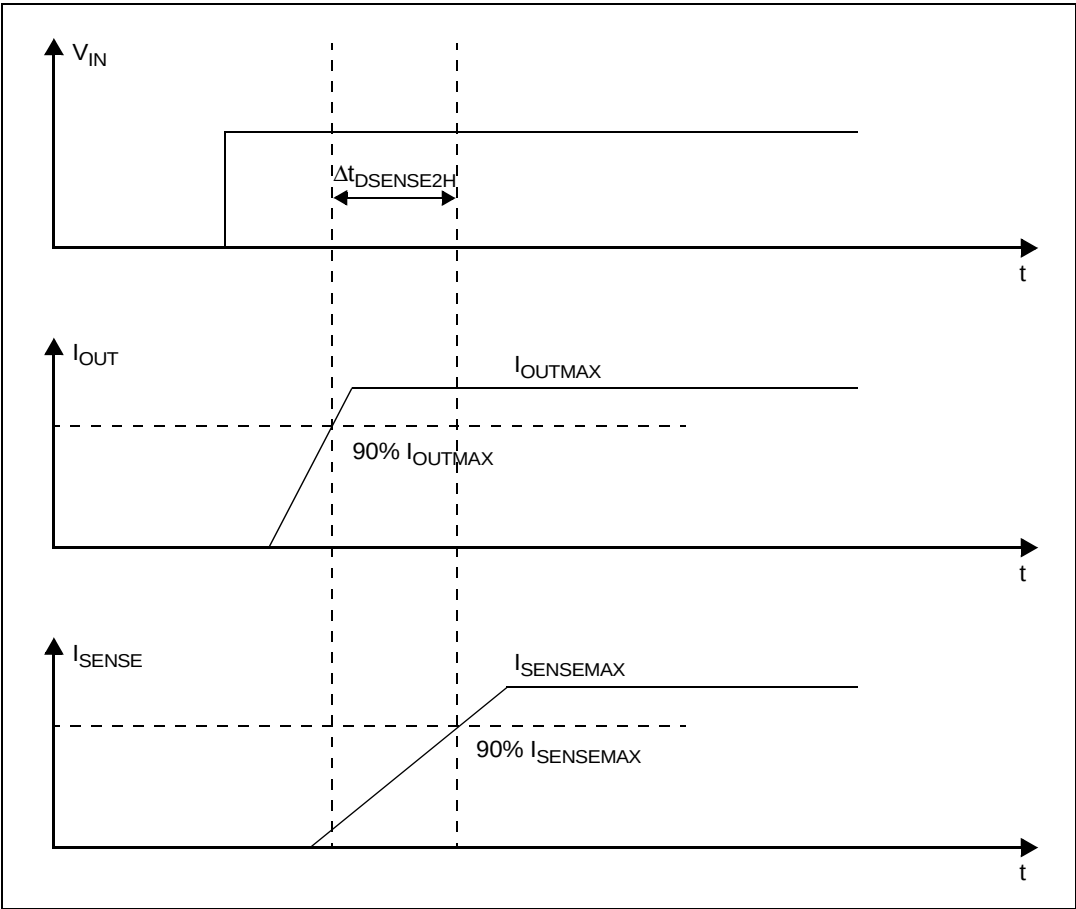


Figure 6. Switching characteristics

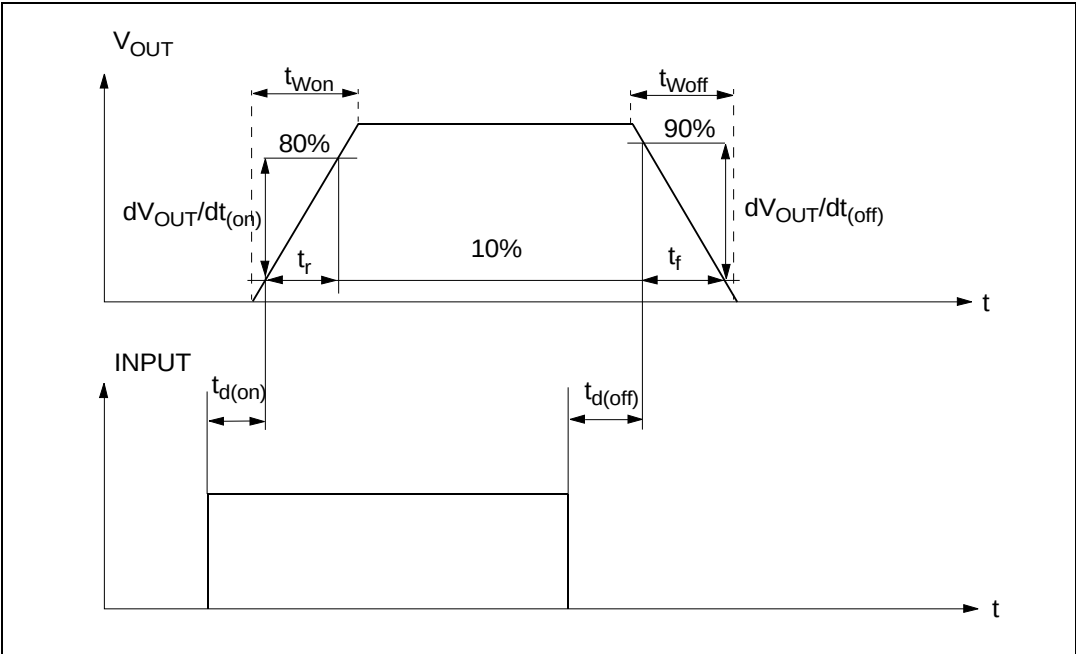


Figure 7. I_{OUT}/I_{SENSE} vs I_{OUT}

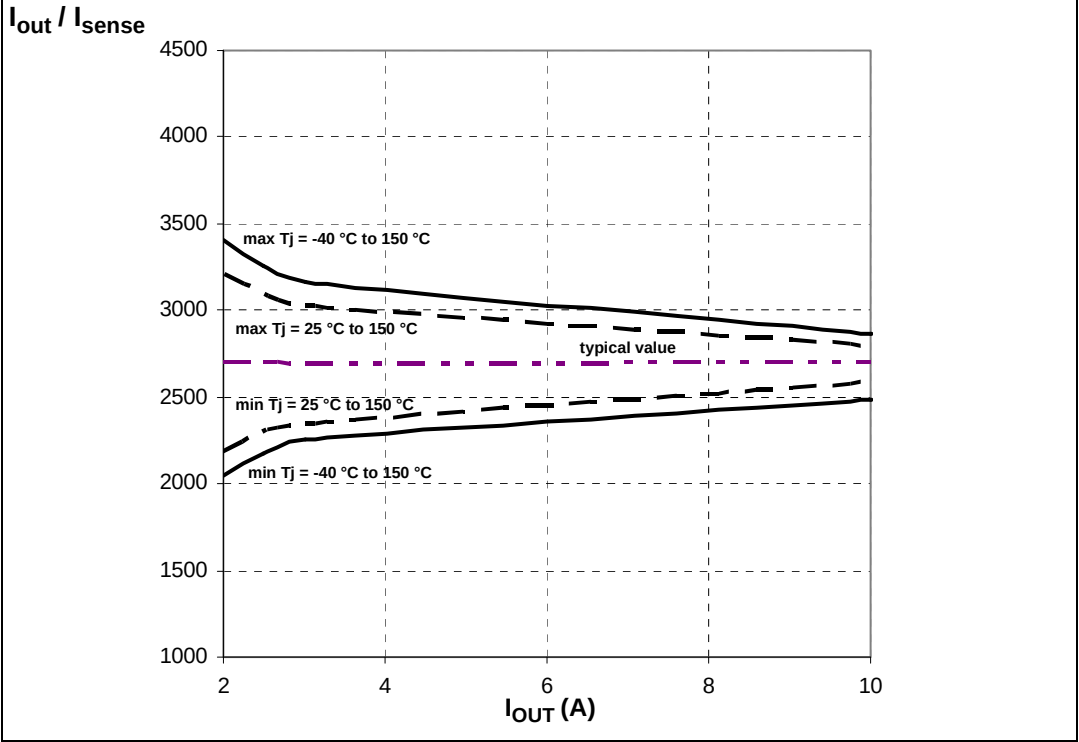
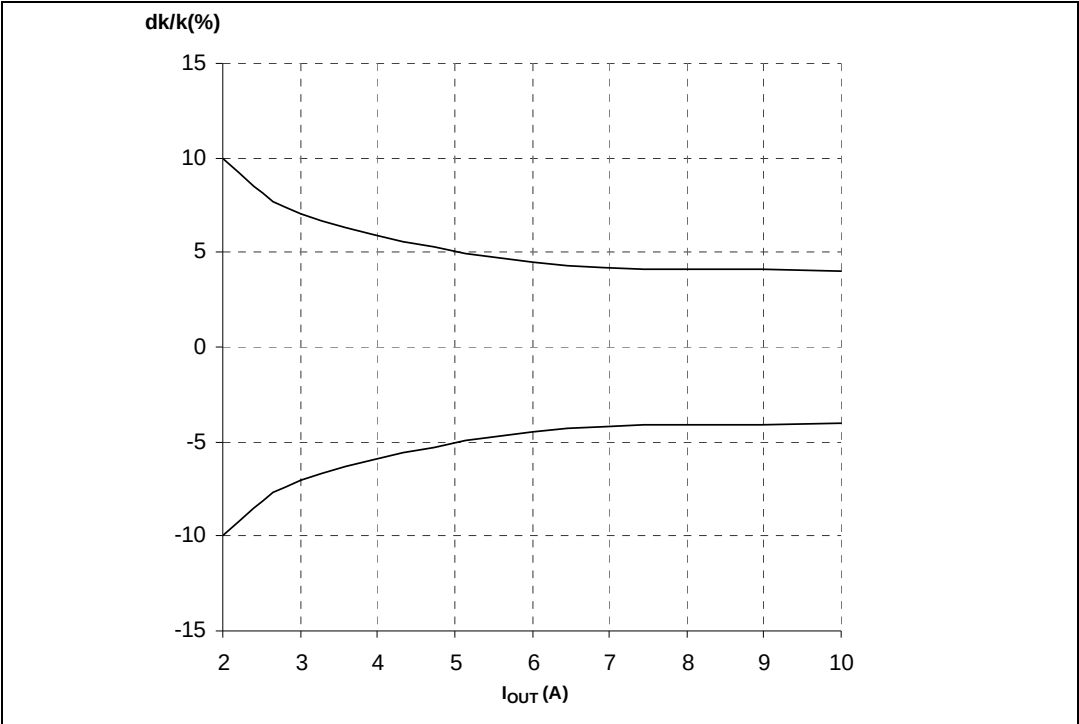


Figure 8. Maximum current sense ratio drift vs load current



Note: Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	Input	Output	Sense ($V_{CSD}=0V$) ⁽¹⁾
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Short circuit to GND ($R_{sc} \leq 10\text{ m}\Omega$)	L	L	0
	H	L	0 if $T_j < T_{TSD}$
	H	L	V_{SENSEH} if $T_j > T_{TSD}$
Short circuit to V_{CC}	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Figure 9. Output voltage drop limitation

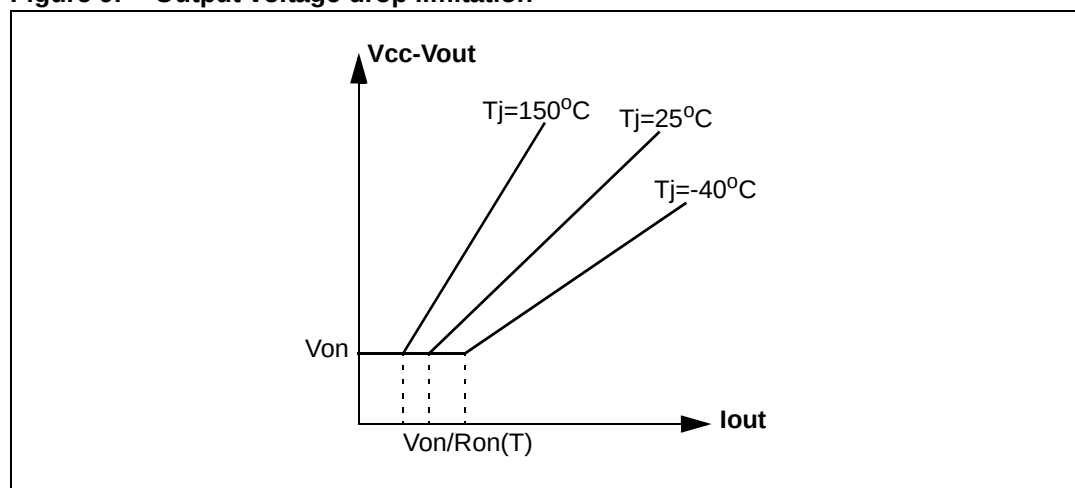


Table 12. Electrical transient requirements (part 1/3)

ISO 7637-2: 2004(E) test pulse	Test levels		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 μ s, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω

Table 12. Electrical transient requirements (part 1/3) (continued)

ISO 7637-2: 2004(E) test pulse	Test levels		Number of pulses or test times	Burst cycle/pulse repetition time	Delays and Impedance
	III	IV			
4	-6 V	-7 V	1 pulse		100 ms, 0.01 Ω
5b ⁽²⁾	+65 V	+87 V	1 pulse		400 ms, 2 Ω

Table 13. Electrical transient requirements (part 2/3)

ISO 7637-2: 2004(E) test pulse	Test level results ⁽¹⁾	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b ⁽²⁾	C	C

1. The above test levels must be considered referred to $V_{cc} = 13.5V$ except for pulse 5b.

2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 14. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Electrical characteristics curves

Figure 10. Off-state output current

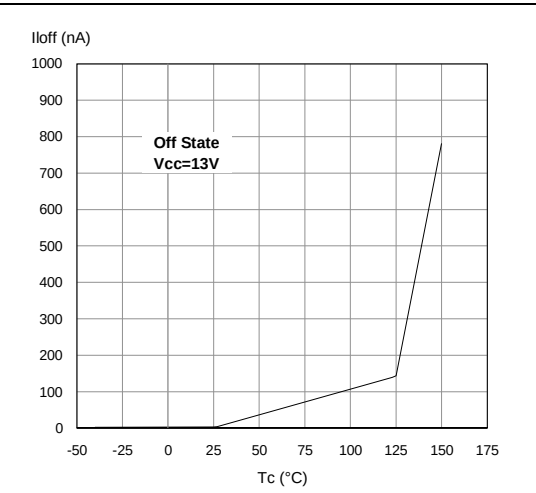


Figure 11. High level input current

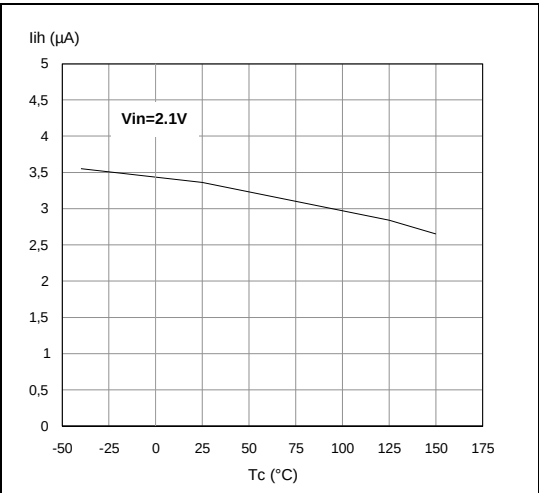


Figure 12. Input clamp voltage

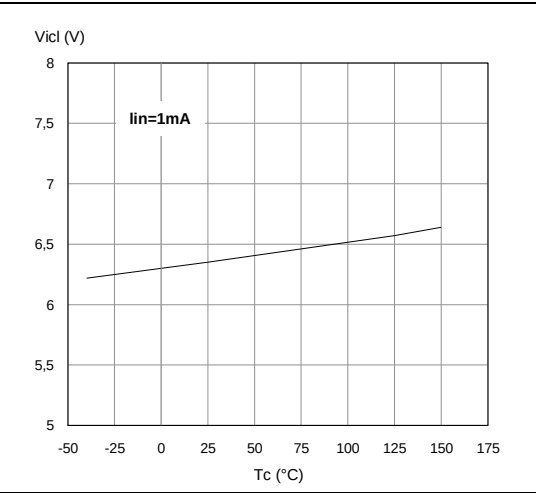


Figure 13. Input low level

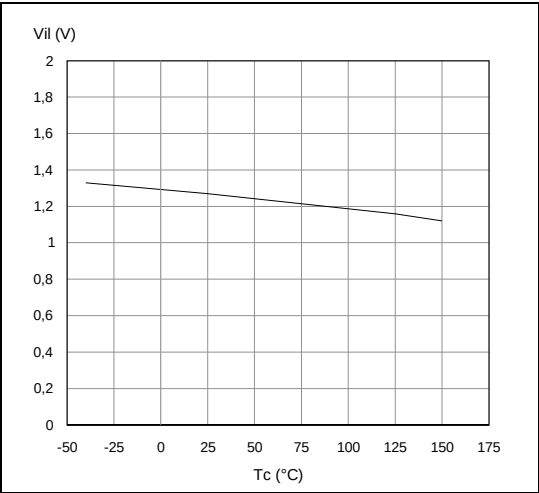


Figure 14. Input high level

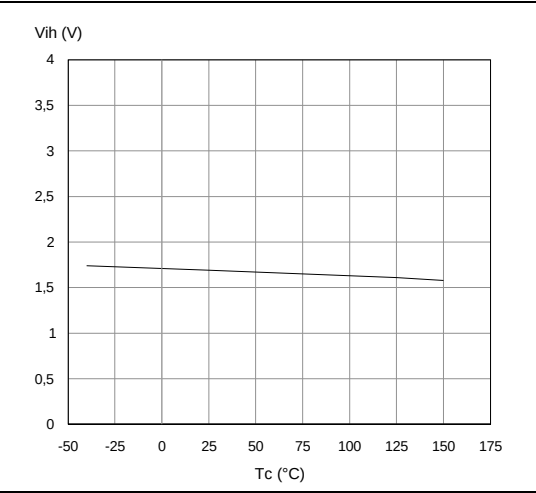


Figure 15. Input hysteresis voltage

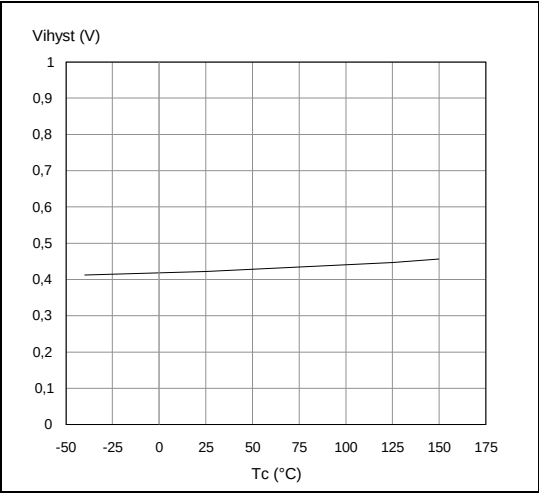


Figure 16. On-state resistance vs T_{case}

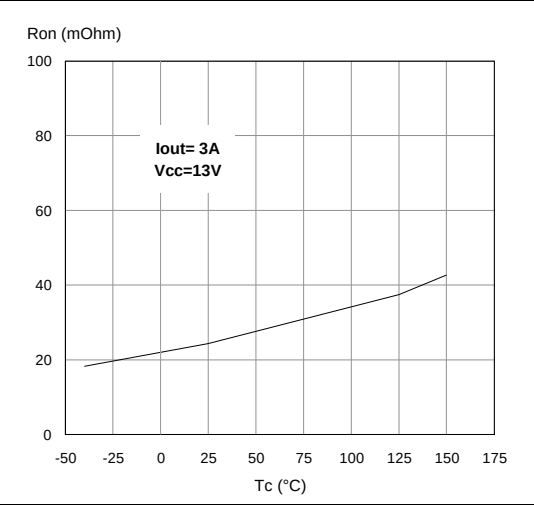


Figure 17. On-state resistance vs V_{CC}

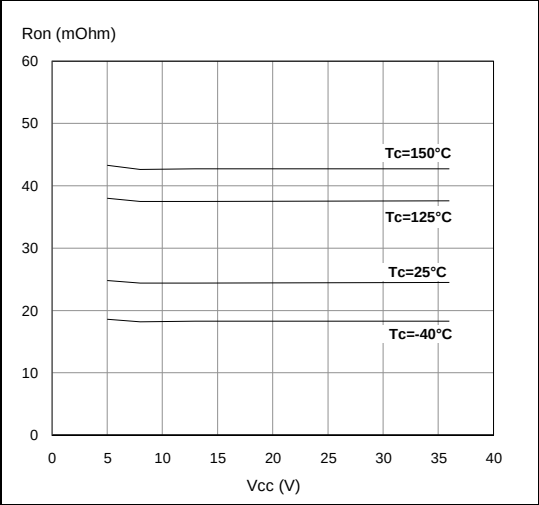


Figure 18. Undervoltage shutdown

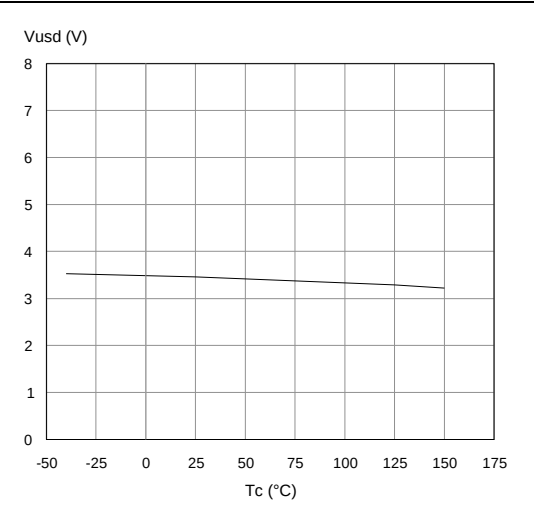


Figure 19. Turn-on voltage slope

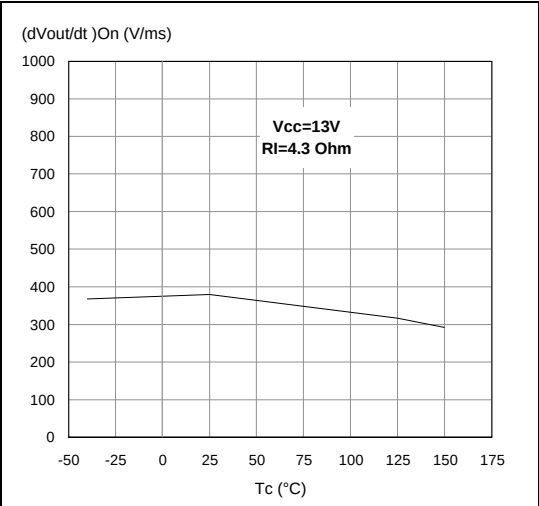


Figure 20. I_{LIMH} vs T_{case}

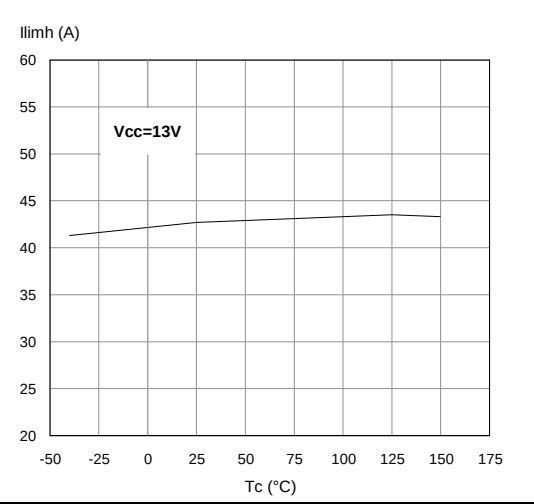


Figure 21. Turn-off voltage slope

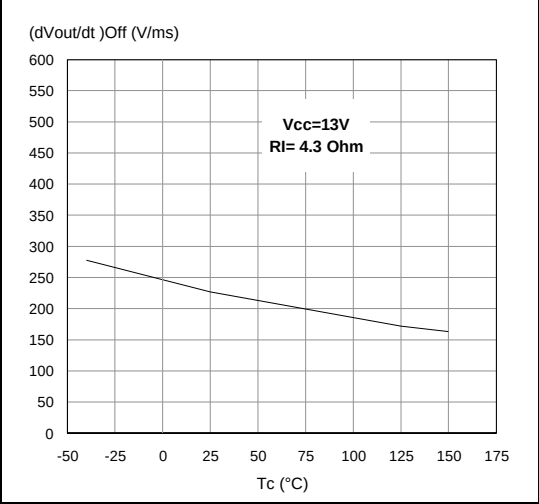


Figure 22. CS_DIS high level voltage

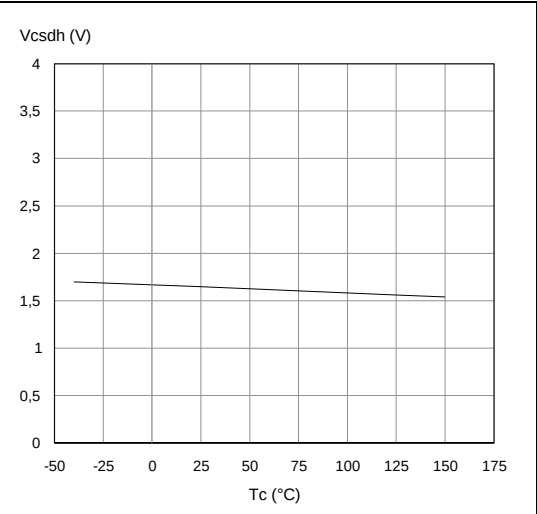


Figure 23. CS_DIS clamp voltage

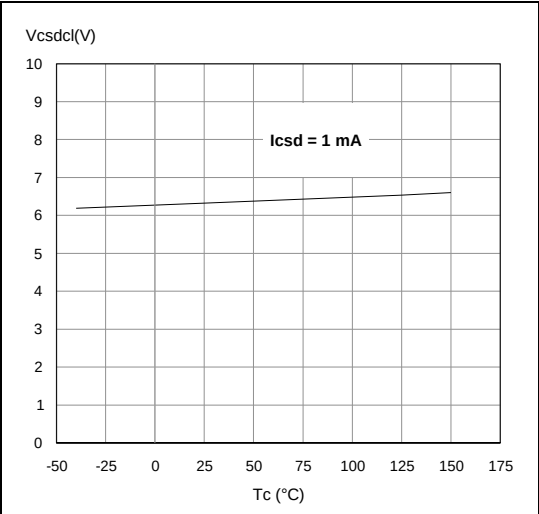
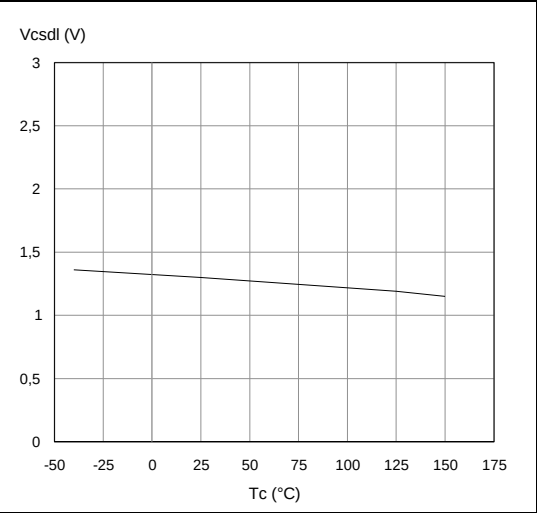
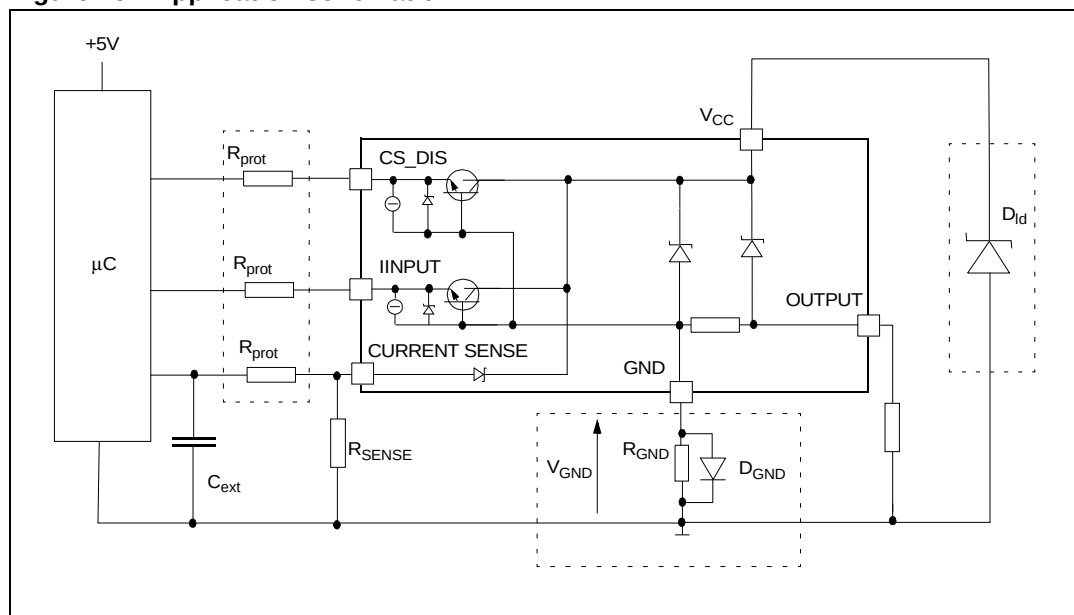


Figure 24. CS_DIS low level voltage



3 Application information

Figure 25. Application schematic



Note: Channel 2, 3, 4 have the same internal circuit as channel 1.

3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor ($R_{GND} = 1k\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ($\approx 600mV$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

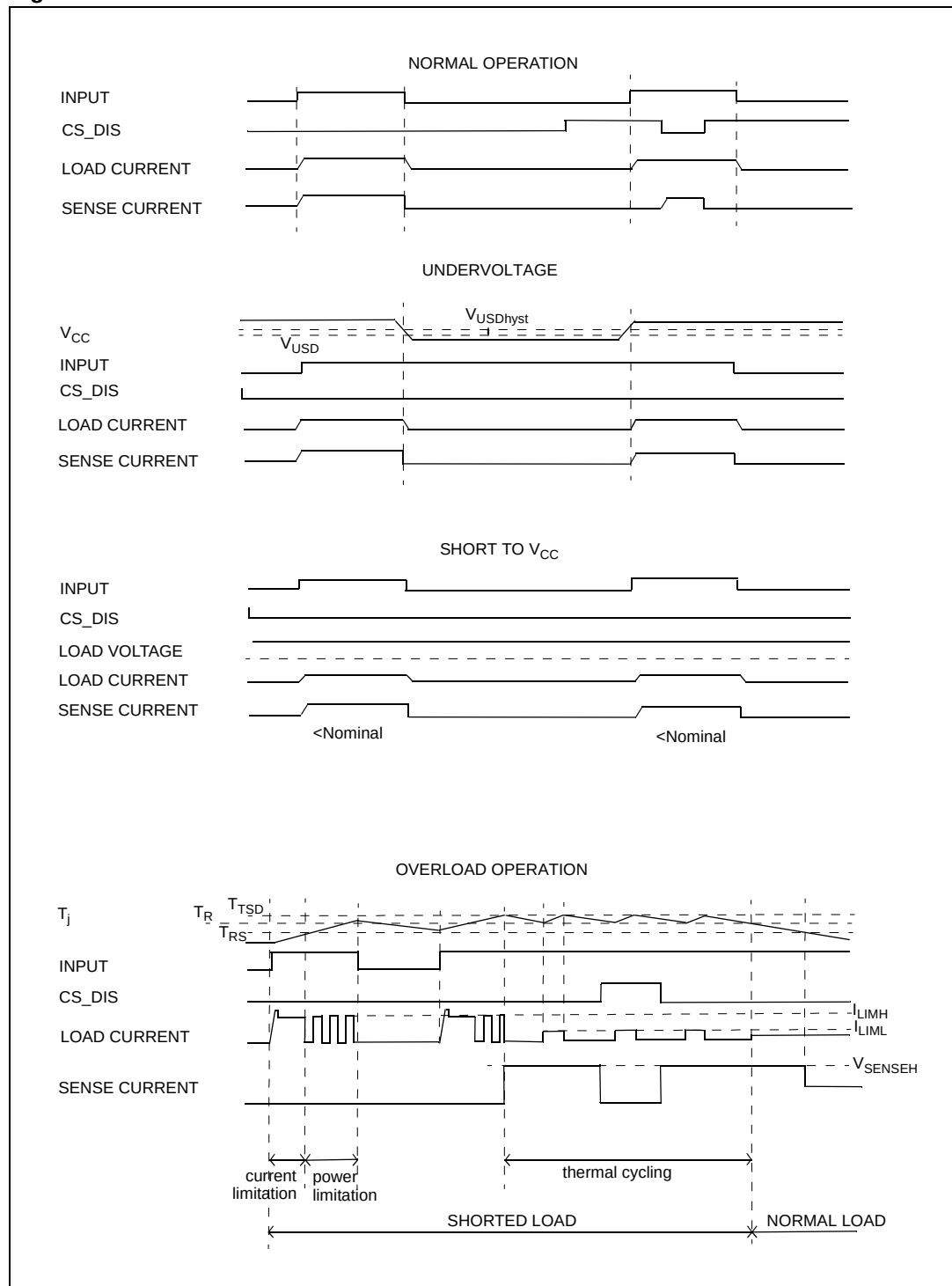
Calculation example:

For $V_{CCpeak} = -100V$ and $I_{latchup} \geq 20mA$; $V_{OH\mu C} \geq 4.5V$

$$5k\Omega \leq R_{prot} \leq 180k\Omega.$$

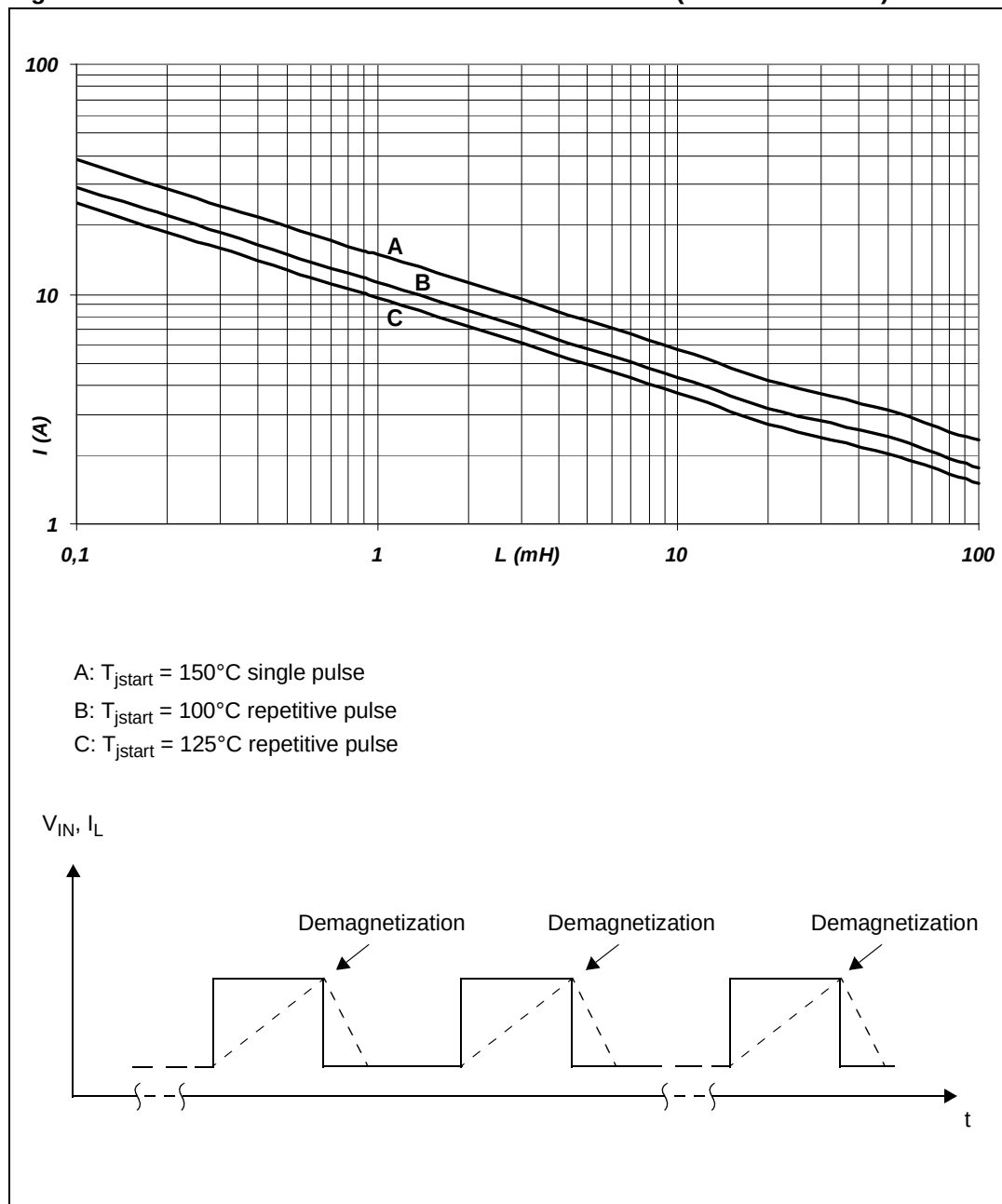
Recommended values: $R_{prot} = 10k\Omega$, $C_{EXT} = 10nF$.

Figure 26. Waveforms



3.4 Maximum demagnetization energy ($V_{CC} = 13.5V$)

Figure 27. Maximum turn-off current versus inductance (for each channel)



Note:

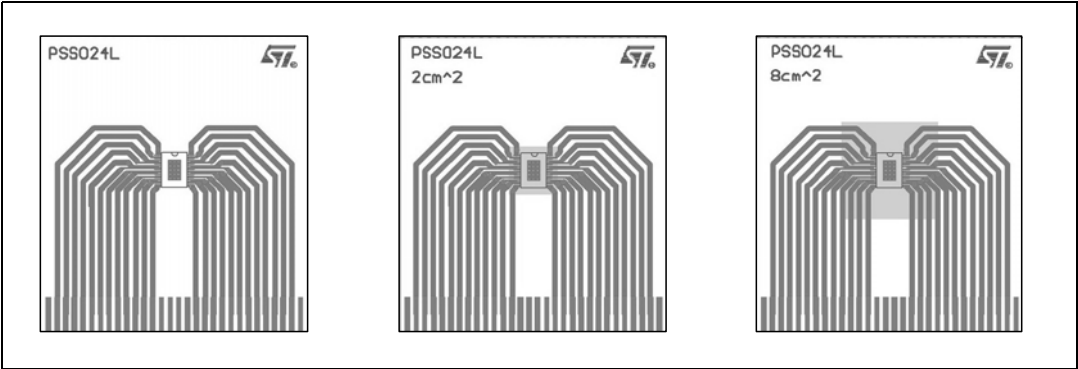
Values are generated with $R_L = 0\Omega$.

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PC board thermal data

4.1 PowerSSO-24™ thermal data

Figure 28. PowerSSO-24™ PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70μm (front and back side), Copper areas: from minimum pad lay-out to 8cm²).

Figure 29. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

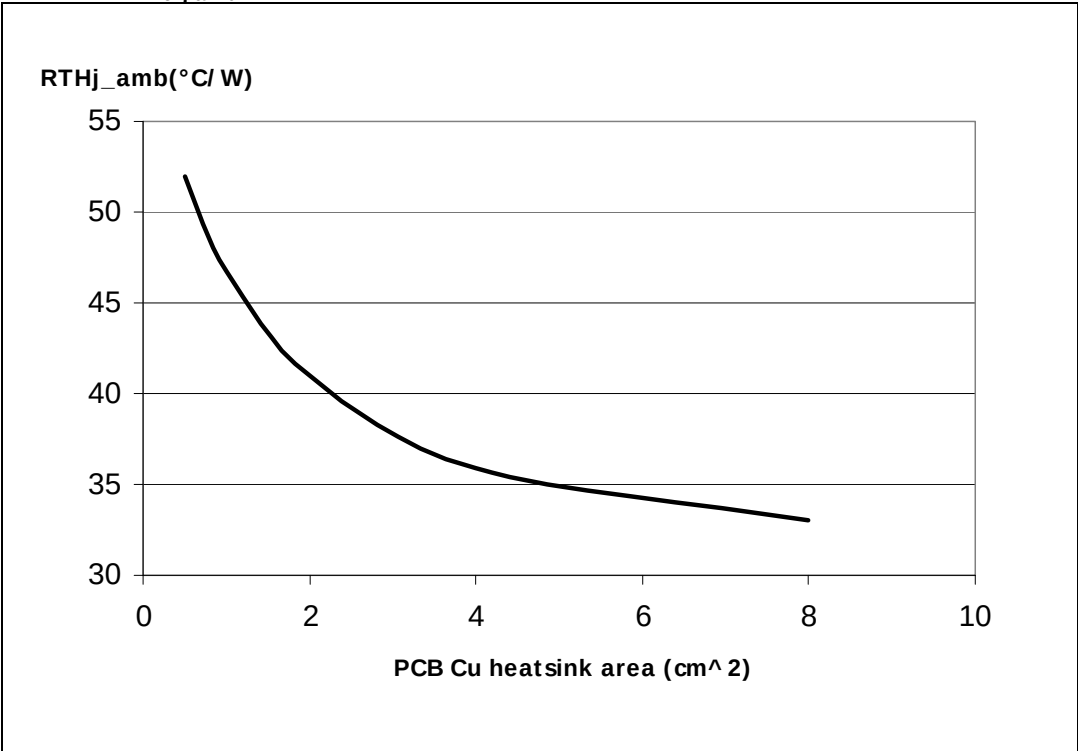


Figure 30. PowerSSO-24™ thermal impedance junction ambient single pulse (one channel on)

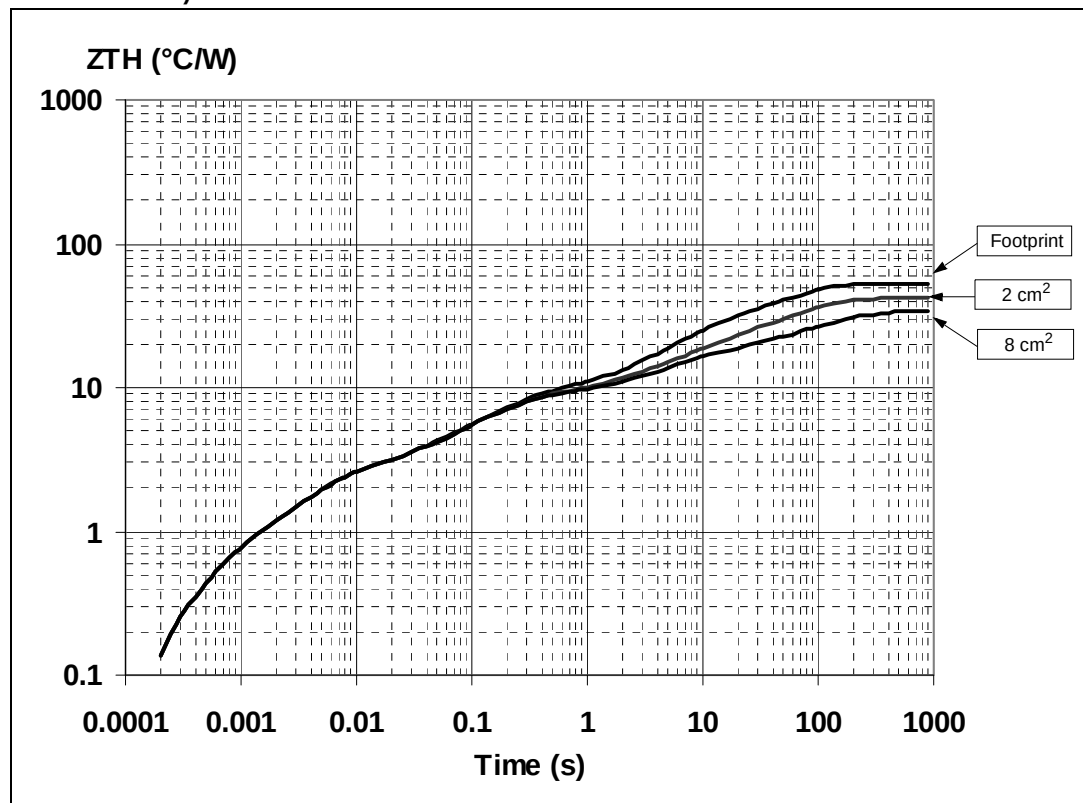
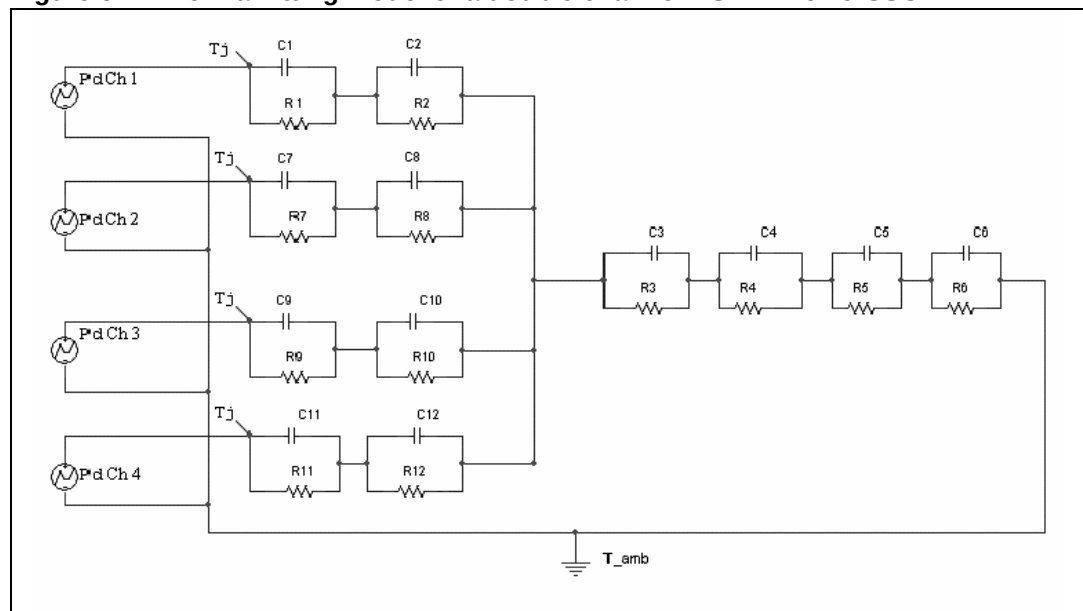


Figure 31. Thermal fitting model of a double channel HSD in PowerSSO-24™ (a)



- a. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Table 15. Thermal parameters

Area/island (cm ²)	Footprint	2	8
R1=R7=R9=R11 (°C/W)	0.28		
R2=R8=R10=R12 (°C/W)	0.9		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1=C7=C9=C11 (W.s/°C)	0.001		
C2=C8=C10=C12 (W.s/°C)	0.003		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

5 Package and packing information

5.1 ECOPACK[®] packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com.

ECOPACK[®] is an ST trademark.

5.2 PowerSSO-24[™] mechanical data

Figure 32. PowerSSO-24[™] package dimensions

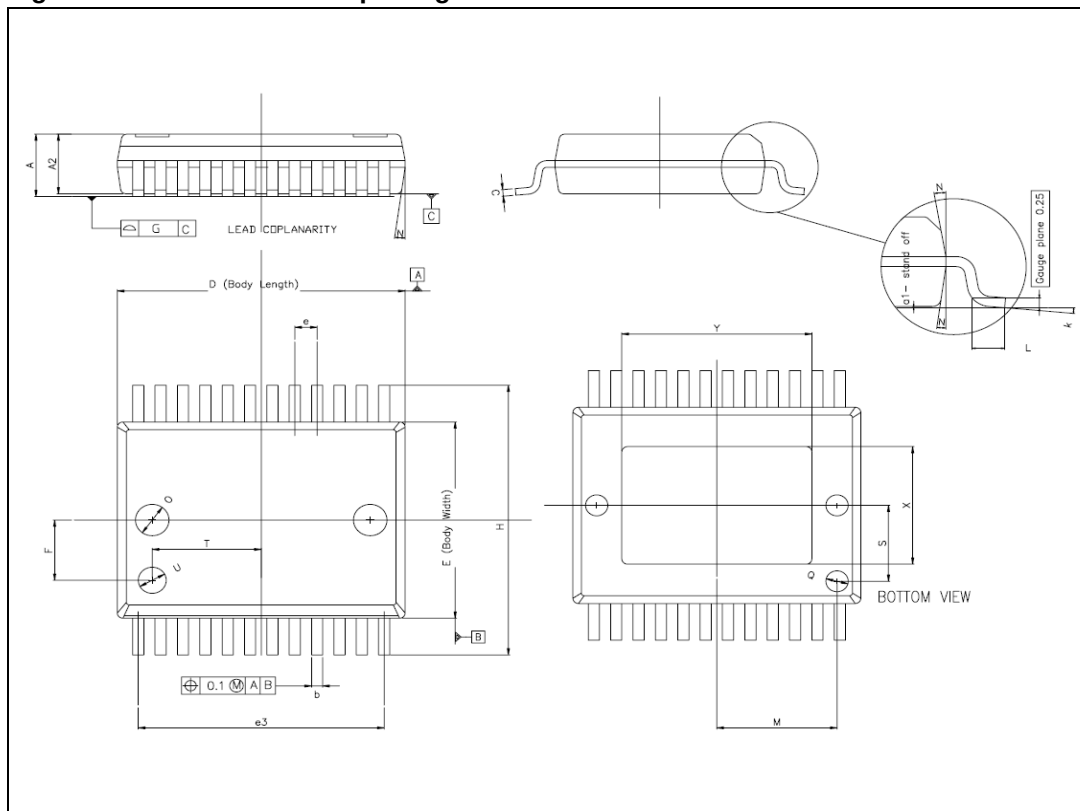


Table 16. PowerSSO-24™ mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A			2.45
A2	2.15		2.35
a1	0		0.1
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
F		2.3	
G			0.1
H	10.1		10.5
h			0.4
k	0°		8°
L	0.55		0.85
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1.0	
N			10°
X	4.1		4.7
Y	6.5		7.1

5.3 Packing information

Figure 33. PowerSSO-24™ tube shipment (no suffix)

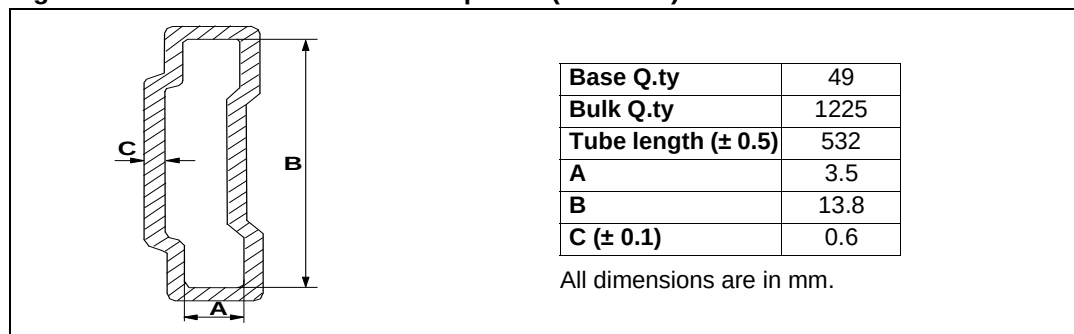
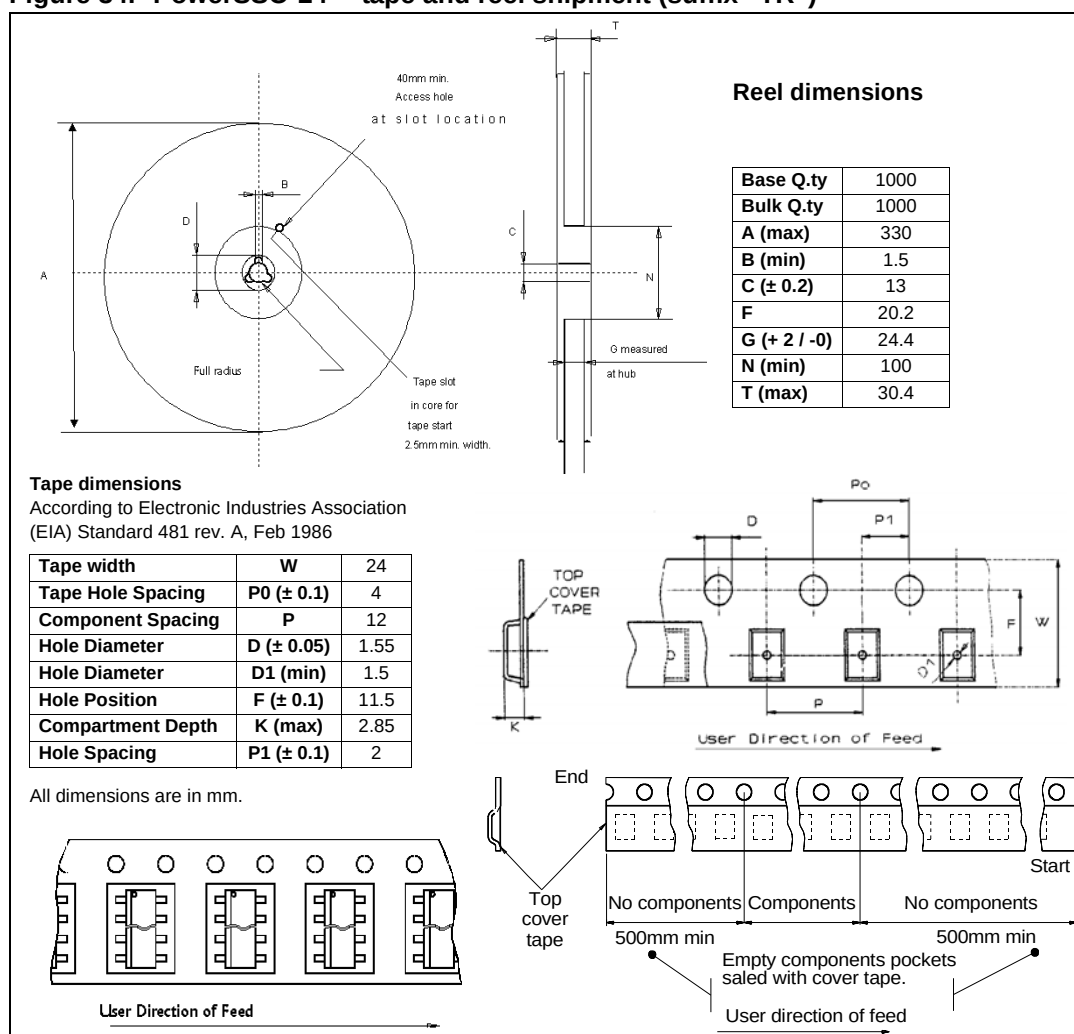


Figure 34. PowerSSO-24™ tape and reel shipment (suffix “TR”)



6 Revision history

Table 17. Document revision history

Date	Revision	Changes
17-Nov-2006	1	Initial release.
18-Dec-2007	2	Table 4: Absolute maximum ratings: E_{MAX} max value changed from 82 to 140 mJ. Updated Table 8: Current Sense (8V<V_{CC}<16V): – added dK_0/K_0 parameter – added K_1 parameter – added dK_1/K_1 parameter – added dK_2/K_2 parameter – added dK_3/K_3 parameter – added $\Delta t_{DSENSE2H}$ parameter – added I_{OL} parameter Added Figure 5: Delay response time between rising edge of output current and rising edge of Current Sense (CS enabled). Added Figure 7: I_{OUT}/I_{SENSE} VS I_{OUT} Added Figure 8: Maximum current sense ratio drift vs load current. Added Section 2.4: Electrical characteristics curves. Added Section 3.4: Maximum demagnetization energy (VCC = 13.5V). Figure 31: Thermal fitting model of a double channel HSD in PowerSSO-24™: added note. Added ECOPACK® packages information. Update Section 5.2: PowerSSO-24™ mechanical data.
12-Feb-2008	3	Corrected typing error in Table 8: Current Sense (8V<V_{CC}<16V) : changed I_{OL} test condition from $V_{IN} = 0V$ to $V_{IN} = 5V$.
10-Apr-2008	4	Corrected Figure 27: Maximum turn-off current versus inductance (for each channel) .
19-Jun-2009	5	Table 16: PowerSSO-24™ mechanical data: – Deleted A (min) value – Changed A (max) value from 2.47 to 2.45 – Changed A2 (max) value from 2.40 to 2.35 – Changed a1 (max) value from 0.075 to 0.1 – Added F row – Updated k row
22-Jul-2009	6	Updated Figure 32: PowerSSO-24™ package dimensions. Updated Table 16: PowerSSO-24™ mechanical data: – Deleted G1 row – Added O, Q, S, T and U rows
20-Sep-2013	7	Updated disclaimer.

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