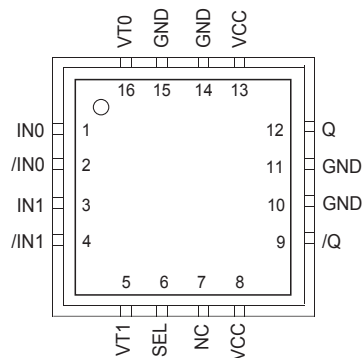


PACKAGE/ORDERING INFORMATION



16-Pin QFN

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58018UMG	QFN-16	Industrial	018U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY58018UMGTR ⁽²⁾	QFN-16	Industrial	018U with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC electricals only.
2. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1, 2 3, 4	IN0, /IN0 IN1, /IN1	Differential Input: These input pairs are the differential signal inputs to the device. They accept differential AC- or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a V_T pin through 50 Ω . Note that these inputs will default to an indeterminate state if left open. Please refer to the "Input Interface Applications" section for more details.
16, 5	VT0, VT1	Input Termination Center-Tap: Each side of the differential input pair terminates to a V_T pin. The V_{T0} and V_{T1} pins provide a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details.
6	SEL	This single-ended TTL/CMOS compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25k Ω pull-up resistor and will default to a logic HIGH state if left open.
7	NC	No connect.
8, 13	VCC	Positive Power Supply: Bypass with 0.1 μF^{TMM} 0.01 μF low ESR capacitors. 0.01 μF capacitor should be as close to V_{CC} pin as possible.
12, 9	Q, /Q	Differential Outputs: This 100k compatible LVPECL output pair is the output of the device. Normally terminate with 50 Ω to $V_{CC} - 2\text{V}$. See "Output Interface Applications" section. It is a logic function of the IN0, IN1, and SEL inputs. Please refer to the "Truth Table" for details.
10, 11, 14, 15	GND, Exposed Pad	Ground. Ground pins and exposed pad must be connected to the same ground plane.

TRUTH TABLE

SEL	Output
0	CH0 Input Selected
1	CH1 Input Selected

Absolute Maximum Ratings⁽¹⁾

Power Supply Voltage (V_{CC})	–0.5V to +4.0V
Input Voltage (V_{IN})	–0.5V to V_{CC}
LVPECL Output Current (I_{OUT})	
Continuous	50mA
Surge	100mA
Termination Current ⁽³⁾	
Source or Sink Current on V_T pin	±100mA
Input Current	
Source or Sink Current on IN, /IN pin	±50mA
Lead Temperature (soldering, 20 sec.)	260°C
Storage Temperature Range (T_S)	–65°C to +150°C

Operating Ratings⁽²⁾

Power Supply Voltage (V_{CC})	+2.375V to +2.625V
	+3.0V to +3.6V
Ambient Temperature Range (T_A)	–40°C to +85°C
Package Thermal Resistance ⁽⁴⁾	
QFN (θ_{JA})	
Still-Air	60°C/W
QFN (ψ_{JB})	
Junction-to-Board	38°C/W

DC ELECTRICAL CHARACTERISTICS⁽⁵⁾

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	$V_{CC} = 2.5V$ $V_{CC} = 3.3V$	2.375 3.0	2.5 3.3	2.625 3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		50	65	mA
R_{DIFF_IN}	Differential Input Resistance (IN0-to-/IN0, IN1-to-/IN1)		80	100	120	Ω
R_{IN}	Input Resistance (IN0-to- V_{T0} , /IN0-to- V_{T0} , IN1-to- V_{T1} , /IN1-to- V_{T1})		40	50	60	Ω
V_{IH}	Input HIGH Voltage (IN0, /IN0, IN1, /IN1)	Note 6	$V_{CC} - 1.6$		V_{CC}	V
V_{IL}	Input LOW Voltage (IN0, /IN0, IN1, /IN1)		0		$V_{IH} - 0.1$	V
V_{IN}	Input Voltage Swing (IN0, /IN0, IN1, /IN1)	See Figure 1a	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing IN0, /IN0 , IN1, /IN1	See Figure 1b	0.2			V
$V_{T\ IN}$	IN to V_T (IN0, /IN0, IN1, /IN1)				1.28	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB. ψ_{JB} uses 4-layer θ_{JA} in still-air number, unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IH} (min) not lower than 1.2V.

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS⁽⁷⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$; $R_L = 50\Omega$ to $V_{CC} - 2V$, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage Q, /Q		$V_{CC} - 1.145$		$V_{CC} - 0.895$	V
V_{OL}	Output LOW Voltage Q, /Q		$V_{CC} - 1.945$		$V_{CC} - 1.695$	V
V_{OUT}	Output Differential Swing Q, /Q	See Figure 1a	550	800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing Q, /Q	See Figure 1b	1100	1600		mV

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS⁽⁷⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current				40	μA
I_{IL}	Input LOW Current		-300			μA

Note:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS⁽⁸⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $85^\circ C$, $R_L = 50\Omega$ to $V_{CC} - 2V$, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	5			Gbps
		$V_{OUT} \geq 400mV$ Clock		4		GHz
t_{pd}	Differential Propagation Delay (IN0 or IN1-to-Q) (SEL-to-Q)		110 50	190 180	240 350	ps ps
				75		fs/°C
$t_{pd} \text{ Tempco}$	Differential Propagation Delay Temperature Coefficient					
t_{SKEW}	Input-to-Input Skew	Note 9		4	15	ps
	Part-to-Part Skew	Note 10			100	ps
t_{JITTER}	Data Random Jitter	Note 11			1	ps _{RMS}
	Deterministic Jitter	Note 12			10	ps _{PP}
	Clock Cycle-to-Cycle Jitter	Note 13			1	ps _{RMS}
	Total Jitter	Note 14			10	ps _{PP}
	Crosstalk-Induced Jitter	Note 15			0.7	ps _{RMS}
t_r, t_f	Output Rise/Fall Time	20% to 80%, at full swing	35	75	110	ps

Notes:

8. High frequency AC parameters are guaranteed by design and characterization.
9. Input-to-input skew is the difference in time from and input-to-output in comparison to any other input-to-output. In addition, the input-to-input skew does not include the output skew.
10. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
11. RJ is measured with a K28.7 comma detect character pattern, measured at 10.7Gbps and 2.5Gbps/3.2Gbps.
12. DJ is measured at 2.5Gbps/3.2Gbps, with both K28.5 and $2^{23} - 1$ PRBS pattern.
13. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
14. Total jitter definition: with an ideal clock input of frequency - f_{MAX} no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
15. Crosstalk is measured at the output while applying two similar frequencies that are asynchronous with respect to each other at the inputs.

SINGLE-ENDED AND DIFFERENTIAL SWINGS

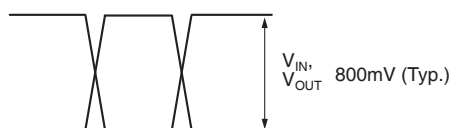


Figure 1a. Single-Ended Voltage Swing

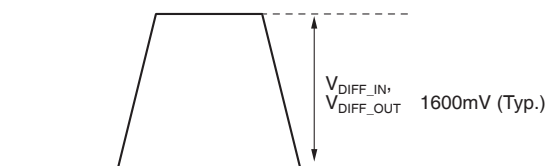
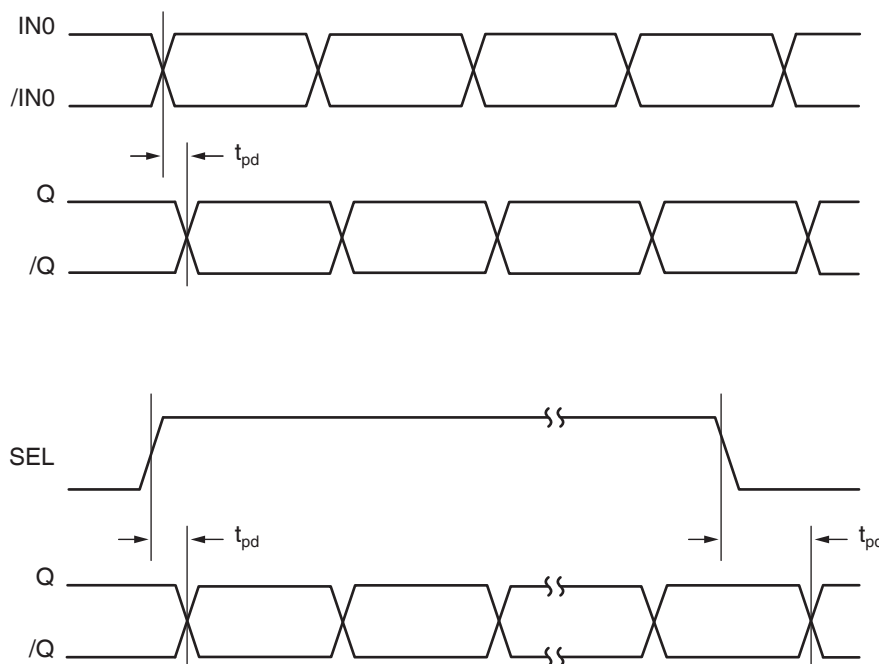


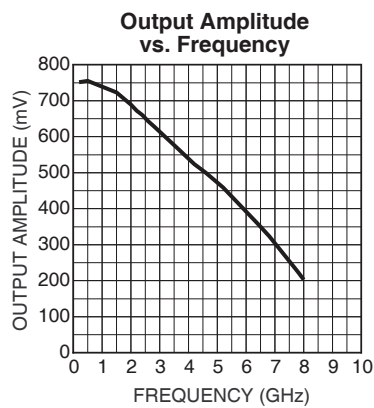
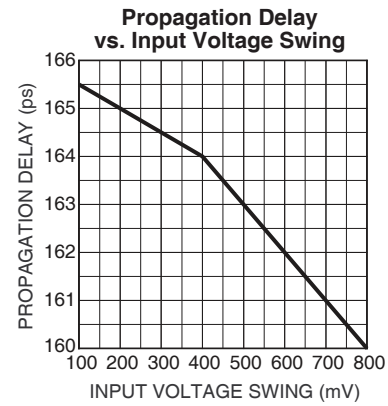
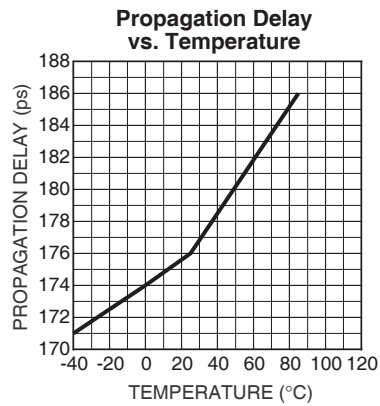
Figure 1b. Differential Voltage Swing

TIMING DIAGRAMS



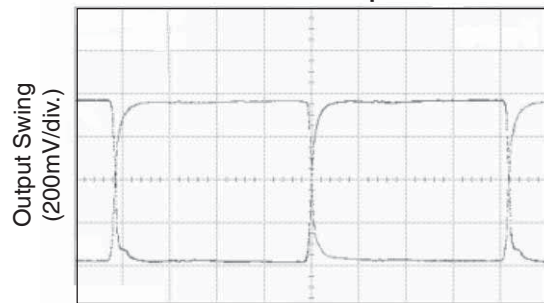
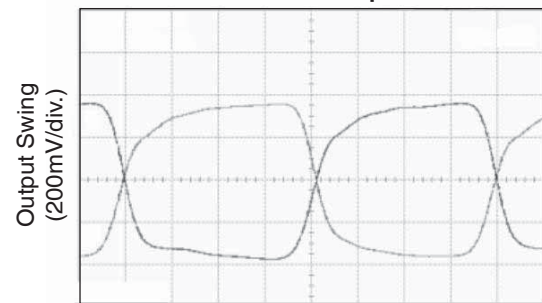
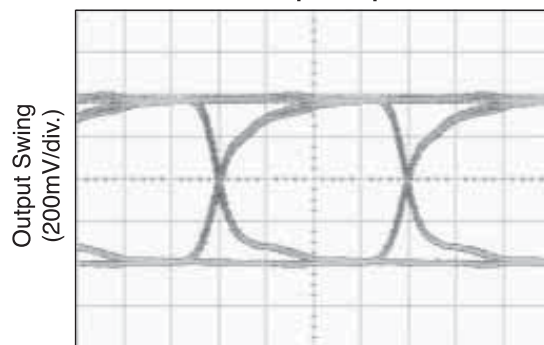
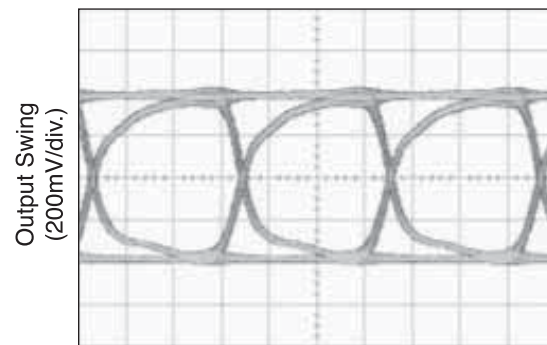
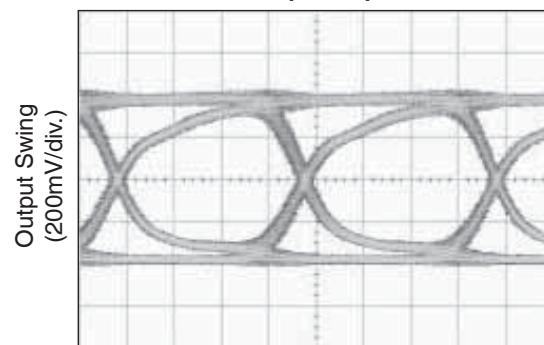
TYPICAL OPERATING CHARACTERISTICS

$V_{CC} = 3.3V$, $V_{IN} = 100mV$, $T_A = 25^\circ C$, unless otherwise stated.



TYPICAL OPERATING CHARACTERISTICS

$V_{CC} = 3.3V$, $V_{IN} = 100mV$, $T_A = 25^\circ C$, unless otherwise stated.

200MHz Output**1.25GHz Output****2.5Gbps Output****3.2Gbps Output****5Gbps Output**

INPUT AND OUTPUT STAGES

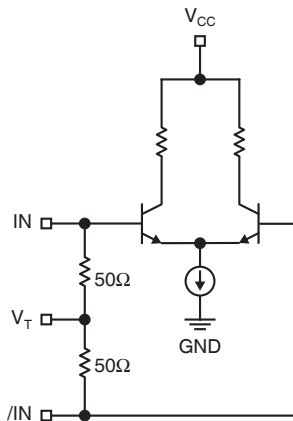


Figure 2a. Simplified Differential Input Stage

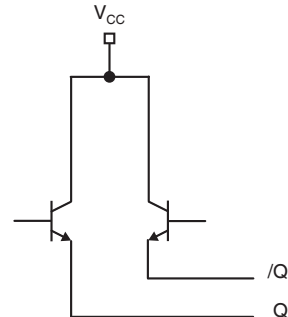


Figure 2b. Simplified LVPECL Output Stage

INPUT INTERFACE APPLICATIONS

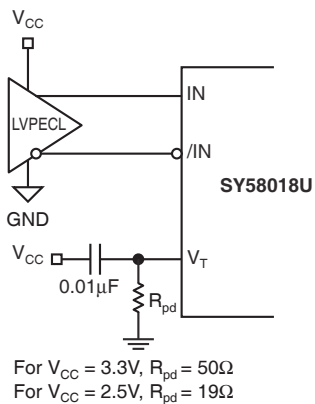
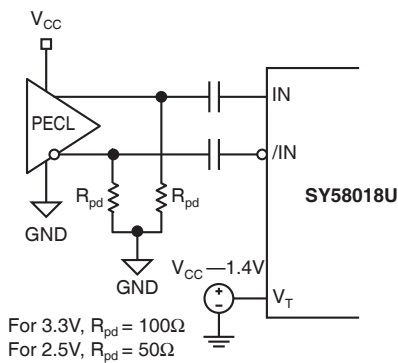
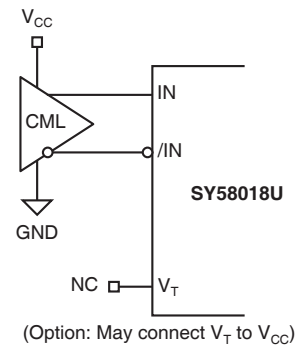
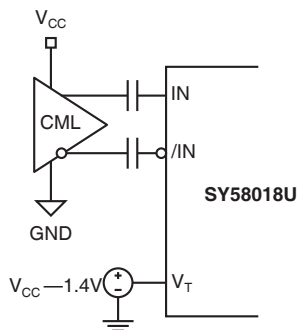
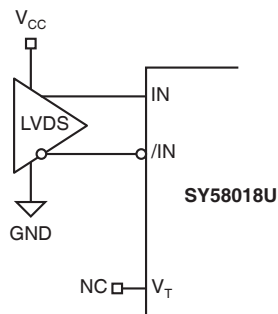
Figure 3a. DC-Coupled
LVPECL InterfaceFigure 3b. AC-Coupled
LVPECL InterfaceFigure 3c. DC-Coupled
CML InterfaceFigure 3d. AC-Coupled
CML Interface

Figure 3e. LVDS Interface

OUTPUT INTERFACE APPLICATIONS

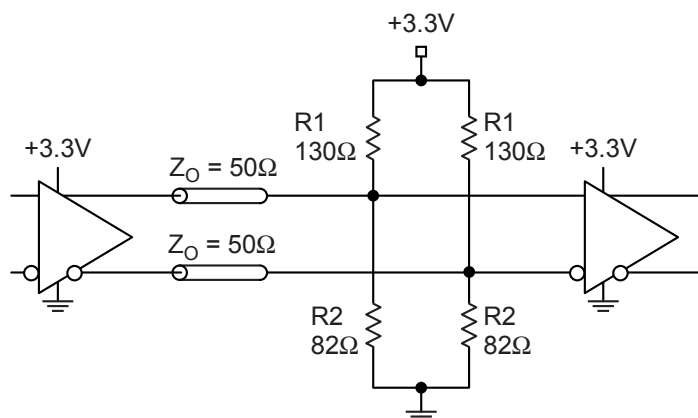


Figure 4a. Parallel Thevenin-Equivalent Termination

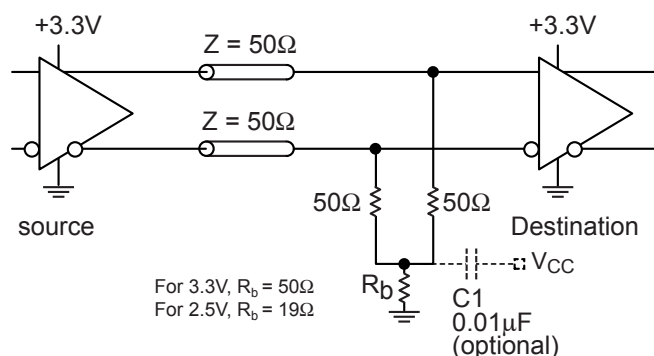


Figure 4b. Three-Resistor "Y" Termination

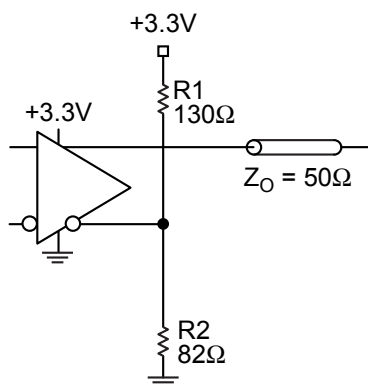
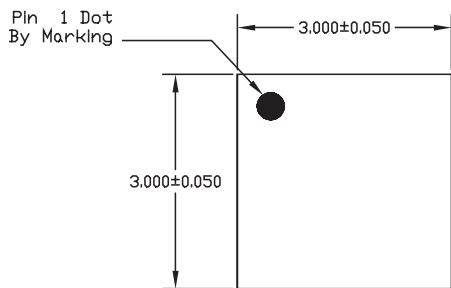
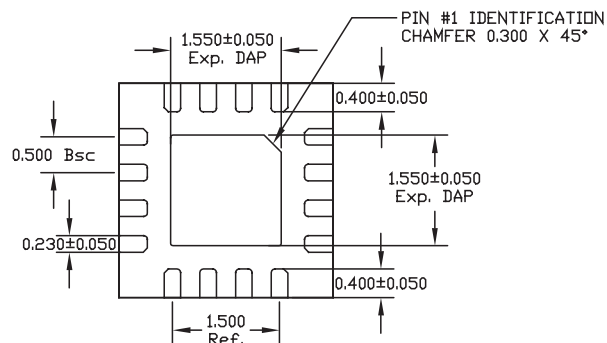
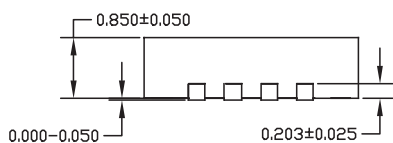


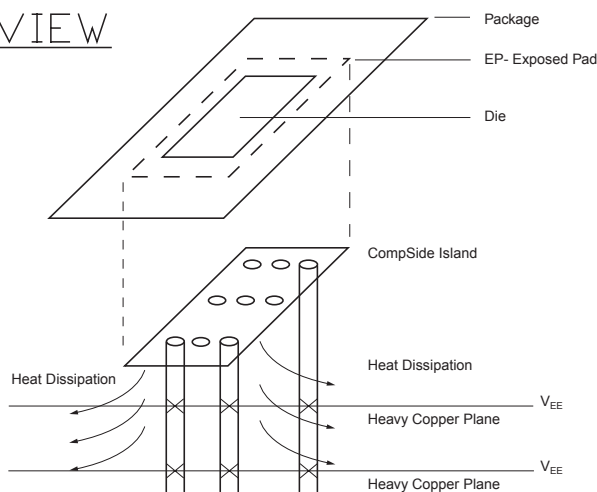
Figure 4c. Terminating Unused I/O

RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY58016L	3.3V 10Gbps Differential CML Line Driver/Receiver with Internal I/O Termination	http://www.micrel.com/product-info/products/sy58016l.shtml
SY58017U	Ultra Precision Differential CML 2:1 Mux with Internal I/O Termination	http://www.micrel.com/product-info/products/sy58017u.shtml
SY58019U	Ultra Precision Differential 400mV LVPECL 2:1 MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58019u.shtml
SY58025U	10.7Gbps Dual 2:1 CML MUX with Internal I/O Termination	http://www.micrel.com/product-info/products/sy58025u.shtml
SY58026U	5Gbps Dual 2:1 MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58026u.shtml
SY58027U	10.7Gbps Dual 2:1 400mV LVPECL MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58027u.shtml
SY58051U	10.7Gbps AnyGate® with Internal Input and Output Termination	http://www.micrel.com/product-info/products/sy58051u.shtml
SY58052U	10Gbps Clock/Data Retimer with 50Ω Input Termination	http://www.micrel.com/product-info/products/sy58052u.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

16-PIN QFN (QFN-16)TOP VIEWBOTTOM VIEWSIDE VIEW**NOTE:**

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 16-Pin QFN Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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