Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	unit
Operating supply voltage 1	$V_{CC}1$	With signals applied (Tc=105°C)	10 to 38	V
Operating supply voltage 2	$V_{CC}2$	With signals applied (Tc=90°C)	10 to 42	V
Operating supply voltage 2	V_{DD}	With signals applied	5±5%	V
Input voltage	V_{IN}		0 to V_{DD}	V
Output current 1	I_O1	V_{DD}=5.0V, DC current, Tc=80°C	6.1	A
Output current 2	I_O2	V_{DD}=5.0V, DC current, Tc=105°C	5	A
Brake current	I_OB	V_{DD}=5.0V, square wave current, operating time 2ms, Low side brake, Tc=105°C	12	A

Refer to the graph for each conduction-period tolerance range for the output current and brake current.

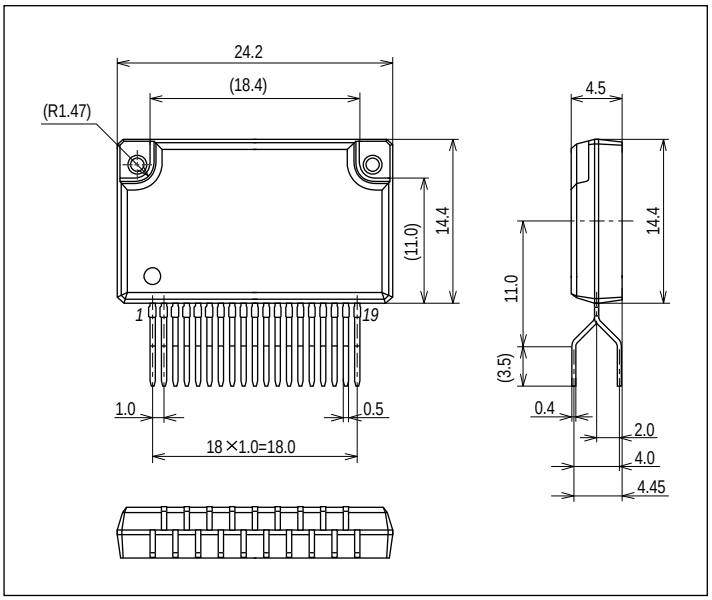
Electrical Characteristics at Tc = 25°C, V_{CC} = 24V, V_{DD} = 5.0V

Parameter	Symbol	Conditions	min	typ	max	unit
V_{DD} supply current	I_{CCO}	Forward or reverse operation		6	9	mA
FET diode forward voltage	Vdf	If=1A (R_L=23Ω)		0.75	1.4	V
Output saturation voltage 1	Vsat1	R_L=23Ω, F1, F2		65	100	mV
Output saturation voltage 2	Vsat2	R_L=23Ω, F3, F4		50	85	mV
Output leak current	I_{OL}	F1, F2, F3, and F4 OFF operation			50	μA
Input high voltage	V_{IH}	IN1, IN2, ENABLE pins	2.5			V
Input low voltage	V_{IL}	IN1, IN2, ENABLE pins			0.8	V
High-level input current	$I_{IL}H$	IN1, IN2, ENABLE pins, V_{IH}=5V		50	75	μA
Low-Level Input current	$I_{IL}L$	IN1, IN2, ENABLE pins, V_{IL}=GND			10	μA
Overcurrent detection voltage	VOC	Between pins Vref1 and S.P		0.48		V
Internal PWM frequency	fc		32	46	62	kHz
Overheat detection temperature	TSD	Design guarantee		144		°C

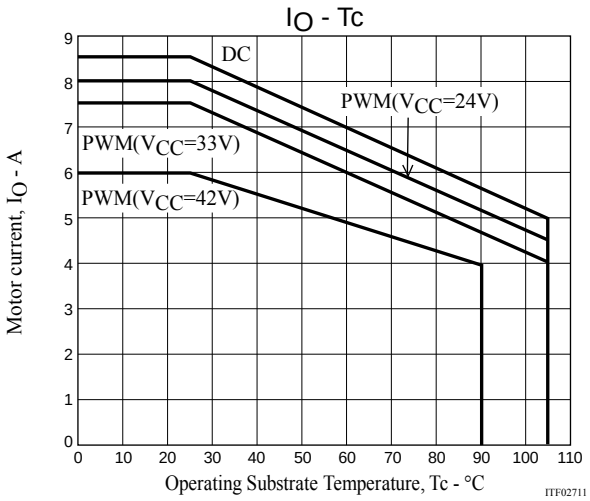
Note: A fixed-voltage power supply must be used.

Package Dimensions

unit:mm (typ)



Derating Curve of Motor Current, I_O, vs. STK681-332-E Operating Board Temperature, Tc

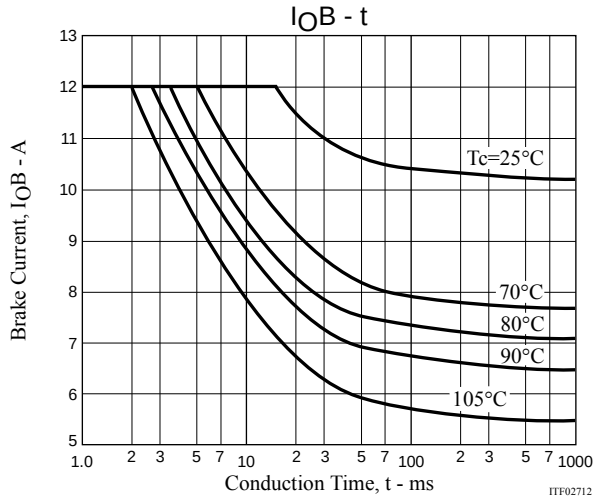


(The maximum PWM frequency is 50kHz.)

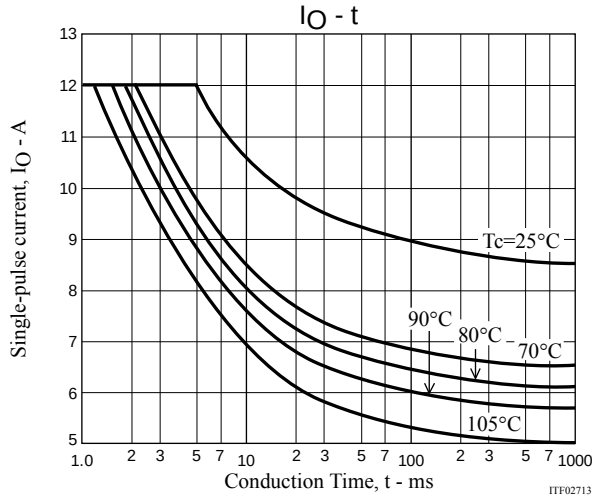
The PWM frequencies in the above graph indicate the ENABLE signal.
The same PWM I_O derating curves as those shown above will be obtained when the internal PWM frequency of the STK681-332-E is used.
Increasing the V_{CC} supply voltage narrows the I_O derating curve range, so I_O should be set in reference to the above graph.

The above operating substrate temperature, Tc, is measured immediately when the motor is started.
Since Tc fluctuates due to the ambient temperature, Ta, the motor current value, and continuous or intermittent operations of the motor current, always confirm this values using an actual set.
The Tc temperature should be checked in the center of the metal surface of the product package.

STK681-332-E Allowable Brake Current Range (Low side: F3, F4=ON)

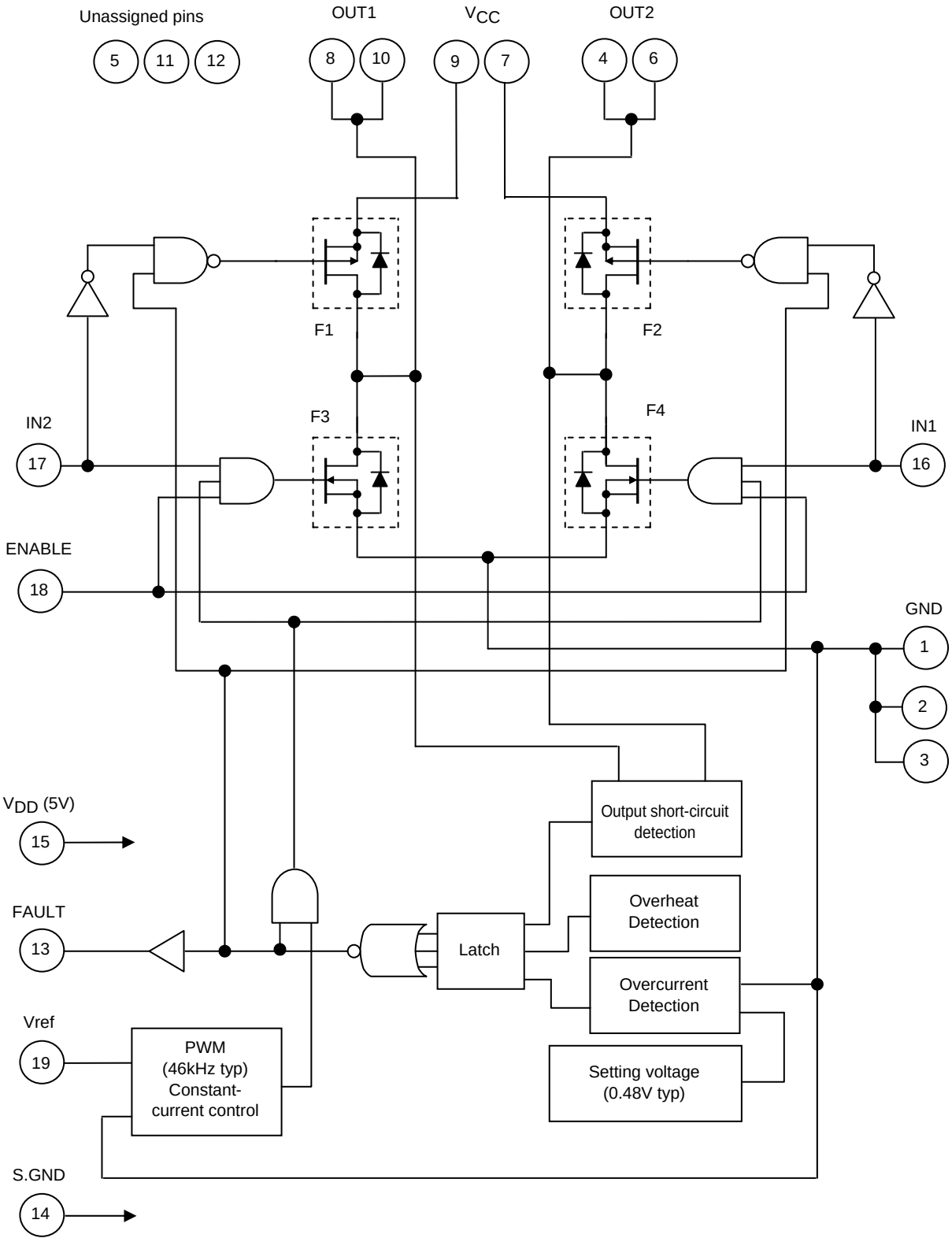


STK681-332-E Allowable Brake Current Range (High side: F1, F2=ON)

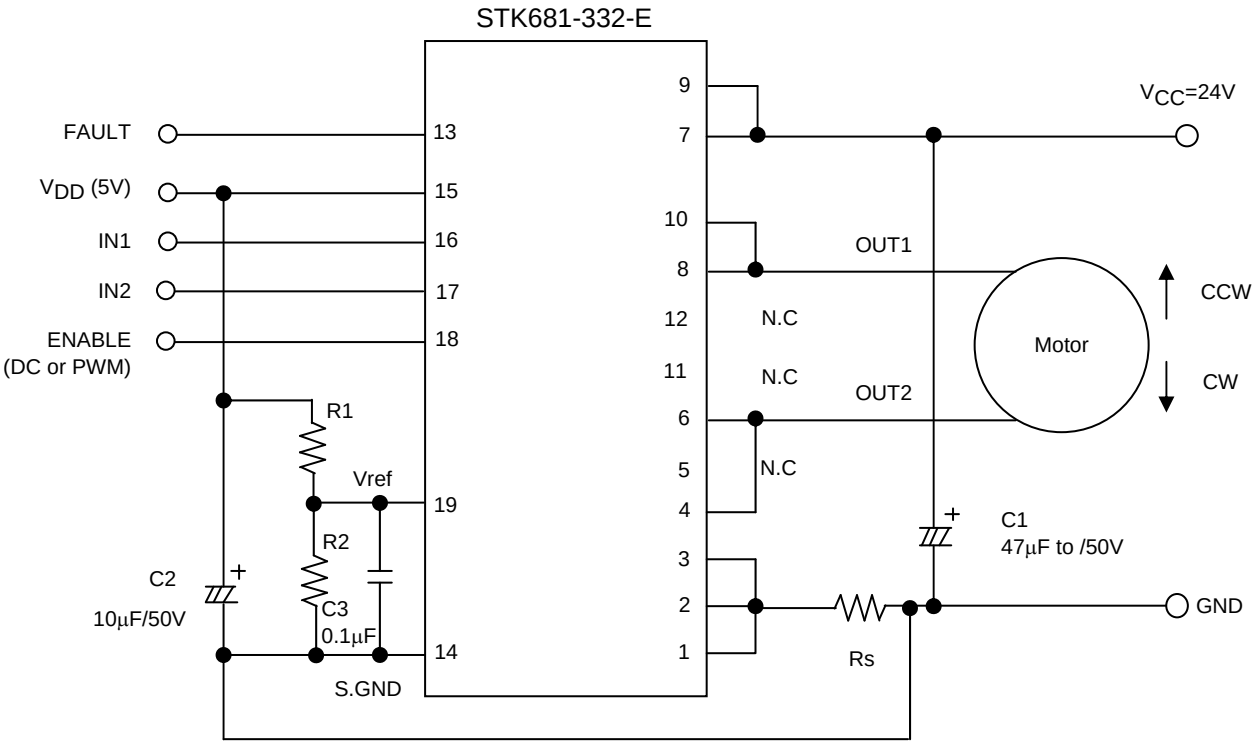


The output current specifications are the same as the high side brake current specifications.

Internal Block Diagram



Sample Application Circuit



Motor Drive Conditions (H: High-level input; L: Low-Level Input)

	IN1	IN2	ENABLE	Remarks
Stop	H	L	L	Turns the power supply OFF. ENABLE must be set Low when V_{DD} is rising or falling.
	L	H	L	
	H	H	L	
Forward (CW)	H	L	H	No input signal is needed that turns off the upper- and lower-side drive devices when switching the rotational direction.
Reverse (CCW)	L	H	H	
Brake	L	L	L or H	GND side MOSFET ON
	H	H	H	V_{CC} side MOSFET ON

* Output control is enabled by applying an external PWM signal to the ENABLE pin.
The product can run at a minimum external PWM pulse width of 1μs. In the case when the high pulse width is less than 16μs, however, the IC may fail to detect a short-circuit condition when an output short-circuit occurs.
If V_{DD} is turned off in the condition with the ENABLE pin set to high during motor rotation or PWM operation, the FAULT signal is output when V_{DD} is falling, indicating error condition. For this reason, ENABLE must be set to low when V_{DD} is rising or falling.
When both IN1 and IN2 are set low, the MOSFET on the V_{CC} side is driven. To minimize the loss when stopped, set IN1 = IN2 = High and ENABLE = Low to turn off the gate signal to the V_{CC} side MOSFETs.

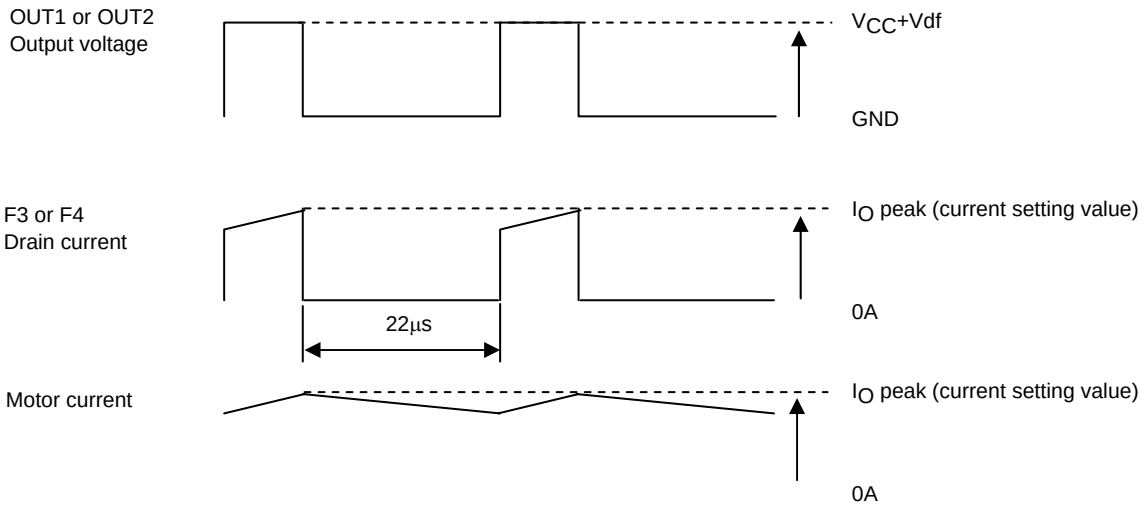
Setting the current limit using the Vref pin
Output current peak (Iop) = (Vref ÷ 4.9) ÷ Rs
"4.9" in the above formula indicates the portion of the Vref voltage that is divided using the circuit inside the control IC.
$Vref = (R2 \div (R1+R2)) \times V_{DD}$
Rs is the external current detection resistance value of the HIC, and Vref ≤ 2.0V must be satisfied so that overcurrent detection is not triggered.

Notes

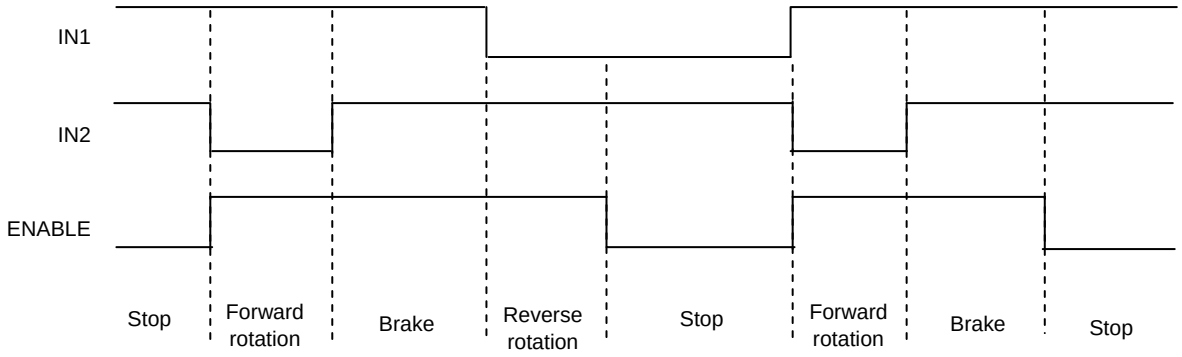
(1) Be sure to set the capacitance of the power supply bypass capacitor, C1, so that the ripple current of the capacitor, which varies as motor current increases, falls within the allowed range.

(2) Chopping operations based on F3 and F4 are used for current control. The timing given below is used for OUT1 or OUT2 voltage output and for F3 or F4 drain current.

(3) Do not connect the N.C pins (5, 11, 12 pin) shown in the internal block diagram or sample application circuit to a circuit pattern on the PCB.



(4) Sample Timing Diagram



(5) If the current detection resistor, Rs, connected to pin1, pin2, and pin3 is short-circuited, the overcurrent detection circuit does not operate. If the output pin is short-circuited directly to V_{CC} or connected directly to GND, an output short-circuit condition is detected and the output is latched in the off state. To restart the operation, turn on V_{DD} again.

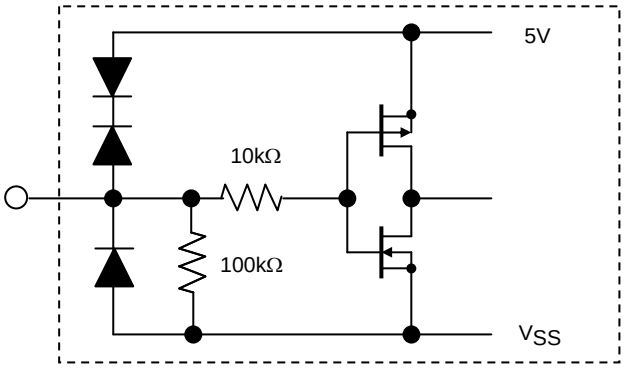
(6) Smoke Emission Precautions: There is a possibility of smoke emission if the hybrid IC is subjected to physical or electrical damage as the result of being used without compliance with the specifications.

I/O Functions of Each Pin

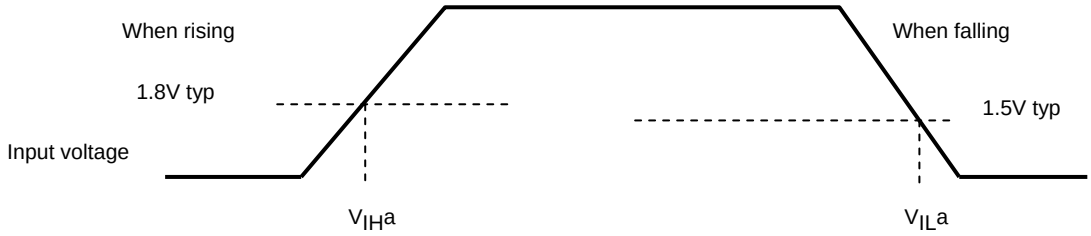
Pin Name	Pin No.	Function
IN1	16	Input pin for turning F2 and F4 ON and OFF At low level F2: ON and F4: OFF; at high level, F2: OFF and F4: ON
IN2	17	Input pin for turning F1 and F3 ON and OFF At low level F1: ON and F3: OFF; at high level, F1: OFF and F3: ON
ENABLE	18	Pin for turning F3 and F4 ON; At high level F31 and F42: ON ENABLE must be set Low when V_{DD} is rising and falling. ENABLE must be set High to drive the motor.
FAULT	13	Monitor pin used when either of the output short-circuit detector, overcurrent detector, or overheat detector is activated. When the detector is activated, this pin is set low and all of F1, F2, F3 and F4 in the final stage are latched off.
OUT1	8, 10	This pin connects to the motor and outputs source/sync current depending on conditions at IN1 and IN2.
OUT2	4, 6	This pin connects to the motor and outputs source/sync current depending on conditions at IN1 and IN2.
Vref	19	This pin limits the peak current when motor startup. The current setting voltage, Vref, is set to the value of 4.9 times the voltage drop of the external current detection resistor. The internal overcurrent detection level is 0.48V, so setting Vref < 2.0V is recommended.
GND	1, 2, 3	Power system ground
S.GND	14	Control system ground
V_{CC}	7, 9	Motor system supply voltage
V_{DD}	15	Control system supply voltage.

Technical Information

1.Configuration of each pins <Configuration of the IN1, IN2, and ENABLE input pins>
Input pins: 16, 17, 18 pin

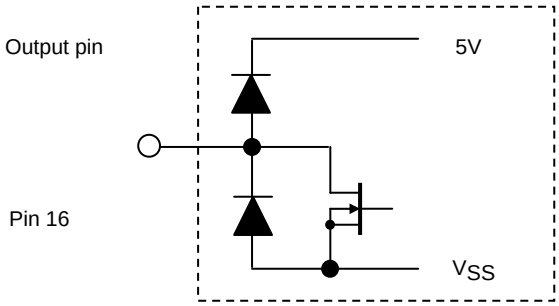


The input pins of this driver all use Schmitt input. Typical specifications at Tc=25°C are given below. Hysteresis voltage is 0.3V ($V_{IH}a$-$V_{IL}a$).

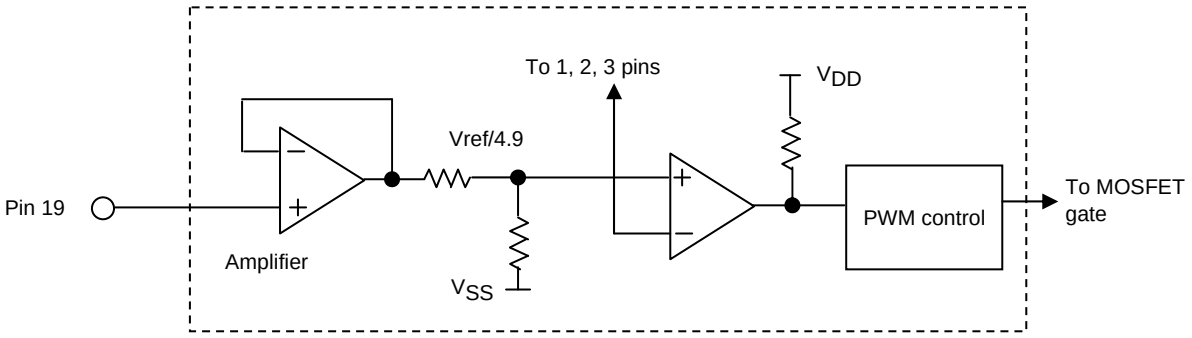


Input voltage specifications are as follows.
V_{IH}=2.5V min
V_{IL}=0.8V max

<Configuration of the FAULT input pin>



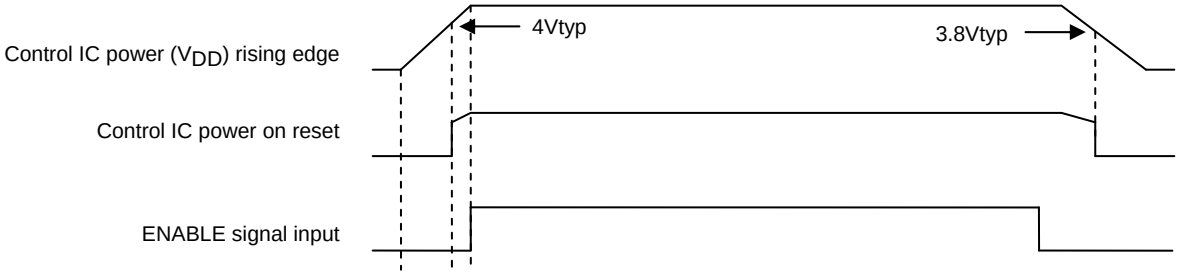
<Configuration of the Vref input pin>



[Reduced voltage detection]

(1) V_{DD}

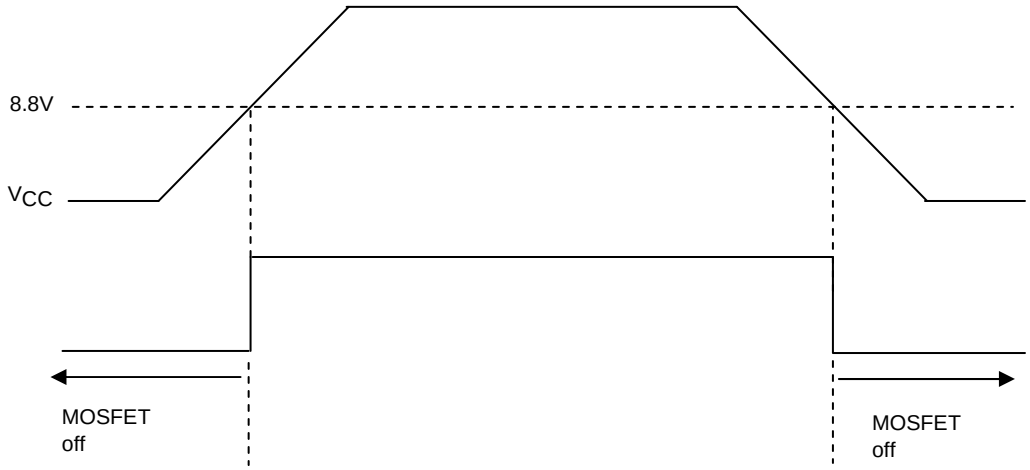
The internal control IC of the driver has a function that detects reduced voltage when V_{DD} is supplied. This reduced voltage threshold level is set to 4V (typ.), and the MOSFET gate voltage specification is 5V ±5%. So, a current flow through the output when V_{DD} is rising results in the power stress to the MOSFET due to insufficient gate voltage. To prevent this power stress, set ENABLE = Low when V_{DD} < 4.75V, which is outside the normal operating supply voltage range of the MOSFET.



V_{DD}, ENABLE Signals Input Timing

(2) V_{CC}

The internal control IC of the driver has a function that detects reduced voltage when V_{CC} is supplied, to prevent insufficient internal P-channel MOSFET gate voltage. The reduced voltage detection level is set to V_{CC} = 8.8V (typ.).



2. Output short-circuit detection, Overcurrent Detection and Overheat Detection

Each detection function operates using a latch system and turns output off. To restore output operation, turn the V_{DD} power supply off and then on again to apply a power-on reset.

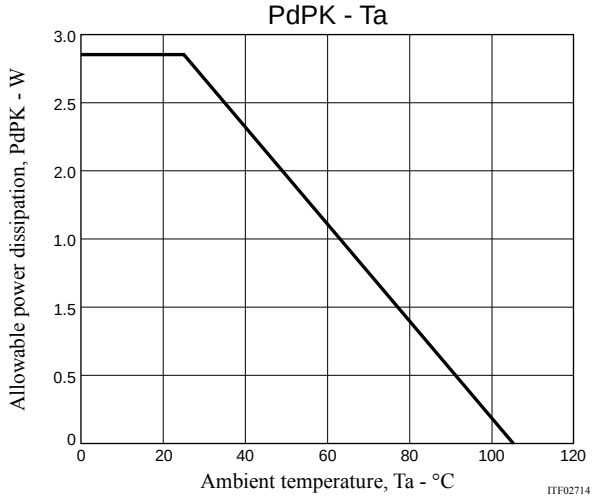
[Output Short-circuit Detection, Overcurrent Detection]
When the output pin is simply connected to the circuit GND or V_{CC}, or when the output load is short-circuited, the output short circuit detector must be activated and turn the output off.
Constant current PWM control can be performed by connecting a current detection resistor to pins 1, 2 and 3, and setting the Vref pin voltage to less than 2.0V. In addition, when this current detection resistor voltage exceeds 0.48V (typ.), the overcurrent detector is activated and shuts the output off.

[Overheat Detection]
Rather than directly detecting the temperature of the semiconductor device, overheat detection detects the temperature of the aluminum substrate (144°C typ).
Within the allowed operating range of I_O1 (6.1A) recommended in the specifications, if a heat sink attached for the purpose of reducing the operating substrate temperature, Tc, comes loose, the semiconductor can operate without breaking.
However, we cannot guarantee operations without breaking in the case of operation other than those recommended, such as operations at a current exceeding I_OH max (6.1A) that occurs before overcurrent detection is activated.

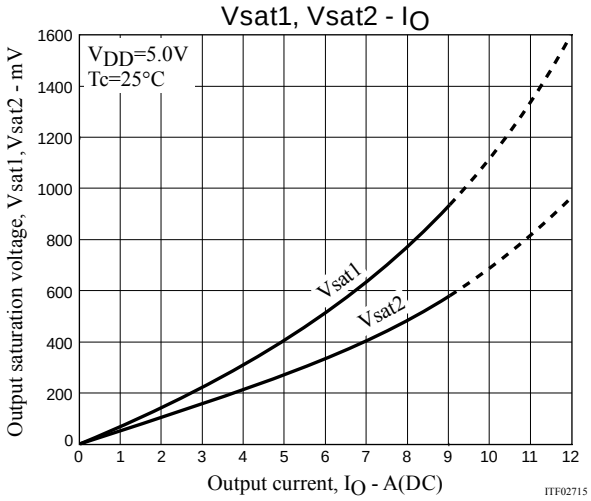
3. Mitigated Curve of Package Power Loss, PdPK, vs. Ambient Temperature, Ta

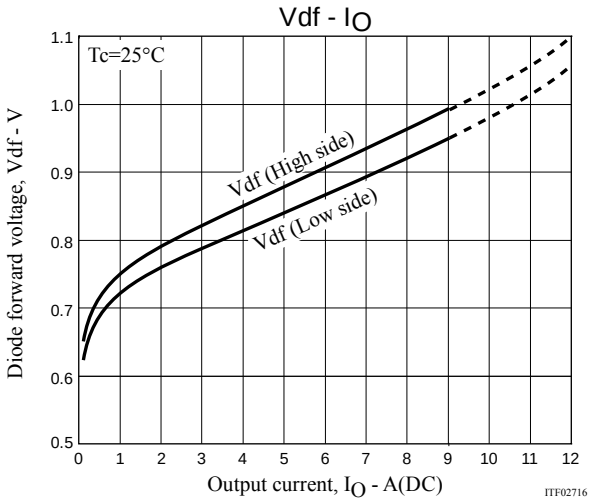
Package power loss, PdPK, refers to the average internal power loss, PdAV, allowable without a heat sink.
The figure below represents the allowable power loss, PdPK, vs. fluctuations in the ambient temperature, Ta.
Power loss of up to 2.8W is allowable at Ta=25°C, and of up to 1.5W at Ta=60°C.

Allowable power dissipation, PdPK (no heat sink) - Ambient temperature, Ta



4. Data





5. Other Notes on Use

In addition to the "Notes" indicated in the Sample Application Circuit, care should also be given to the following contents during use.

(1) Allowable operating range

Operation of this product assumes use within the allowable operating range. If a supply voltage or an input voltage outside the allowable operating range is applied, an overvoltage may damage the internal control IC or the MOSFET. If a voltage application mode that exceeds the allowable operating range is anticipated, connect a fuse or take other measures to cut off power supply to the product.

(2) Input pins

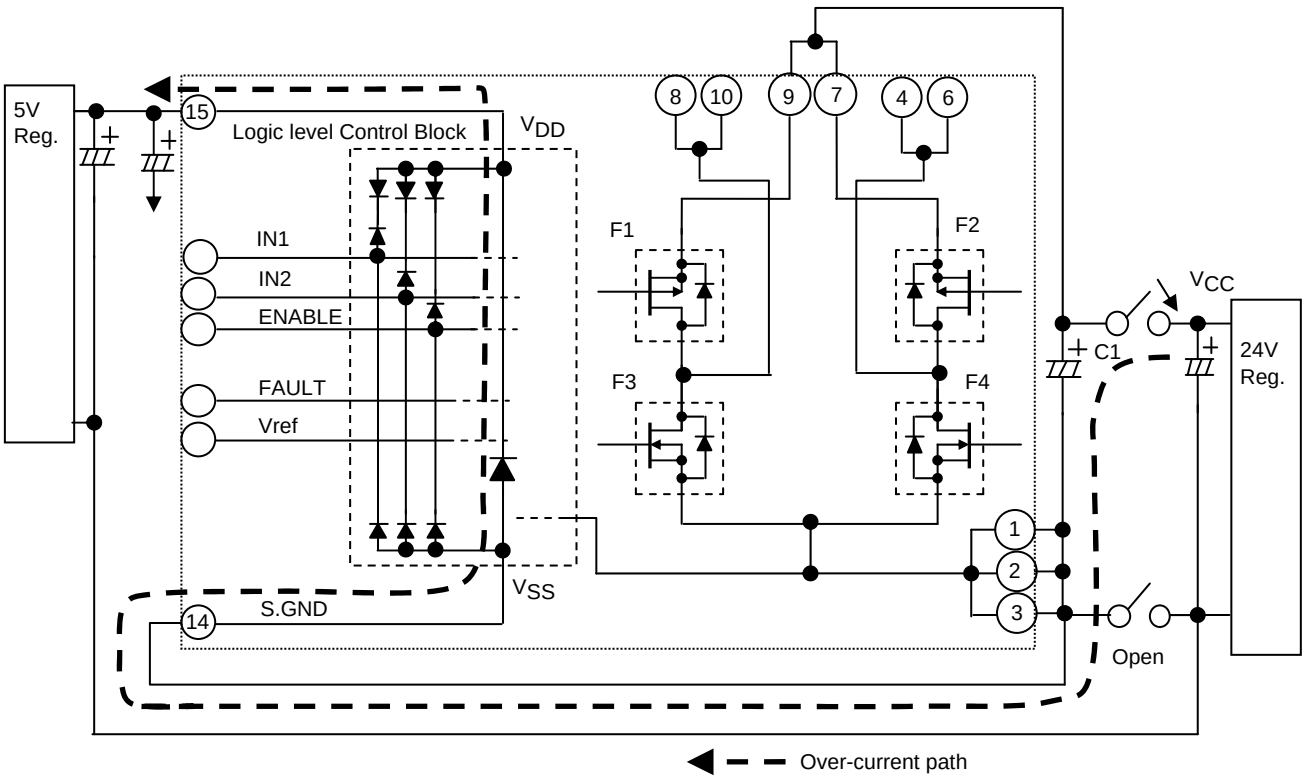
If the input pins are connected directly to the PC board connectors, electrostatic discharge or other overvoltage outside the specified range may be applied from the connectors and may damage the product. Current generated by this overvoltage can be suppressed to effectively prevent damage by inserting 100Ω to 1kΩ resistors in lines connected to the input pins.

Take measures such as inserting resistors in lines connected to the input pins

(3) Power connectors

If the motor power supply V_{CC} is applied by mistake without connecting the GND part of the power connector when the product is operated, such as for test purposes, an overcurrent flows through the V_{CC} decoupling capacitor, C1, to the parasitic diode between the V_{DD} of the internal control IC and GND, and may damage the power supply pin block of the internal control IC.

Always connect the GND pin before supplying V_{CC}.

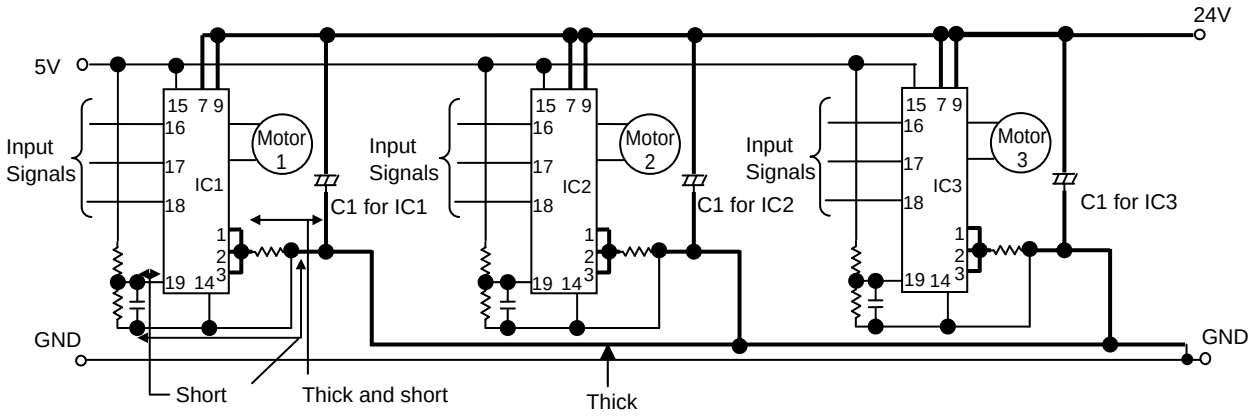


(4) Input Signal Lines

1) Do not use an IC socket to mount the driver, and instead solder the driver directly to the PC board to minimize fluctuations in the GND potential due to the influence of the resistance component and inductance component of the GND pattern wiring.
2) To reduce noise due to electromagnetic induction to small signal lines, do not design small signal lines (sensor signals, 5V or 3.3V power supply signal lines) that run parallel near the motor output lines OUT1 and OUT2.
3) Pins 5, 11 and 12 of this product are N.C pins. Do not connect any wiring to these pins.

(5) When mounting multiple drivers on a single PC board

When mounting multiple drivers on a single PC board, the GND design should mount a V_{CC} decoupling capacitor, C1, for each driver to stabilize the GND potential of the other drivers. The key wiring points are as follows.



ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK681-332-E	SIP-19 (Pb-Free)	20 / Fan-Fold