Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (t_p = 8/20µs)	P_{pk}	500	Watts
Peak Pulse Current (t_p = 8/20µs)	I_{PP}	25	A
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

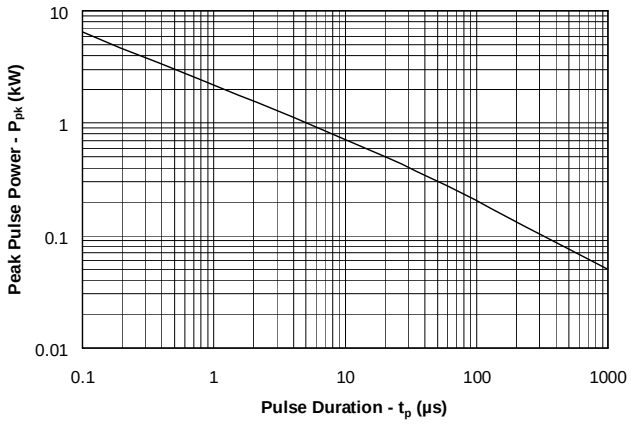
Electrical Characteristics (T=25°C)

SRDA3.3-4

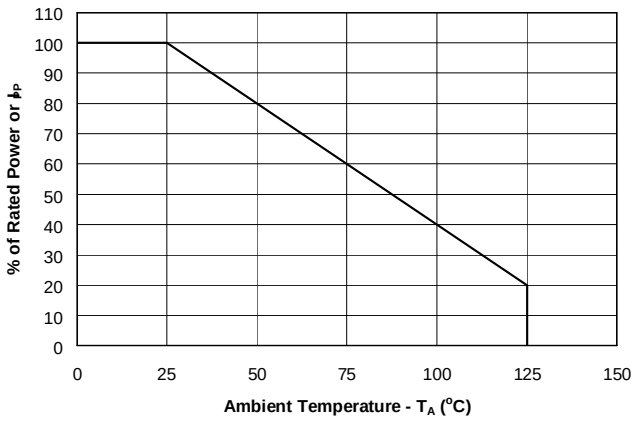
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				3.3	V
Punch-Through Voltage	V_{PT}	I_{PT} = 2µA	3.5			V
Snap-Back Voltage	V_{SB}	I_{SB} = 50mA	2.8			V
Reverse Leakage Current	I_R	V_{RWM} = 3.3V, T=25°C			1	µA
Clamping Voltage	V_C	I_{PP} = 1A, t_p = 8/20µs			5.3	V
Clamping Voltage	V_C	I_{PP} = 10A, t_p = 8/20µs			10	V
Clamping Voltage	V_C	I_{PP} = 25A, t_p = 8/20µs			15	V
Junction Capacitance	C_j	Between I/O pins and Ground V_R = 0V, f = 1MHz		8	15	pF
		Between I/O pins V_R = 0V, f = 1MHz		4		pF

Typical Characteristics

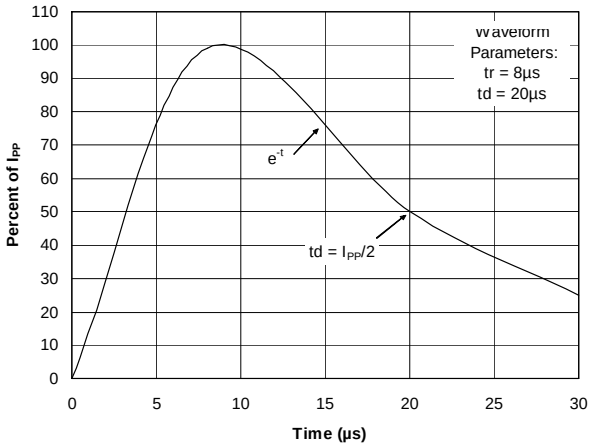
Non-Repetitive Peak Pulse Power vs. Pulse Time



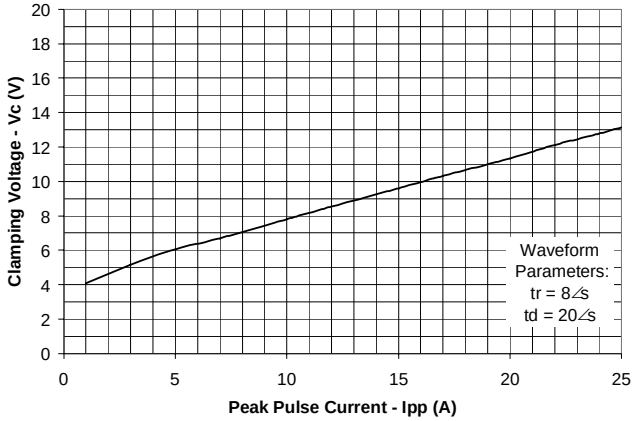
Power Derating Curve



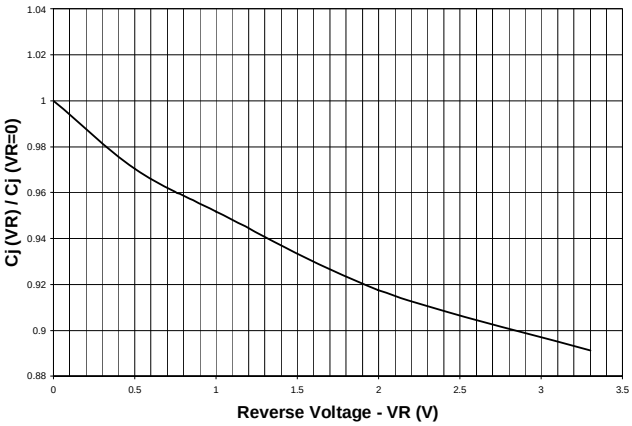
Pulse Waveform



Clamping Voltage vs. Peak Pulse Current



Normalized Junction Capacitance vs. Reverse Voltage



Applications Information

Device Connection Options for Protection of Four High-Speed Data Lines

These devices are designed to protect low voltage data lines operating at 3.3 volts. When the voltage on the protected line exceeds the punch-through or "turn-on" voltage of the TVS diode, the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry.

Data lines are connected at pins 1, 4, 6 and 7. Pins 5 and 8 should be connected directly to a ground plane. The path length is kept as short as possible to minimize parasitic inductance.

Note that pins 2 and 3 are connected internally to the cathode of the low voltage TVS. It is not recommended that these pins be directly connected to a DC source greater than the snap-back votlage (V_{SB}) as the device can latch on as described below.

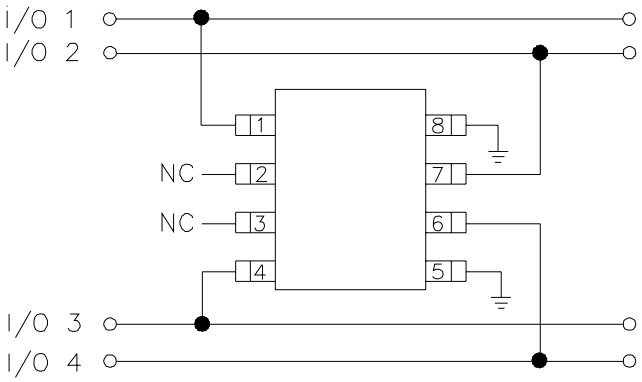
EPD TVS Characteristics

These devices are constructed using Semtech's proprietary EPD technology. By utilizing the EPD technology, the SRDA3.3-4 can effectively operate at 3.3V while maintaining excellent electrical characteristics.

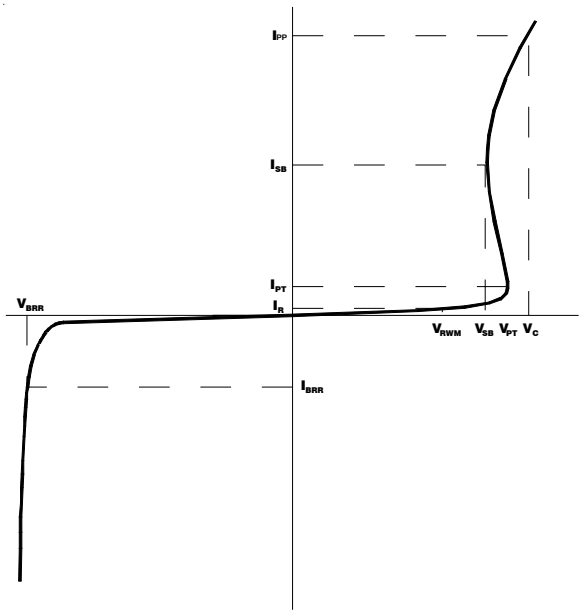
The EPD TVS employs a complex nppn structure in contrast to the pn structure normally found in traditional silicon-avalanche TVS diodes. Since the EPD TVS devices use a 4-layer structure, they exhibit a slightly different IV characteristic curve when compared to conventional devices. During normal operation, the device represents a high-impedance to the circuit up to the device working voltage (V_{RWM}). During an ESD event, the device will begin to conduct and will enter a low impedance state when the punch through voltage (V_{PT}) is exceeded. Unlike a conventional device, the low voltage TVS will exhibit a slight negative resistance characteristic as it conducts current. This characteristic aids in lowering the clamping voltage of the device, but must be considered in applications where DC voltages are present.

When the TVS is conducting current, it will exhibit a slight "snap-back" or negative resistance characteristics due to its structure. This point is defined on the curve by the snap-back voltage (V_{SB}) and snap-back current (I_{SB}). To return to a non-conducting state, the current through the device must fall below the I_{SB} (approximately <50mA) and the voltage must fall below the V_{SB} (normally 2.8 volts for a 3.3V device). If a 3.3V TVS is connected to 3.3V DC source, it will never fall below the snap-back voltage of 2.8V and will therefore stay in a conducting state.

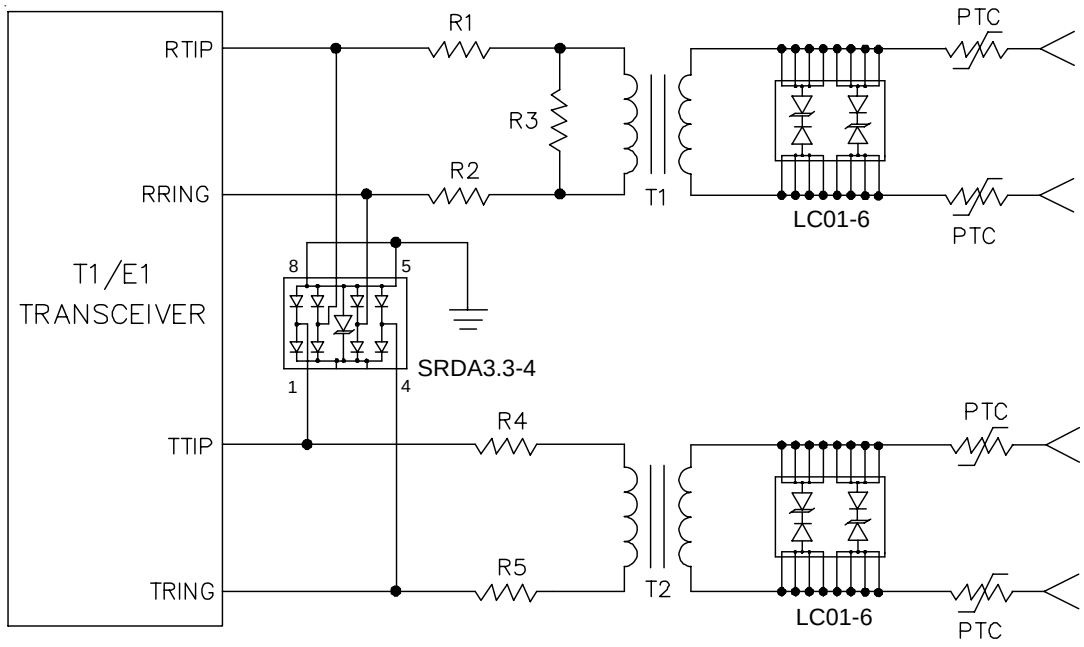
Data Line Protection Using Internal TVS Diode as Reference



EPD TVS IV Characteristic Curve

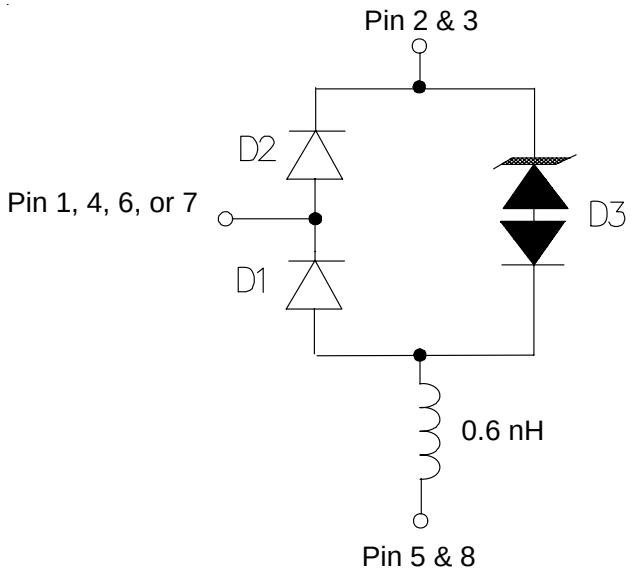


Typical Applications



T1/E1 Interface Protection (GR-1089 Long Haul)

Applications Information - Spice Model



SRDA3.3-4 Spice Model

SRDA3.3-4 Spice Parameters				
Parameter	**Unit**	**D1 (LCRD)**	**D2 (LCRD)**	**D3 (TVS)**
IS	Amp	2.092E-11	2.156E-12	6.09E-14
BV	Volt	680	240	3.54
VJ	Volt	0.62	0.64	13.8
RS	Ohm	0.180	0.155	0.220
IBV	Amp	1E-3	1E-3	10E-3
CJO	Farad	5.2E-12	6.2E-12	45E-12
TT	sec	2.541E-9	2.541E-9	2.541E-9
M	--	0.058	0.058	0.111
N	--	1.1	1.1	1.1
EG	eV	1.11	1.11	1.11

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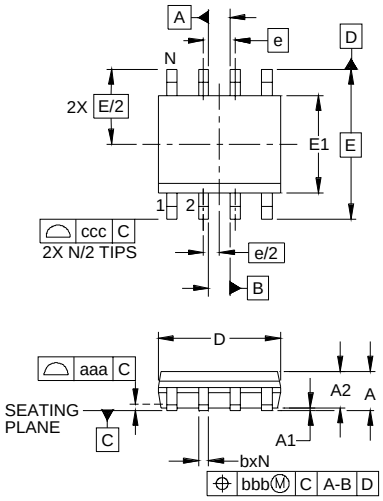
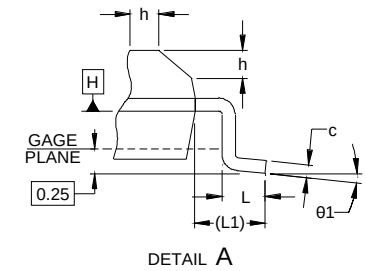
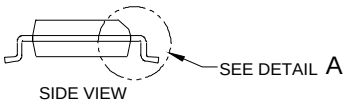
PROTECTION PRODUCTS

Outline Drawing - SO-8





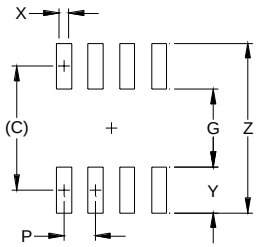


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AA.

Land Pattern - SO-8



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.

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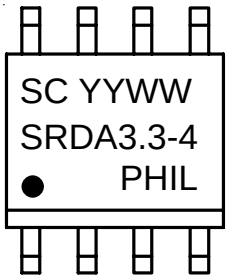
PROTECTION PRODUCTS

Marking Diagram



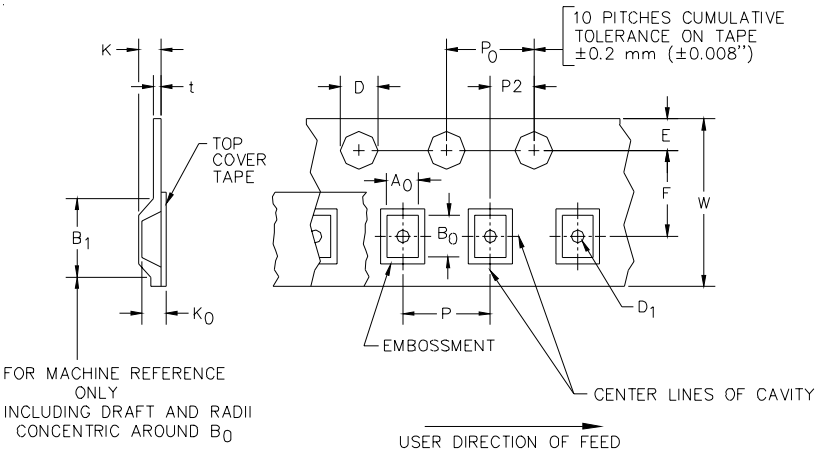
Note:
YYWW = Date Code

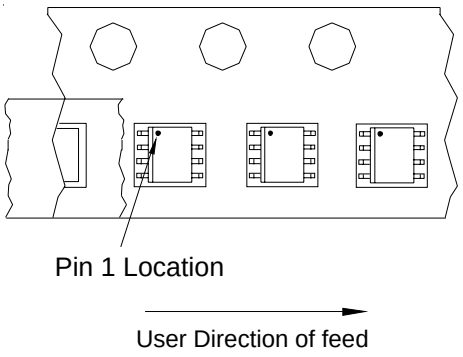
Ordering Information

Part Number	Lead Finish	Qty per Reel	Reel Size
SRDA3.3-4.TB	SnPb	500	7 Inch
SRDA3.3-4.TBT	Matte Sn	500	7 Inch

Note: Lead-free devices are RoHS/WEEE Compliant

Tape and Reel Specification





Device Orientation in Tape

A0	B0	K0
6.50 +/-0.20 mm	5.40 +/-0.20 mm	2.00 +/-0.10 mm

Tape Width	B, (Max)	D	D1	E	F	K (MAX)	P	P0	P2	T(MAX)	W
12 mm	8.2 mm	1.5 + 0.1 mm - 0.0 mm	1.5 mm	1.750±.10 mm	5.5±0.05 mm	4.5 mm	4.0±0.1 mm	4.0±0.1 mm	2.0±0.05 mm	0.4 mm	12.0 mm ±0.3

Contact Information for Semtech International AG

Taiwan Branch Tel: 886-2-2748-3380 Fax: 886-2-2748-3390

Korea Branch Tel: 82-2-527-4377 Fax: 82-2-527-4376

Shanghai Office Tel: 86-21-6391-0830 Fax: 86-21-6391-0831

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Semtech Switzerland GmbH Japan Branch Tel: 81-3-6408-0950 Fax: 81-3-6408-0951

Semtech Limited (U.K.) Tel: 44-1794-527-600 Fax: 44-1794-527-601

Semtech France SARL Tel: 33-(0)169-28-22-00 Fax: 33-(0)169-28-12-98

Semtech Germany GmbH Tel: 49-(0)8161-140-123 Fax: 49-(0)8161-140-124