ABSOLUTE MAXIMUM RATINGS

Parameter	Limit	Unit
Input Voltage, V_{IN} to GND	- 0.3 to 6.5	V
V_{EN} (See Detailed Description)	- 0.3 to 6.5	
Output Current (I_{OUT})	Short Circuit Protected	
Output Voltage (V_{OUT})	- 0.3 to V_{IN} + 0.3	V
Package Power Dissipation (P_D)[a]	305	mW
Package Thermal Resistance (θ_{JA})[b]	180	°C/W
Maximum Junction Temperature, $T_{J(max)}$	125	°C
Storage Temperature, T_{STG}	- 65 to 150	
Lead Temperature, T_L[c]	260	

Notes:
a. Derate 5.5 mW/°C above T_A = 70 °C.
b. Device mounted with all leads soldered or welded to multilayer 1S2P PC board.
c. Soldering for 5 s.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Limit	Unit
Input Voltage, V_{IN}	2.2 to 6	V
Operating Ambient Temperature T_A	- 40 to 85	°C

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified $V_{IN} = V_{OUT(nom)} + 1\ V = V_{EN}$ $V_{OUT} = 2.8\ V$, $C_{IN} = 1\ \mu F$, $C_{OUT} = 1\ \mu F$ $-40\ °C < T_A < 85\ °C$ for Full Temp.	Temp.[a]	Min.[b]	Typ.[c]	Max.[b]	Unit
Input Voltage Range	V_{IN}		Full	2.2		6	V
Feedback Voltage	V_{Adj}		Room	1.188	1.2	1.212	V
			Full	1.170		1.23	V
Output Voltage Range[f]	V_{OUTR}		Full	1.3		5	V
Output Voltage Accuracy	V_{OUT}	$V_{OUT} = 2.8\ V$, $I_L = 1\ mA$	Room	- 1		1	%
			Full	- 2.5		2.5	%
Line Regulation	LNR	V_{IN} range 3.8 V to 6 V, $I_L = 1\ mA$	Room		0.025	0.2	%/V
Load Regulation	LDR	V_{IN} 3.8 V, I_L step 1 mA to 250 mA	Room		0.001		%/mA
Dropout Voltage[d]	V_{DO}	$I_L = 250\ mA$	Room	180	225	300	mV
			Full			390	mV
Ground Current[e]	I_{GND}	V_{IN} 3.8 V, $I_L = 1\ mA$	Room		35	75	µA
			Full			85	µA
		V_{IN} 3.8 V, $I_L = 250\ mA$	Room		39	75	µA
			Full			85	µA
Shutdown Current	I_{VINLKG}		Full		0.035	1	µA
Output Current Limit	$I_{O-Limit}$	$V_O = 0\ V$	Room	275	500	800	mA
EN Input Current	I_{EN}	$EN = V_{IN} = 6\ V$	Full		0.004	1	µA
EN Pin Input Voltage	V_{ENH}	minimum V_{EN} output on	Full	1.2			V
	V_{ENL}	maximum V_{EN} output off	Full			0.4	V
Auto Discharge Resistance	R_{DIS}	$V_{OUT} = 2\ V$	Room		100		Ω
Thermal Shutdown Junction Temperature	T_{JSD}	minimum V_{EN} output on	Full		160		°C
Thermal Hysteresis	T_{HYST}	maximum V_{EN} output off	Full		20		°C
Output Noise Voltage (RMS)	e_N	BW = 10 Hz to 100 kHz, $1\ mA < I_{OUT} < 250\ mA$	Room		350		µV
Ripple Rejection	PSRR	$f = 1\ kHz$, $I_{OUT} = 10\ mA$			72		dB
		$f = 10\ kHz$, $I_{OUT} = 10\ mA$			53		dB
		$f = 100\ kHz$, $I_{OUT} = 10\ mA$			38		dB
Output Voltage Turn-On Time	t_{on}	EN to V_{OUT} delay; $I_{OUT} = 1\ mA$	Room		70		µs

Notes:

a. Room = 25 °C, Full = - 40 °C to 85 °C. Derate 5.5 mW/°C for SiP21110 above $T_A = 70\ °C$.

b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

d. Dropout voltage is defined as the input-to-output differential voltage at which the output voltage drops 2 % below its nominal value with constant load. For outputs = 2.2 V, dropout voltage is not applicable due to 2.2 V minimum input voltage requirement.

e. Ground current is specified for normal operation as well as “drop-out” operation.

f. The LDO output range is confined to 2.5 V minimum and 5.0 V maximum as a result of min V_{IN} is 2.2 V. For linear regulator outputs where the output voltages is less than 2.5 V the dropout voltage does not apply.

TIMING WAVEFORMS

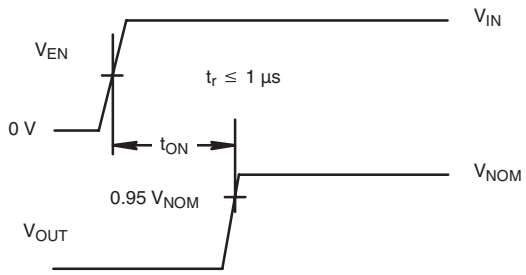
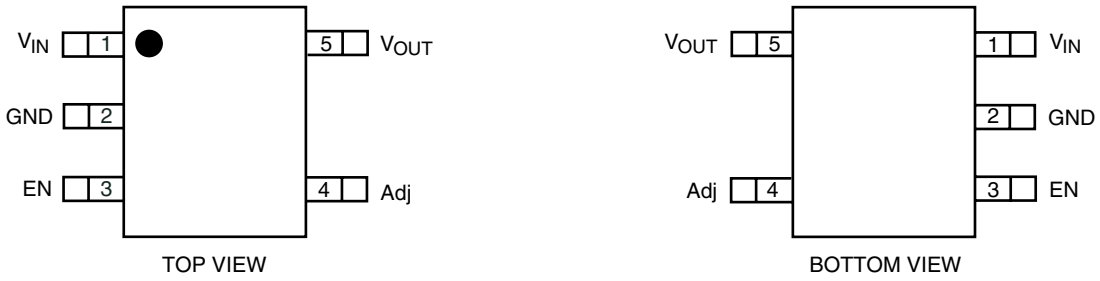


Figure 1.

PIN CONFIGURATION



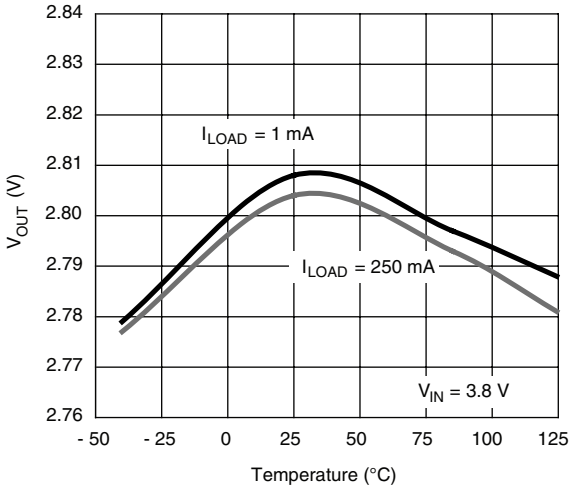
TSOT23-5L Package

Figure 2.

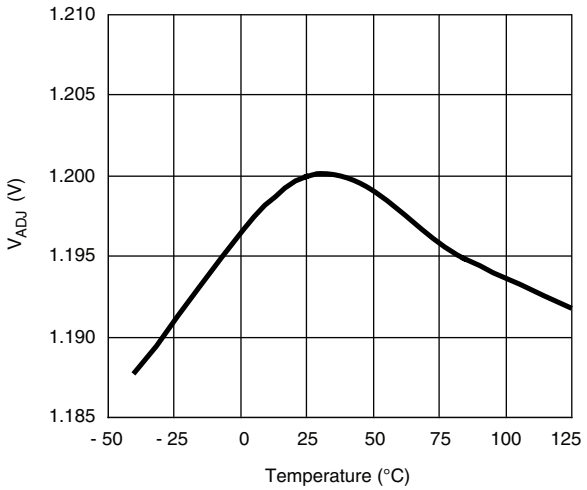
PIN DESCRIPTION		
Pin Number	**Name**	**Function**
3	EN	By applying less than 0.4 V to this pin, the device will be turned off. Connect this pin to V_{IN} if unused. Do not leave floating.
2	GND	Ground pin. For better thermal capability, directly connected to large ground plane.
1	V_{IN}	Input supply pin. Bypass this pin with a 1 µF ceramic or tantalum capacitor to ground.
5	V_{OUT}	Output voltage. Connect C_{OUT} between this pin and ground.
4	Adj	Adjust input pin. Connect feedback resistors to program the output voltage for trim value of 1.2 V.

ORDERING INFORMATION			
Part Number	**Marking**	**Temperature Range**	**Package**
SiP21110DT-T1-E3	AC	- 40 °C to 85 °C	TSOT23-5L

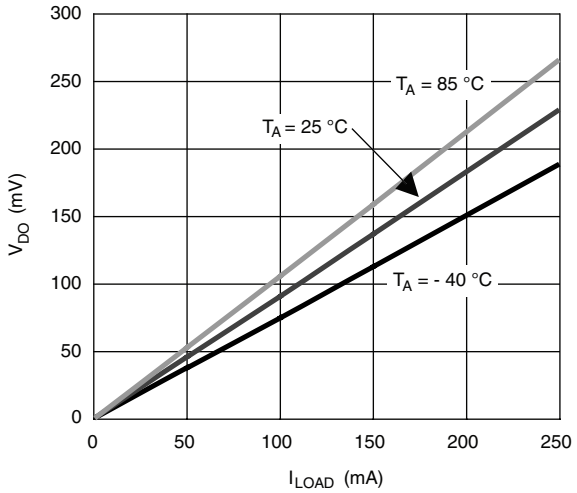
TYPICAL CHARACTERISTICS



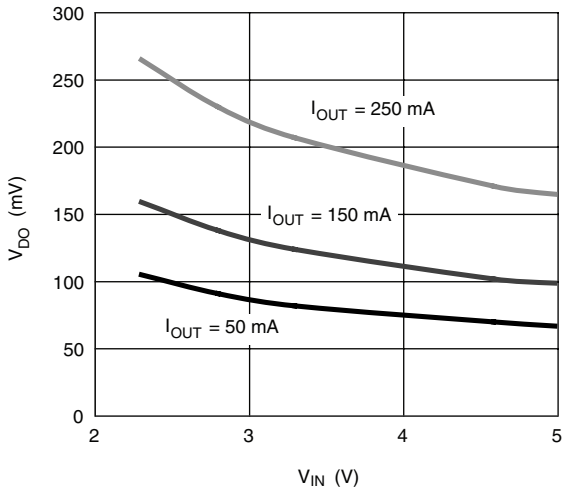
V_{OUT} vs. I_{LOAD} vs. Temperature



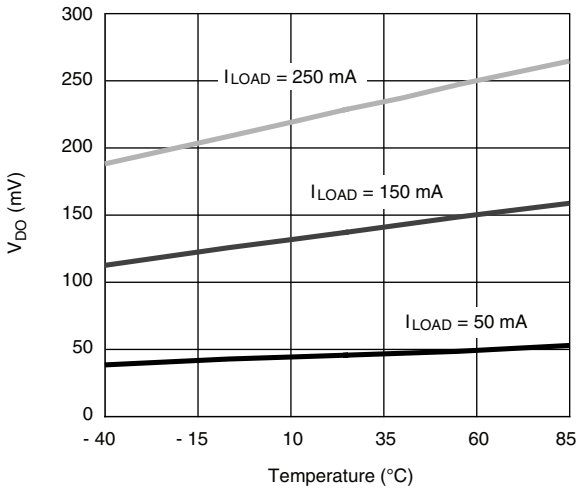
V_{ADJ} vs. Temperature



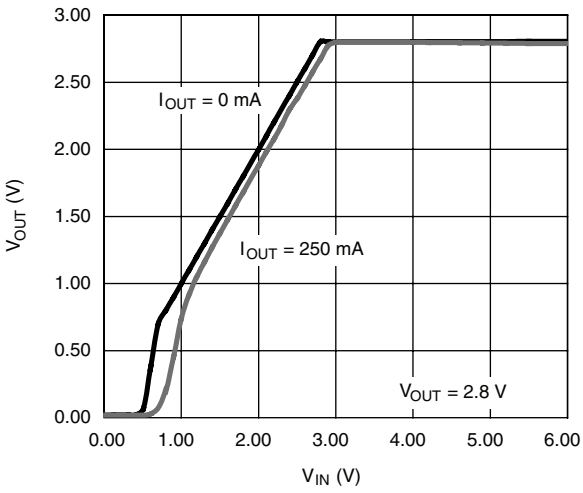
V_{DO} vs. I_{LOAD}



V_{DO} vs. V_{IN}

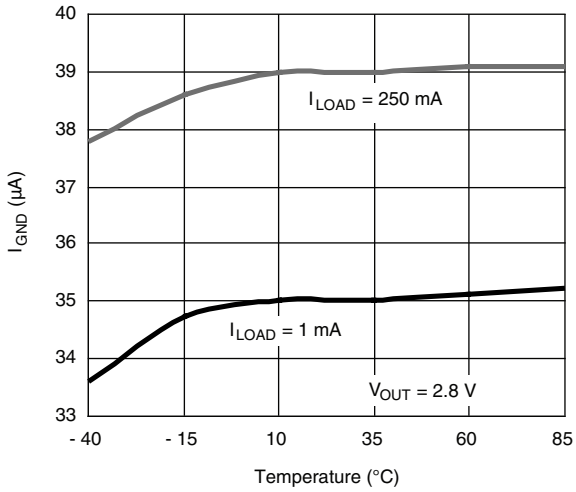


V_{DO} vs. Temperature

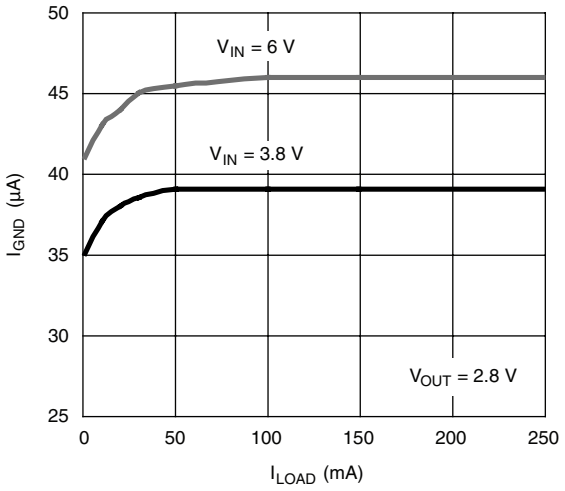


V_{OUT} vs. V_{IN}

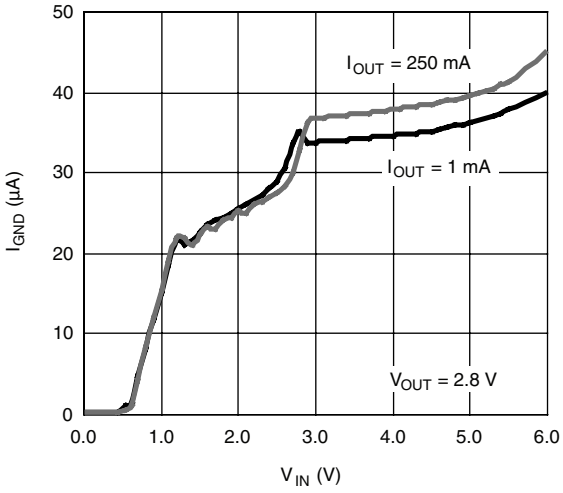
TYPICAL CHARACTERISTICS



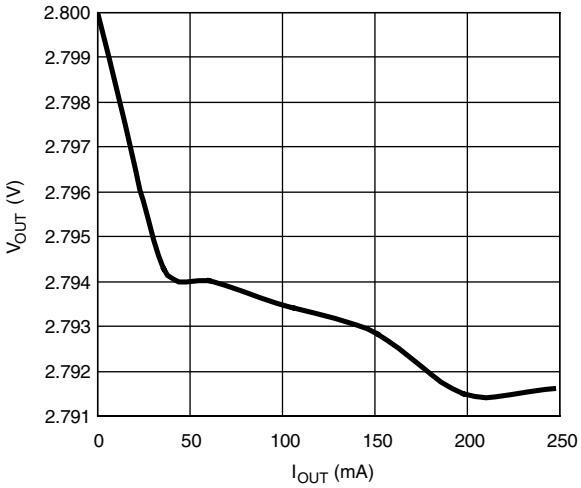
I_{GND} vs. Temperature



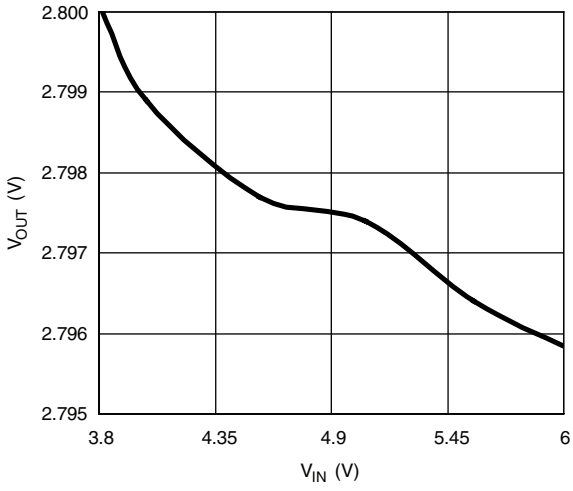
I_{GND} vs. I_{LOAD}



I_{GND} vs. V_{IN}

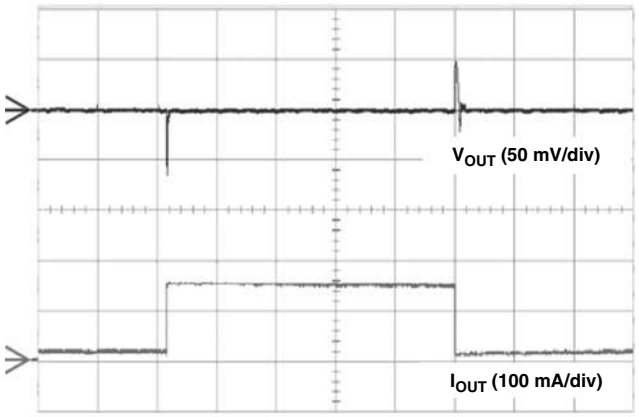


Load Regulation

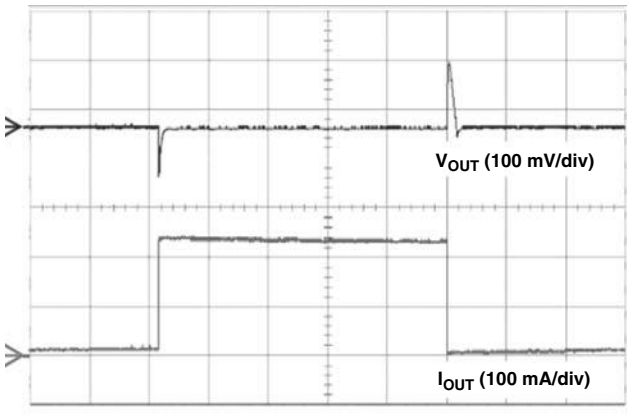


Line Regulation

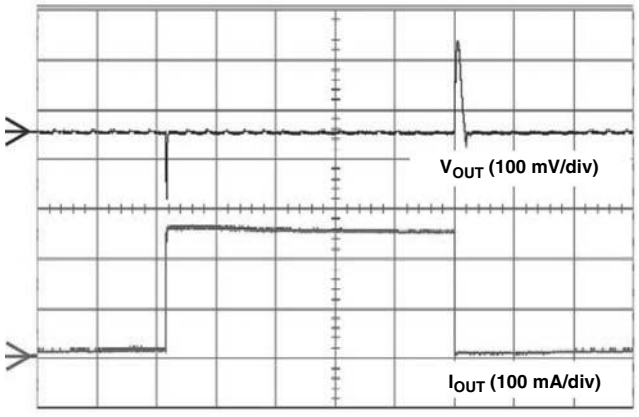
TYPICAL OPERATING WAVEFORMS



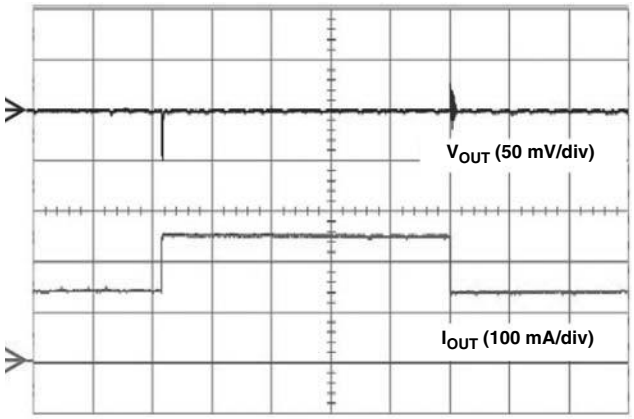
100 µs/div
V_{OUT} = 1.2 V, V_{IN} = 2.2 V, I_{OUT} = 10 mA to 150 mA
Load Transient Response



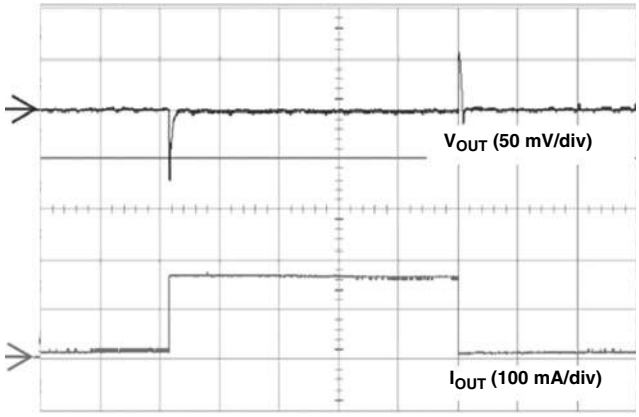
100 µs/div
V_{OUT} = 3.3 V, V_{IN} = 4.3 V, I_{OUT} = 10 mA to 250 mA
Load Transient Response



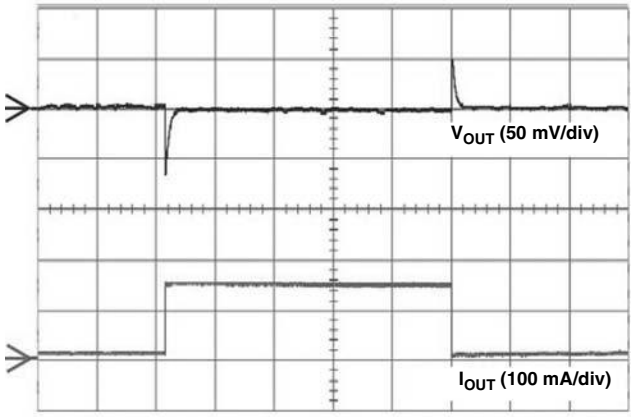
100 µs/div
V_{OUT} = 1.2 V, V_{IN} = 2.2 V, I_{OUT} = 10 mA to 250 mA
Load Transient Response



100 µs/div
V_{OUT} = 1.2 V, V_{IN} = 2.2 V, I_{OUT} = 50 mA to 250 mA
Load Transient Response

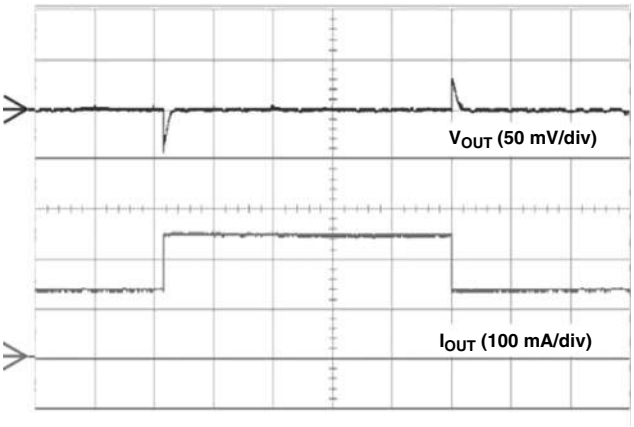


100 µs/div
V_{OUT} = 3.3 V, V_{IN} = 4.3 V, I_{OUT} = 10 mA to 150 mA
Load Transient Response

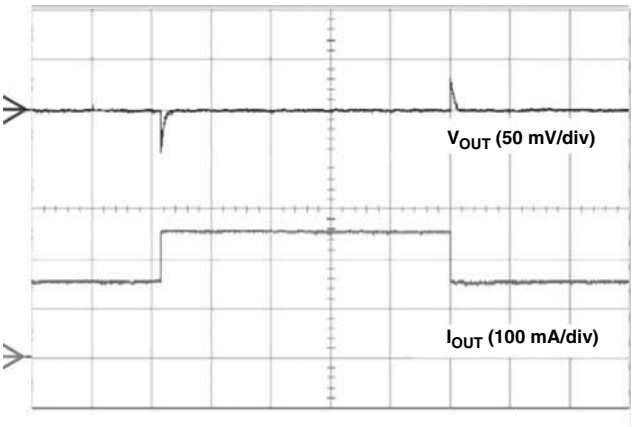


100 µs/div
V_{OUT} = 4.5 V, V_{IN} = 5.5 V, I_{OUT} = 10 mA to 150 mA
Load Transient Response

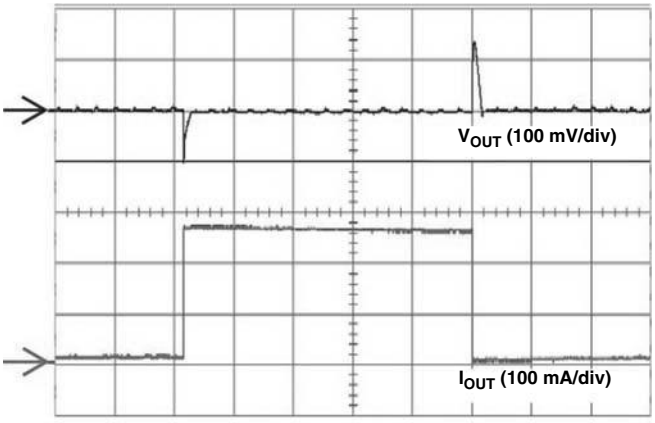
TYPICAL OPERATING WAVEFORMS



100 µs/div
V_{OUT} = 4.5 V, V_{IN} = 5.5 V, I_{OUT} = 150 mA to 250 mA
Load Transient Response

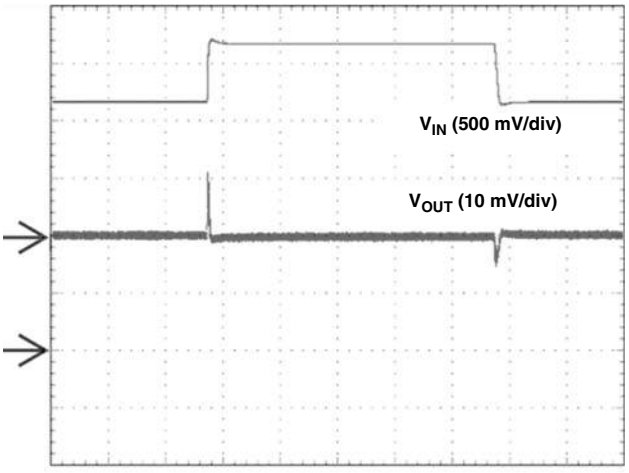


100 µs/div
V_{OUT} = 3.3 V, V_{IN} = 4.3 V, I_{OUT} = 150 mA to 250 mA
Load Transient Response

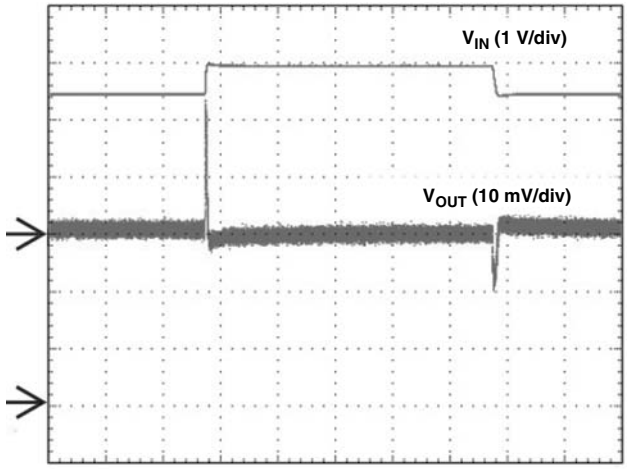


100 µs/div
V_{OUT} = 4.5 V, V_{IN} = 5.5 V, I_{OUT} = 10 mA to 250 mA
Load Transient Response

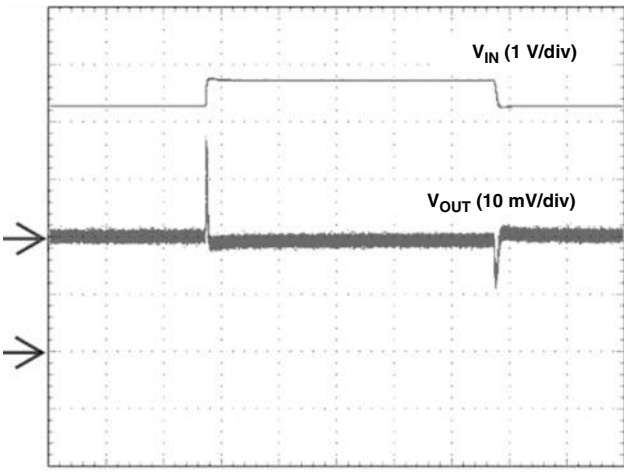
TYPICAL OPERATING WAVEFORMS



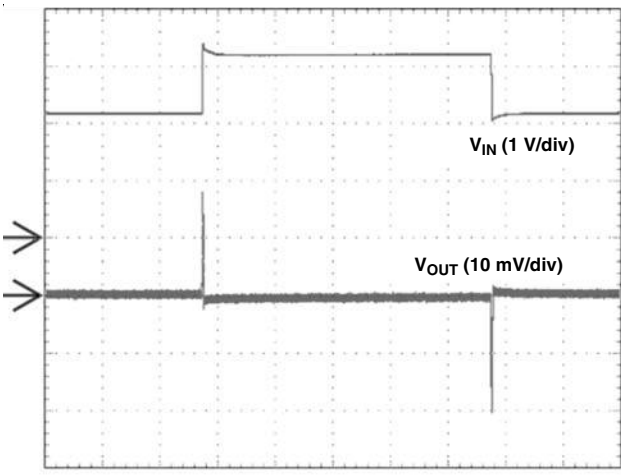
100 µs/div
V_{OUT} = 1.2 V, I_{OUT} = 250 mA, V_{IN} = 2.2 V to 2.7 V
Line Transient Response



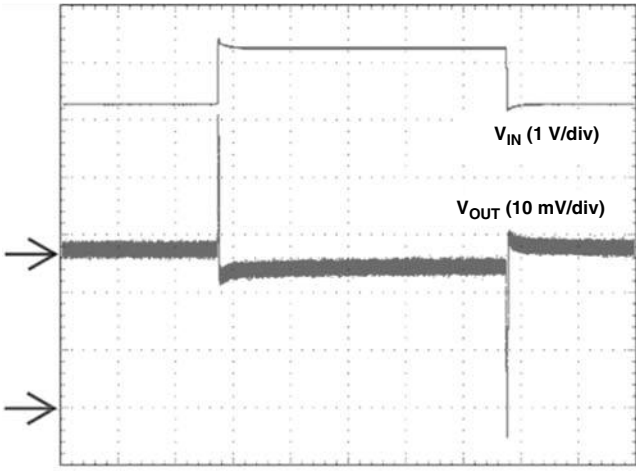
500 µs/div
V_{OUT} = 4.5 V, I_{OUT} = 250 mA, V_{IN} = 5.5 V to 6 V
Line Transient Response



500 µs/div
V_{OUT} = 3.3 V, I_{OUT} = 250 mA, V_{IN} = 4.3 V to 4.8 V
Line Transient Response



500 µs/div
V_{OUT} = 1.2 V, I_{OUT} = 250 mA, V_{IN} = 2.2 V to 3.2 V
Line Transient Response



500 µs/div
V_{OUT} = 3.3 V, I_{OUT} = 250 mA, V_{IN} = 4.3 V to 5.3 V
Line Transient Response

FUNCTIONAL BLOCK DIAGRAM

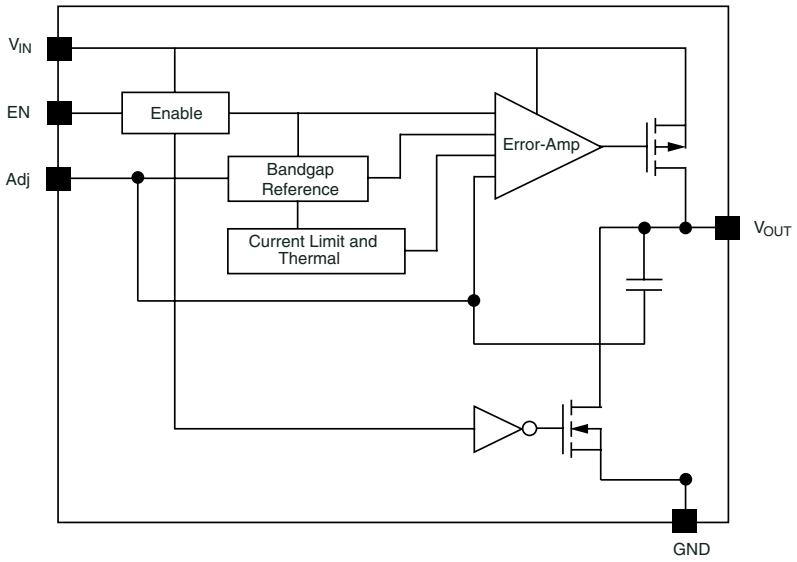


Figure 3.

DETAILED DESCRIPTION

As shown in the block diagram, the circuit consists of a bandgap reference, error amplifier, P-channel pass transistor and an internal feedback resistor voltage divider, which is used to monitor and control the output voltage.

A constant 1.2 V bandgap reference voltage is applied to the non-inverting input of the error amplifier. The error amplifier compares this reference with the feedback voltage on its inverting input and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled low. This increases the PMOS's gate to source voltage and allows more current to pass through the transistor to the output which increases the output voltage. Conversely, if the feedback voltage is higher than the reference voltage, the pass transistor gate is pulled high, decreasing the gate-to-source voltage, thereby allowing less current to pass to the output and causing it to drop.

Internal P-Channel Pass Transistor

A 0.9 Ω (typical) P-channel MOSFET is used as the pass transistor for SiP21110. The MOSFET transistor offers many advantages over the more, formerly, common PNP pass transistor designs, which ultimately result in longer battery lifetime. The main disadvantage of PNP pass transistors is that they require a certain base current to stay on, which significantly increases under heavy load conditions. In addition, during dropout, when the pass transistor saturates, the PNP regulators waste considerable current. In contrast, P-channel MOSFETS require virtually zero-base drive and do not suffer from the stated problems. These savings in base drive current translate to lower quiescent current which is typical around 35 µA as shown in the *Typical Characteristics.*

Shutdown and Auto-Dischage/No-Discharge

Bringing the EN voltage low will place the part in shutdown mode where the device output enters a high-impedance state and the quiescent current is reduced to below 1 µA, reducing the drain on the battery in standby mode and increasing standby time. Connect EN pin to input for normal operation. The output has an internal pull down to discharge the output to ground when the EN pin is low. The internal pull down is a 100 Ω typical resistor, which can discharge a 1 µF in less than 1 ms. Refer to *Typical Operating Waveforms* for turn-off waveforms.

Output Voltage Selection

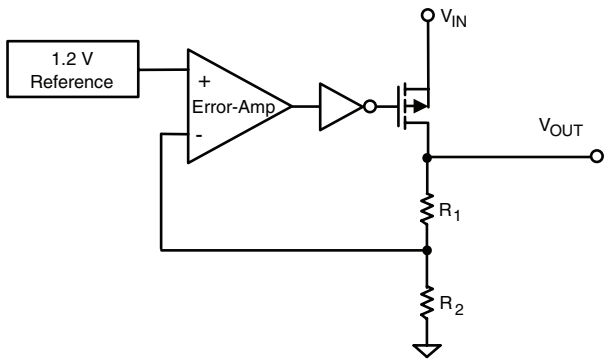


Figure 4.

The SiP21110 has a user-adjustable output that can be set through the resistor feedback network consisting of R_1 and R_2. R_2 range of 100K to 400K is recommended to be consistent with ground current specification. R_1 can then be determined by the following equation:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{ref}} - 1\right)$$

Where V_{ref} is typically 1.2 V. Use 1 % or better resistors for better output voltage accuracy (see Figure 4).

Current Limit

The SiP21110 includes a current limit block which monitors the current passing through the pass transistor through a current mirror and controls the gate voltage of the MOSFET, limiting the output current to 330 mA (typical). This current limit feature allows for the output to be shorted to ground for an indefinite amount of time without damaging the device.

Thermal-Overload Protection

The thermal overload protection limits the total power dissipation and protects the device from being damaged. When the junction temperature exceeds T_J = 150 °C, the device turns the P-Channel pass transistor off allowing the device to cool down. Once the temperature drops by about 20 °C, the thermal sensor turns the pass transistor on again and resumes normal operation. Consequently, a continuous thermal overload condition will result in a pulsed output. It is generally recommended to not exceed the junction temperature rating of 125 °C for continuous operation.

APPLICATION INFORMATION

Input/Output Capacitor Selection and Regulator Stability

It is recommended that a low ESR 1 µF capacitor be used on the SiP21110 input. A larger input capacitance with lower ESR would improve noise rejection and line-transient response. A larger input bypass capacitor may be required in applications involving long inductive traces between the source and LDO. The circuit is stable with only a small output capacitor equal to 6 nF/mA (≈ 1 µF at 150 mA) of load. Since the bandwidth of the error amplifier is around 1 MHz to 3 MHz and the dominant pole is at the output node, the capacitor should be capacitive in this range, i.e., for 150 mA load current, an ESR < 0.4 Ω is necessary. Parasitic inductance of about 10 nH can be tolerated. Applying a larger output capacitor would increase power supply rejection and improve load-transient response. Some ceramic dielectrics such as the Z5U and Y5V exhibit large capacitance and ESR variation over temperature. If such capacitors are used, a 2.2 µF or larger value may be needed to ensure stability over the industrial temperature range. If using higher quality ceramic capacitors, such as those with X7R and Y7R dielectrics, a 1 µF capacitor will be sufficient at all operating temperatures.

Operating Region and Power Dissipation

An important consideration when designing power supplies is the maximum allowable power dissipation of a part. The maximum power dissipation in any application is dependant on the maximum junction temperature, $T_{J(max)}$ = 125 °C, the ambient temperature, T_A, and the junction-to-ambient thermal resistance for the package, which is the summation of θ_{J-C}, the thermal resistance of the package, and θ_{C-A}, the thermal resistance through the PC board and copper traces. Power dissipation may be expressed as:

$$P_{(max)} = \frac{T_{J(max)} - T_A}{\theta_{J-C} + \theta_{C-A}}$$

The GND pin of the SiP21110 acts as both the electrical connection to GND as well as a path for channeling away heat. Connect this pin to a GND plane to maximize heat dissipation. Once maximum power dissipation is calculated using the equation above, the maximum allowable output current for any input/output potential can be calculated as

$$I_{OUT(max)} = \frac{P_{(max)}}{V_{IN} - V_{OUT}}$$

PCB Layout

The component placement around the LDO should be done carefully to achieve good dynamic line and load response. The input and noise capacitor should be kept close to the LDO. The rise in junction temperature depends on how efficiently the heat is carried away from junction-to-ambient. The junction-to-lead thermal impedance is a characteristic of the package and is fixed. The thermal impedance between lead-to-ambient can be reduced by increasing the copper area on PCB. Increase the input, output and ground trace area to reduce the junction-to-ambient thermal impedance.

Disclaimer

All product specifications and data are subject to change without notice.

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