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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter[1]	Symbol	Test Condition	Min[2]	Typ	Max[2]	Unit
Ambient Temperature	T_A	K-Grade	0	25	70	°C
Si3056 Supply Voltage, Digital[3]	V_D		3.0	3.3	3.6	V

Notes:
1. The Si3056 specifications are guaranteed when the typical application circuit (including component tolerance) and the Si3056 and any Si3018 or Si3019 are used. See Figure 17 on page 18 for typical application schematic.
2. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
3. 3.3 V applies to both the digital and serial interface and the digital signals RGDT/FSD, OFHK, RESET, M0, and M.

Table 2. Loop Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade, see Figure 1)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V_{TR}	I_L = 20 mA, MINI = 11, ILIM = 0, DCV = 00, DCR = 0	—	—	6.0	V
DC Termination Voltage	V_{TR}	I_L = 120 mA, MINI = 11, ILIM = 0, DCV = 00, DCR = 0	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, MINI = 00, ILIM = 0, DCV = 11, DCR = 0	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 120 mA, MINI = 00, ILIM = 0, DCV = 11, DCR = 0	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, MINI = 00, ILIM = 1, DCV = 11, DCR = 0	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 60 mA, MINI = 00, ILIM = 1, DCV = 11, DCR = 0	40	—	—	V
DC Termination Voltage	V_{TR}	I_L = 50 mA, MINI = 00, ILIM = 1, DCV = 11, DCR = 0	—	—	40	V
On Hook Leakage Current	I_{LK}	V_{TR} = –48 V	—	—	5	µA
Operating Loop Current	I_{LP}	MINI = 00, ILIM = 0	10	—	120	mA
Operating Loop Current	I_{LP}	MINI = 00, ILIM = 1	10	—	60	mA
DC Ring Current		DC current flowing through ring detection circuitry	—	1.5	3	µA
Ring Detect Voltage*	V_{RD}	RT = 0	13.5	15	16.5	V_{rms}
Ring Detect Voltage*	V_{RD}	RT = 1	19.35	21.5	23.65	V_{rms}
Ring Frequency	F_R		13	—	68	Hz
Ringer Equivalence Number	REN		—	—	0.2	

***Note:** The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.

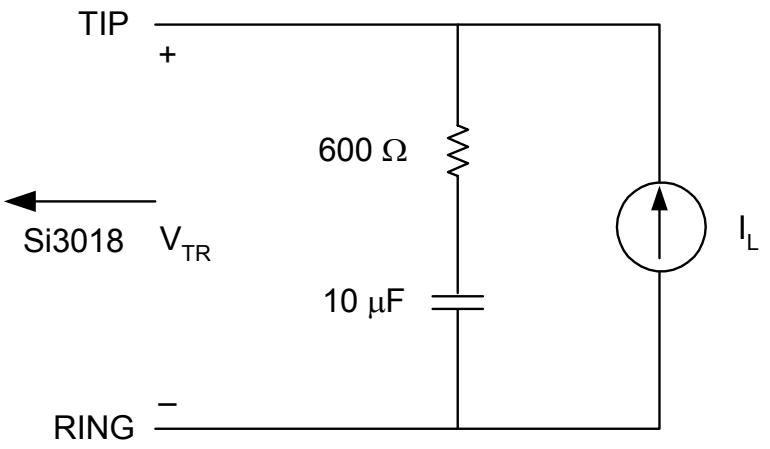


Figure 1. Test Circuit for Loop Characteristics

Table 3. DC Characteristics, V_D = 3.3 V

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.4	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	2.4	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 2 mA	—	—	0.35	V
Input Leakage Current	I_L		–10	—	10	µA
Power Supply Current, Digital[1]	I_D	V_D pin	—	15	—	mA
Total Supply Current, Sleep Mode[1]	I_D	PDN = 1, PDL = 0	—	9	—	mA
Total Supply Current, Deep Sleep[1,2]	I_D	PDN = 1, PDL = 1	—	1	—	mA

Notes:
1. All inputs at 0.4 or V_D – 0.4 (CMOS levels). All inputs are held static except clock and all outputs unloaded (Static I_{OUT} = 0 mA).
2. RGDT is not functional in this state.

Table 4. AC Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade; see Figure 17 on page 18)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sample Rate[1]	Fs	Fs = F_{PLL2}/5120	7.2	—	16	kHz
PLL Output Clock Frequency[1]	F_{PLL1}	F_{PLL1} = (F_{MCLK} x M)/N	—	98.304	—	MHz
Transmit Frequency Response		Low –3 dBFS Corner	—	0	—	Hz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 0	—	5	—	Hz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 1[11]	—	200	—	Hz
Transmit Full Scale Level[2,3]	V_{FS}	FULL = 0 (0 dBm)	—	1.1	—	V_{PEAK}
		FULL = 1[11](3.2 dBm)	—	1.58	—	V_{PEAK}
		FULL2 = 1 (6.0 dBm)	—	2.16	—	V_{PEAK}
Receive Full Scale Level[2,4]	V_{FS}	FULL = 0 (0 dBm)		1.1		V_{PEAK}
		FULL = 1[11](3.2 dBm)	—	1.58	—	V_{PEAK}
		FULL2 = 1 (6.0 dBm)	—	2.16	—	V_{PEAK}
Dynamic Range[5,6,7]	DR	ILIM = 0, DCV = 11, DCR = 0, I_L = 100 mA, MINI = 00	—	80	—	dB
Dynamic Range[5,6,7]	DR	ILIM = 0, DCV = 00, DCR = 0, I_L = 20 mA, MINI = 11	—	80	—	dB
Dynamic Range[5,6,7]	DR	ILIM = 1, DCV = 11, DCR = 0, I_L = 50 mA, MINI = 00	—	80	—	dB
Transmit Total Harmonic Distortion[8,9]	THD	ILIM = 0, DCV = 11, DCR = 0, I_L = 100 mA, MINI = 00	—	–72	—	dB
Transmit Total Harmonic Distortion[8,9]	THD	ILIM = 0, DCV = 00, DCR = 0, I_L = 20 mA, MINI = 11	—	–78	—	dB

Notes:

1. See Figure 26 on page 37.
2. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1.
3. With FULL = 1, the transmit and receive full scale level of +3.2 dBm can be achieved with a 600 Ω ac termination, while the transmit and receive level in dBm varies with reference impedance, the DAA will transmit and receive 1 dBV into all reference impedances in “FULL” mode. With FULL2 = 1, the transmit and receive full scale level of +6.0 dBm can be achieved with a 600 Ω ac termination. In “FULL2” mode, the DAA will transmit and receive +1.5 dBV into all reference impedances.
4. Receive full scale level produces –0.9 dBFS at SDO.
5. DR = 20 x log (RMS V_{FS}/RMS V_{IN}).+ 20 x log (RMS V_{IN}/RMS noise). The RMS noise measurement excludes harmonics. V_{FS} is the 0 dBm full-scale level.
6. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths. V_{IN} = 1 kHz, –3 dBFS, Fs = 10300 Hz.
7. When using the Si3010 line-side, the typical DR values will be approximately 10 dB lower.
8. THD = 20 x log (RMS distortion/RMS signal). V_{IN} = 1 kHz, –3 dBFS, Fs = 10300 Hz.
9. When using the Si3010 line-side, the typical THD values will be approximately 10 dB higher.
10. DR_{CID} = 20 x log (RMS V_{CID}/RMS V_{IN}) + 20 x log(RMS V_{IN}/RMS noise). V_{CID} is the 6 V full-scale level for the typical application circuit in Figure 17. With the enhanced CID circuit, the V_{CID} full-scale level is 1.5 V peak, and DR_{CID} increases to 62 dB.
11. Available on the Si3019 line-side device only.

Table 4. AC Characteristics (Continued)
(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade; see Figure 17 on page 18)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Receive Total Harmonic Distortion[8,9]	THD	ILIM = 0, DCV = 00, DCR = 0, I_L = 20 mA, MINI = 11	—	–78	—	dB
Receive Total Harmonic Distortion[8,9]	THD	ILIM = 1, DCV = 11, DCR = 0, I_L = 50 mA, MINI = 00	—	–78	—	dB
Dynamic Range (caller ID mode)[10,7]	DR_{CID}	VIN = 1 kHz, –13 dBFS	—	50	—	dB
Caller ID Full Scale Level[10]	V_{CID}		—	6	—	V_{PEAK}
AOUT Low Level Current			—	—	10	mA
AOUT High Level Current			—	—	10	mA

Notes:
1. See Figure 26 on page 37.
2. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1.
3. With FULL = 1, the transmit and receive full scale level of +3.2 dBm can be achieved with a 600 Ω ac termination, while the transmit and receive level in dBm varies with reference impedance, the DAA will transmit and receive 1 dBV into all reference impedances in “FULL” mode. With FULL2 = 1, the transmit and receive full scale level of +6.0 dBm can be achieved with a 600 Ω ac termination. In “FULL2” mode, the DAA will transmit and receive +1.5 dBV into all reference impedances.
4. Receive full scale level produces –0.9 dBFS at SDO.
5. DR = 20 x log (RMS V_{FS}/RMS V_{IN}).+ 20 x log (RMS V_{IN}/RMS noise). The RMS noise measurement excludes harmonics. V_{FS} is the 0 dBm full-scale level.
6. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths. V_{IN} = 1 kHz, –3 dBFS, Fs = 10300 Hz.
7. When using the Si3010 line-side, the typical DR values will be approximately 10 dB lower.
8. THD = 20 x log (RMS distortion/RMS signal). V_{IN} = 1 kHz, –3 dBFS, Fs = 10300 Hz.
9. When using the Si3010 line-side, the typical THD values will be approximately 10 dB higher.
10. DR_{CID} = 20 x log (RMS V_{CID}/RMS V_{IN}) + 20 x log(RMS V_{IN}/RMS noise). V_{CID} is the 6 V full-scale level for the typical application circuit in Figure 17. With the enhanced CID circuit, the V_{CID} full-scale level is 1.5 V peak, and DR_{CID} increases to 62 dB.
11. Available on the Si3019 line-side device only.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_D	–0.5 to 3.6	V
Input Current, Si3056 Digital Input Pins	I_{IN}	±10	mA
Digital Input Voltage	V_{IND}	–0.3 to (V_D + 0.3)	V
Operating Temperature Range	T_A	–40 to 100	°C
Storage Temperature Range	T_{STG}	–65 to 150	°C

Note: Permanent device damage can occur if the above absolute maximum ratings are exceeded. Restrict functional operation to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods might affect device reliability.

Table 6. Switching Characteristics—General Inputs

(V_D = 3.0 to 3.6 V, T_A = 70 °C for K-Grade, C_L = 20 pF)

Parameter[1]	Symbol	Min	Typ	Max	Unit
Cycle Time, MCLK	t_{mc}	16.67	—	1000	ns
MCLK Duty Cycle	t_{dty}	40	50	60	%
MCLK Jitter Tolerance	t_{jitter}	—	—	±2	ns
Rise Time, MCLK	t_r	—	—	5	ns
Fall Time, MCLK	t_f	—	—	5	ns
MCLK Before $\overline{\text{RESET}}$ ↑	t_{mr}	10	—	—	cycles
$\overline{\text{RESET}}$ Pulse Width[2]	t_{rl}	250	—	—	ns
M0, M Before $\overline{\text{RESET}}$↑[3]	t_{mxr}	20	—	—	ns

Notes:
1. All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_D – 0.4 V, V_{IL} = 0.4 V. Rise and fall times are referenced to the 20% and 80% levels of the waveform.
2. The minimum $\overline{\text{RESET}}$ pulse width is the greater of 250 ns or 10 MCLK cycle times.
3. M0 and M are typically connected to V_D or GND and should not be changed during normal operation.

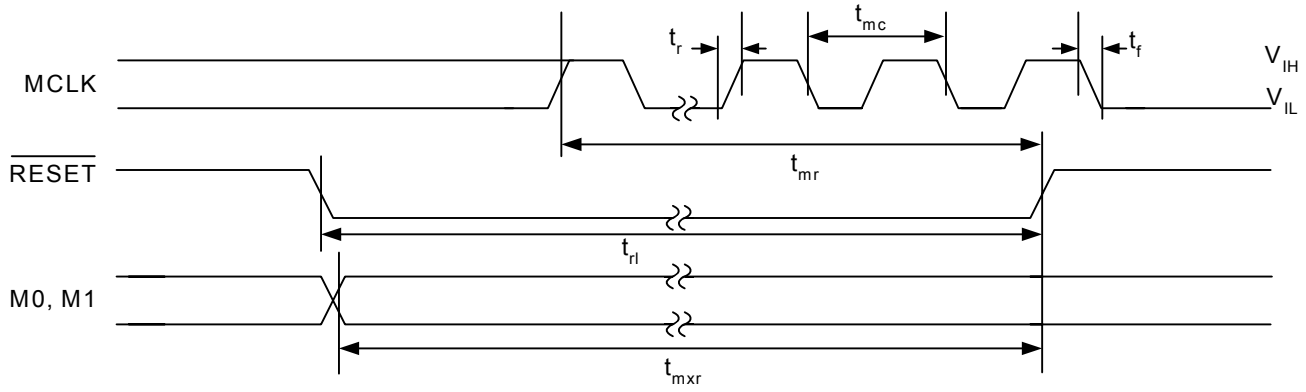


Figure 2. General Inputs Timing Diagram

Table 7. Switching Characteristics—Serial Interface (Master Mode, DCE = 0)
(V_D = 3.0 to 3.6 V, T_A = 70 °C for K-Grade, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Cycle time, SCLK	t_c	244	1/256 Fs	—	ns
SCLK Duty Cycle	t_{dty}	—	50	—	%
Delay Time, SCLK↑ to $\overline{\text{FSYNC}}$↓	t_{d1}	—	—	20	ns
Delay Time, SCLK↑ to SDO Valid	t_{d2}	—	—	20	ns
Delay Time, SCLK↑ to $\overline{\text{FSYNC}}$↑	t_{d3}	—	—	20	ns
Setup Time, SDI Before SCLK ↓	t_{su}	25	—	—	ns
Hold Time, SDI After SCLK ↓	t_h	20	—	—	ns
Setup Time, FC↑ Before SCLK↑	t_{sfc}	40	—	—	ns
Hold time, FC↑ After SCLK↑	t_{hfc}	40	—	—	ns

Note: All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, V_{IL} = 0.4 V.

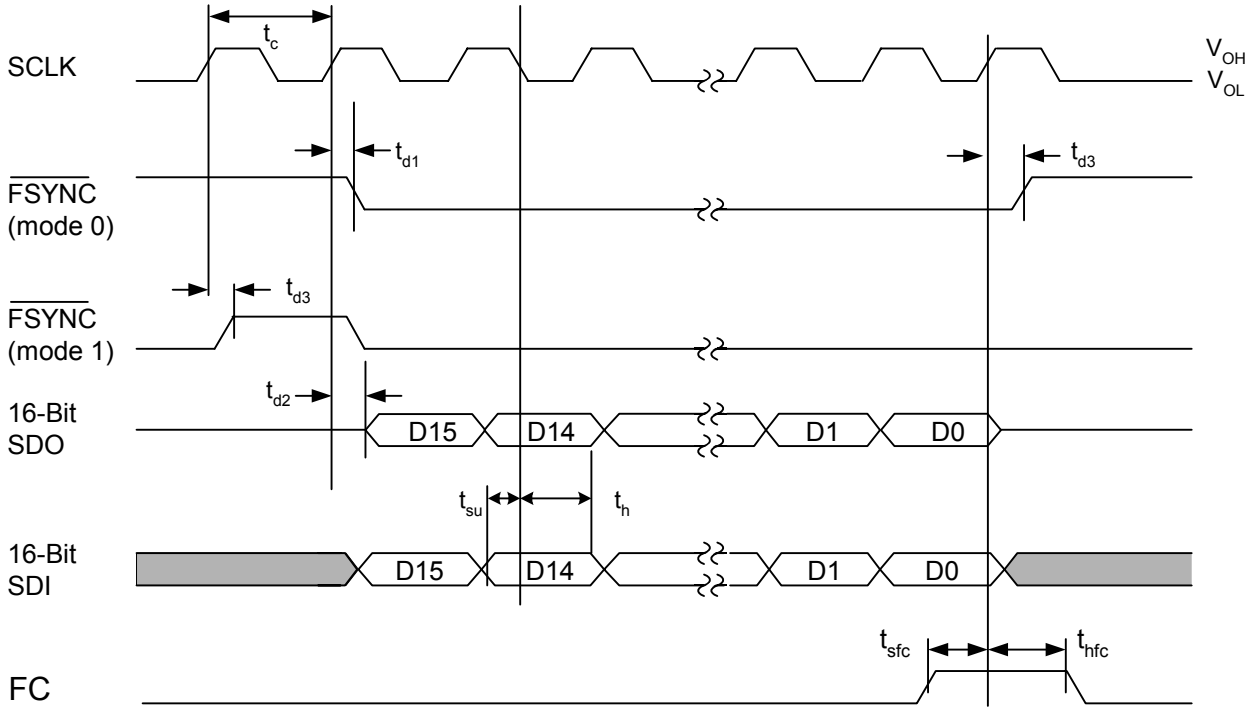


Figure 3. Serial Interface Timing Diagram (DCE = 0)

Table 8. Switching Characteristics—Serial Interface (Master Mode, DCE = 1, FSD = 0)
(V_A = Charge Pump, V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade, C_L = 20 pF)

Parameter[1,2]	Symbol	Min	Typ	Max	Unit
Cycle Time, SCLK	t_c	244	1/256 Fs	—	ns
SCLK Duty Cycle	t_{dty}	—	50	—	%
Delay Time, SCLK↑ to $\overline{\text{FSYNC}}$↑	t_{d1}	—	—	20	ns
Delay Time, SCLK↑ to $\overline{\text{FSYNC}}$↓	t_{d2}	—	—	20	ns
Delay Time, SCLK↑ to SDO valid	t_{d3}	—	—	20	ns
Delay Time, SCLK↑ to SDO Hi-Z	t_{d4}	—	—	20	ns
Delay Time, SCLK↑ to FSD↓	t_{d5}	—	—	20	ns
Delay Time, SCLK↑ to FSD↑	t_{d6}	—	—	20	ns
Setup Time, SDO Before SCLK↓	t_{su}	25	—	—	ns
Hold Time, SDO After SCLK↓	t_h	20	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, $V_{IL} = 0.4$ V.
2. See "5.27.Multiple Device Support" on page 38 for functional details.

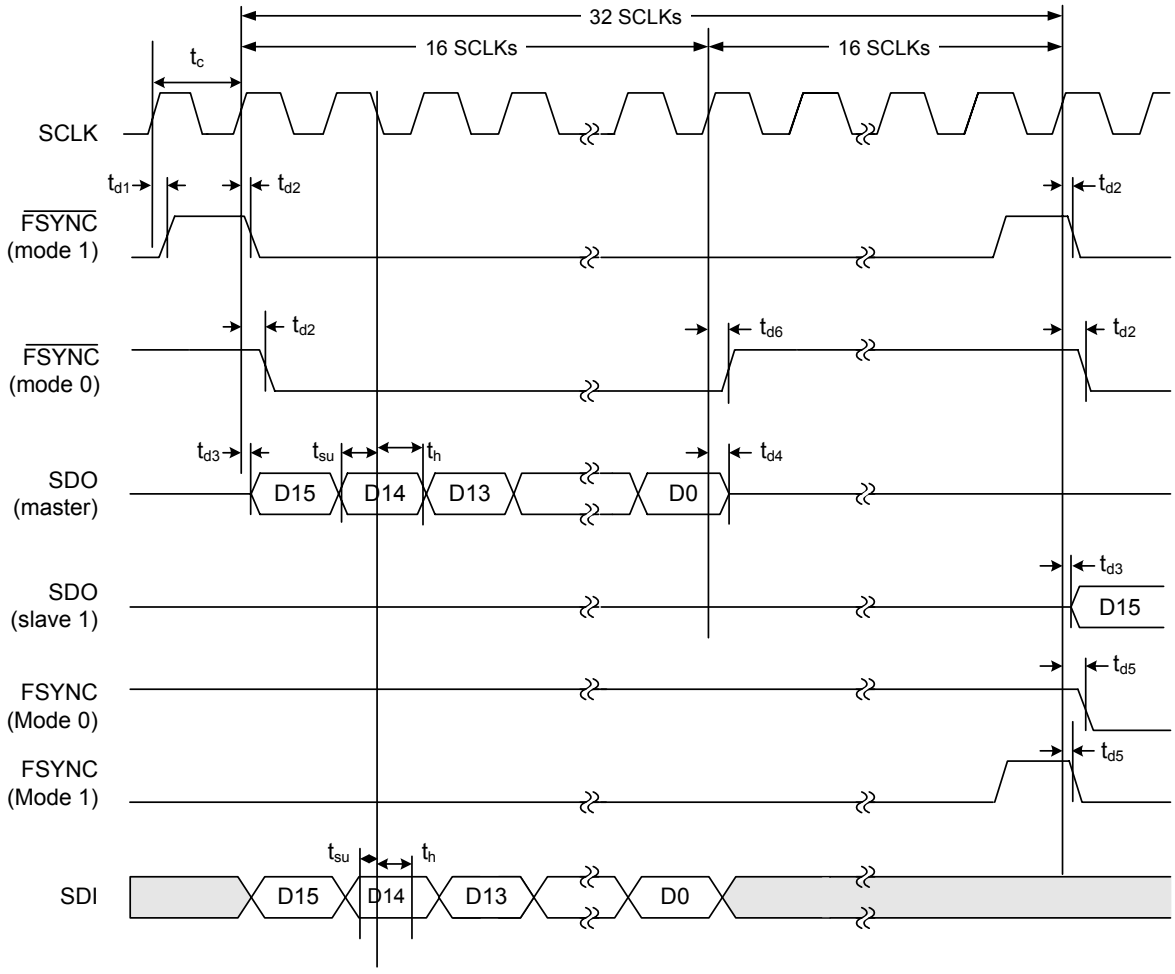


Figure 4. Serial Interface Timing Diagram (DCE = 1, FSD = 0)

Table 9. Switching Characteristics—Serial Interface (Master Mode, DCE = 1, FSD = 1)
(V_D = 3.0 to 3.6 V, T_A = 70 °C for K-Grade, C_L = 20 pF)

Parameter[1, 2]	Symbol	Min	Typ	Max	Unit
Cycle Time, SCLK	t_c	244	1/256 Fs	—	ns
SCLK Duty Cycle	t_{dty}	—	50	—	%
Delay Time, SCLK↑ to $\overline{\text{FSYNC}}$↑	t_{d1}	—	—	20	ns
Delay Time, SCLK↑ to $\overline{\text{FSYNC}}$↓	t_{d2}	—	—	20	ns
Delay Time, SCLK↑ to SDO Valid	t_{d3}	—	—	20	ns
Delay Time, SCLK↑ to SDO Hi-Z	t_{d4}	—	—	20	ns
Delay Time, SCLK↑ to FSD↓	t_{d5}	—	—	20	ns
Setup Time, SDO Before SCLK↓	t_{su}	25	—	—	ns
Hold Time, SDO After SCLK↓	t_h	20	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, V_{IL} = 0.4 V.
2. See "5.27.Multiple Device Support" on page 38 for functional details.

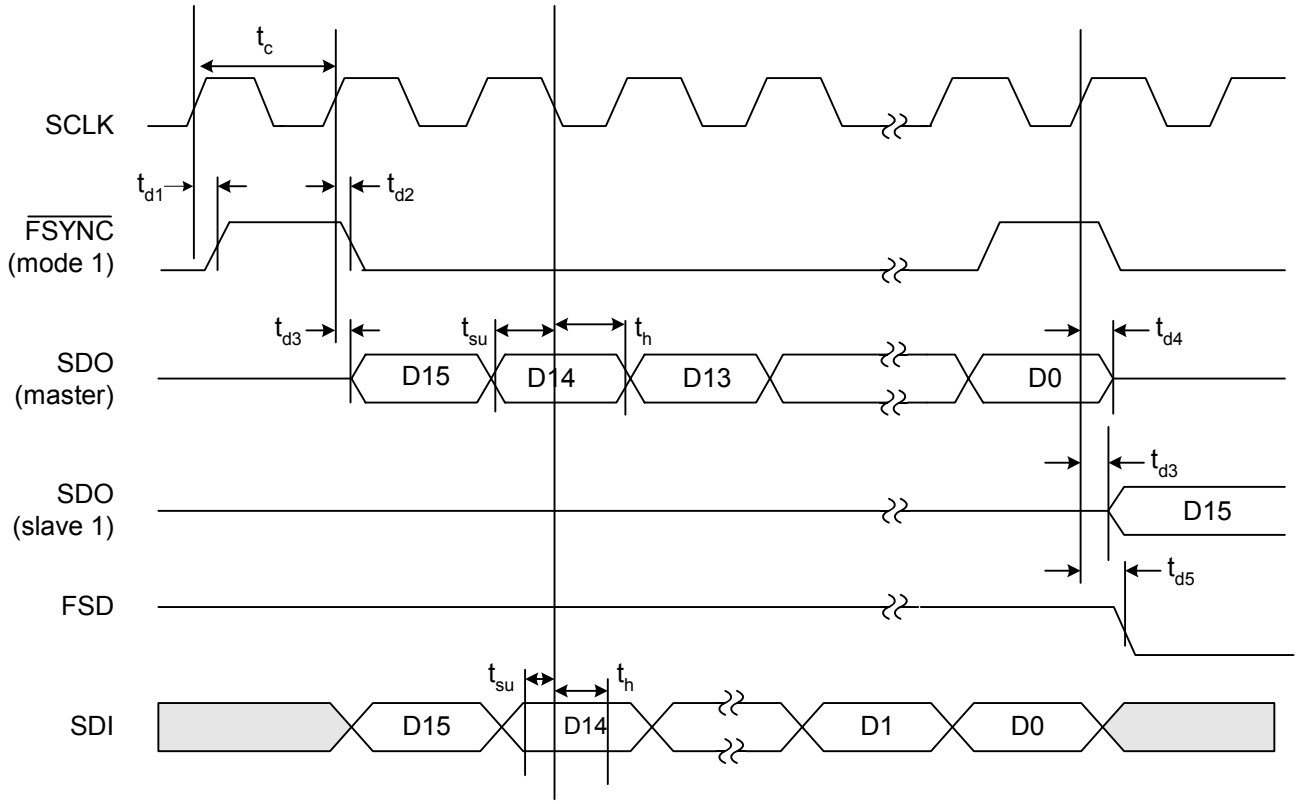


Figure 5. Serial Interface Timing Diagram (DCE = 1, FSD = 1)

Table 10. Switching Characteristics—Serial Interface (Slave Mode, DCE = 1, FSD = 1)
(V_A = Charge Pump, V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Cycle Time, MCLK	t_c	244	1/256 Fs	—	ns
Setup Time, FSYNC↑ before MCLK↓*	t_{su1}	—	—	20	ns
Delay Time, FSYNC↑ after MCLK↓*	t_{d1}	—	—	20	ns
Setup Time, SDI before MCLK↓	t_{su3}	—	—	20	ns
Hold Time, SDI After MCLK↓	t_{h2}	—	—	20	ns
Delay Time, MCLK↑ to SDO	t_{d3}	—	—	20	ns
Delay Time, MCLK↑ to FSYNC↑	t_{d1}	—	—	20	ns
Delay Time, MCLK↑ to FSYNC↓	t_{d2}	—	—	20	ns
***Note:** T_{su1} and T_{h1} are listed for applications where the controller drives the MCLK and FSYNC instead of a master DAA.					

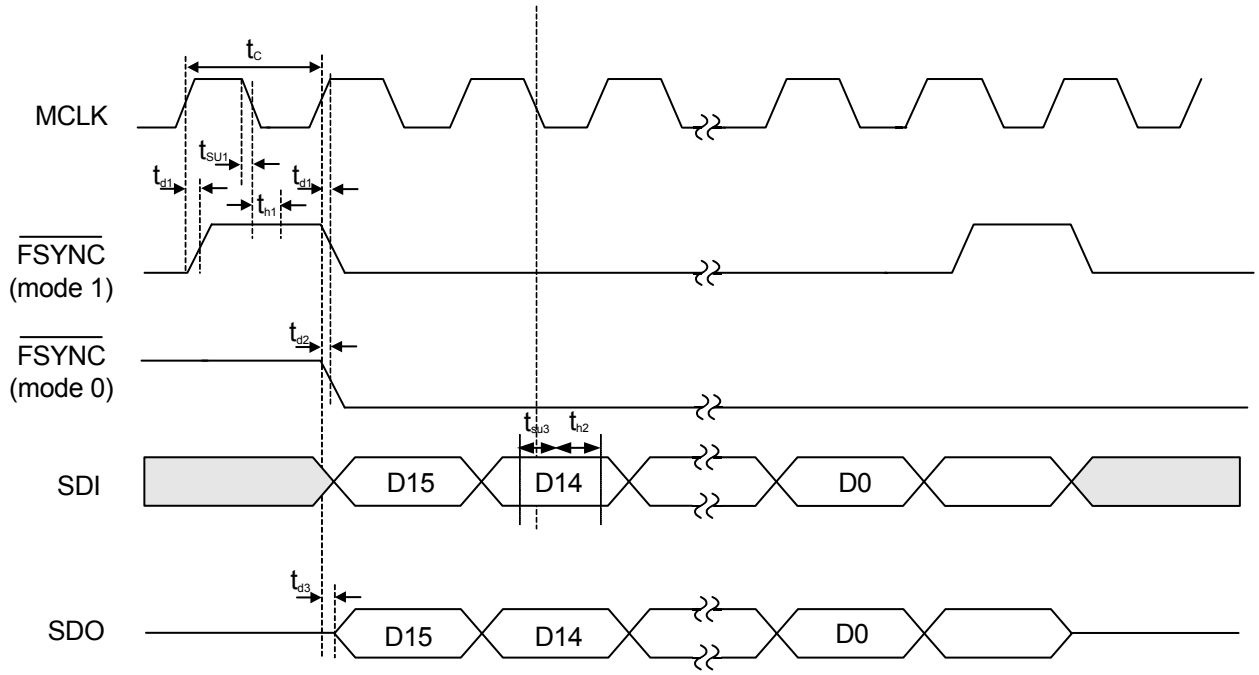


Figure 6. Serial Interface Timing Diagram (Slave Mode, DCE = 1, FSD = 1)

Table 11. Digital FIR Filter Characteristics—Transmit and Receive
(V_D = 3.0 to 3.6 V, Sample Rate = 8 kHz, T_A = 70 °C for K-Grade)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (0.1 dB)	$F_{(0.1\ dB)}$	0	—	3.3	kHz
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.1	—	0.1	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–74	—	—	dB
Group Delay	t_{gd}	—	12/Fs	—	s
Note: Typical FIR filter characteristics for Fs = 8000 Hz are shown in Figures 7, 8, 9, and 10.					

Table 12. Digital IIR Filter Characteristics—Transmit and Receive
(V_D = 3.0 to 3.6 V, Sample Rate = 8 kHz, T_A = 70 °C for K-Grade)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.2	—	0.2	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–40	—	—	dB
Group Delay	t_{gd}	—	1.6/Fs	—	s
Note: Typical IIR filter characteristics for Fs = 8000 Hz are shown in Figures 11, 12, 13, and 14. Figures 15 and 16 show group delay versus input frequency.					

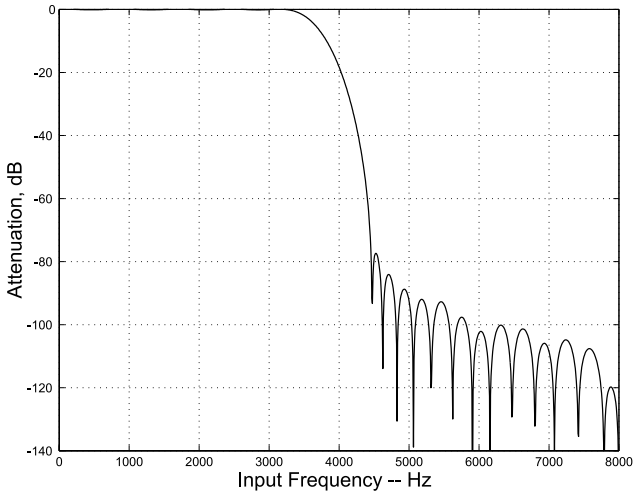


Figure 7. FIR Receive Filter Response

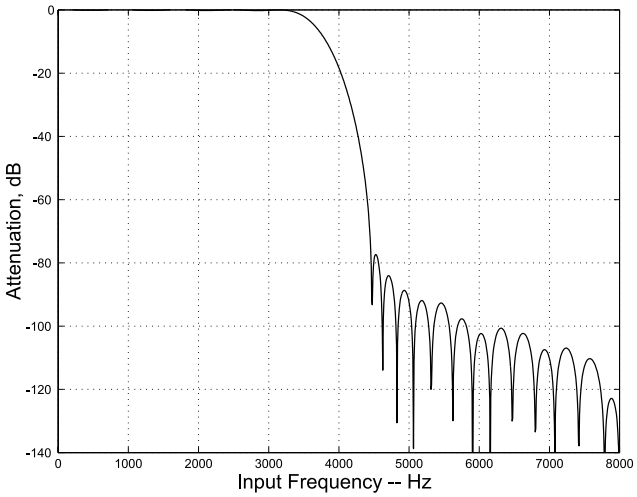


Figure 9. FIR Transmit Filter Response

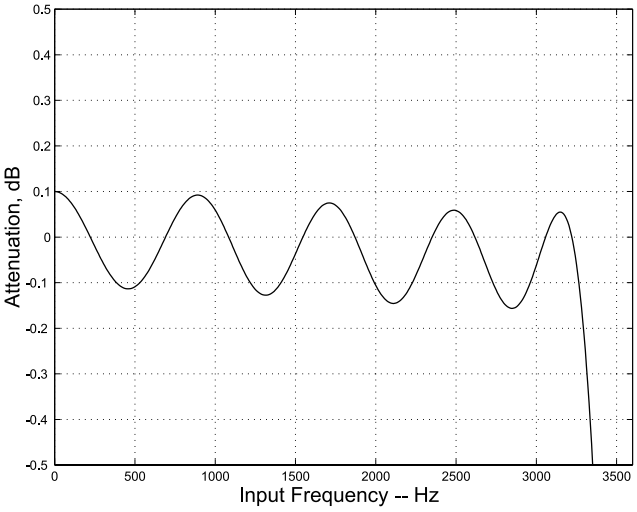


Figure 8. FIR Receive Filter Passband Ripple

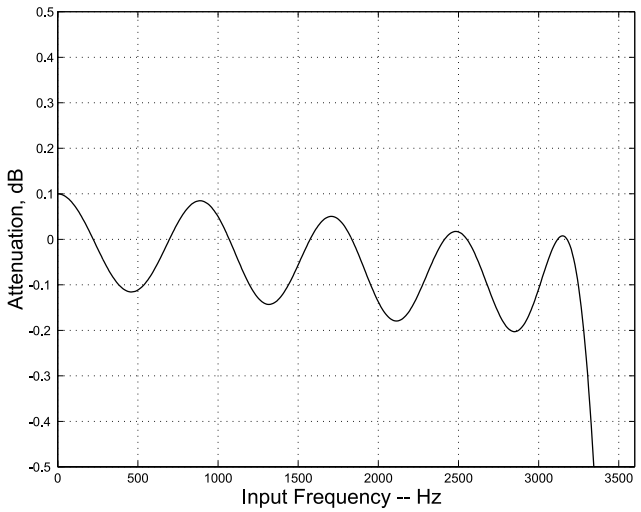


Figure 10. FIR Transmit Filter Passband Ripple

For Figures 7–10, all filter plots apply to a sample rate of Fs = 8 kHz.

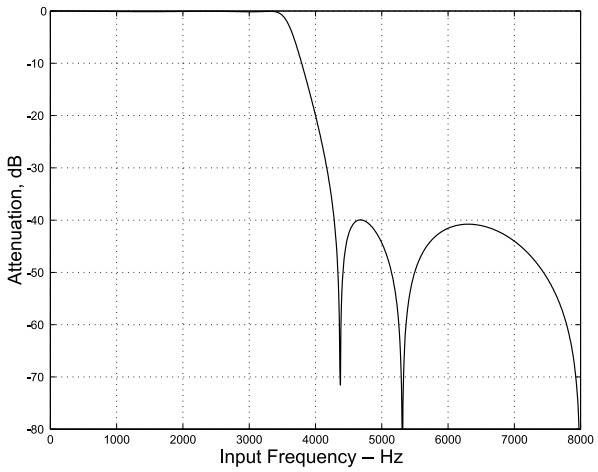


Figure 11. IIR Receive Filter Response

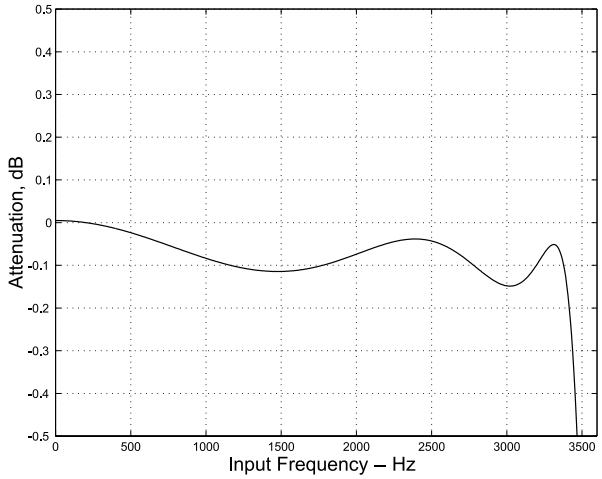


Figure 12. IIR Receive Filter Passband Ripple

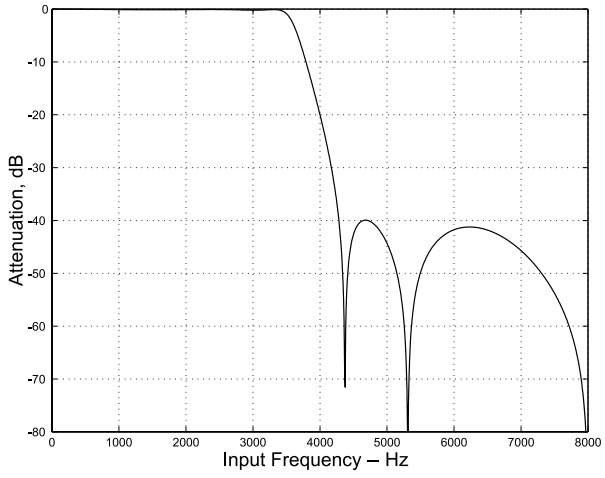


Figure 13. IIR Transmit Filter Response

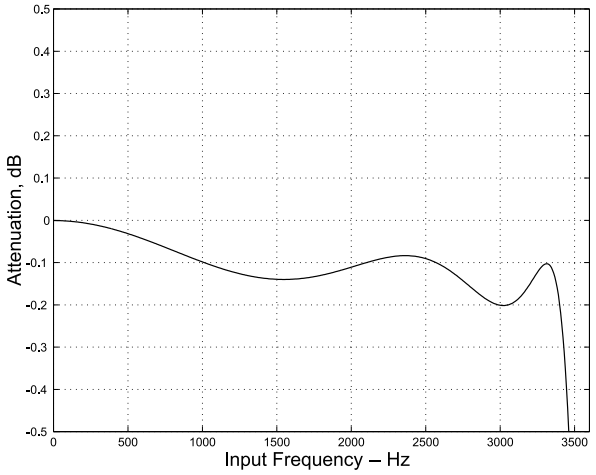


Figure 14. IIR Transmit Filter Passband Ripple

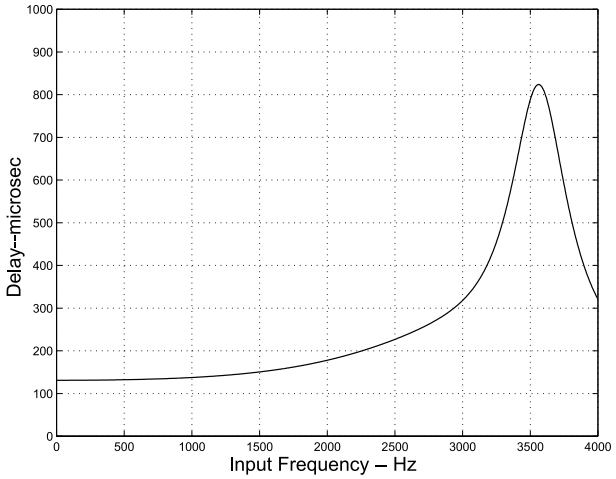


Figure 15. IIR Receive Group Delay

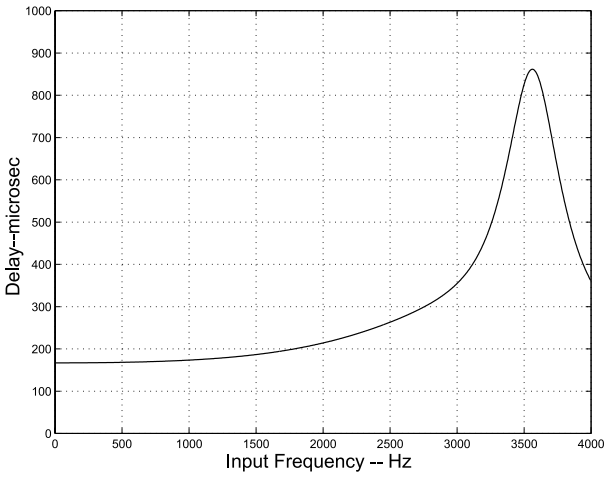


Figure 16. IIR Transmit Group Delay

2. Typical Application Schematic

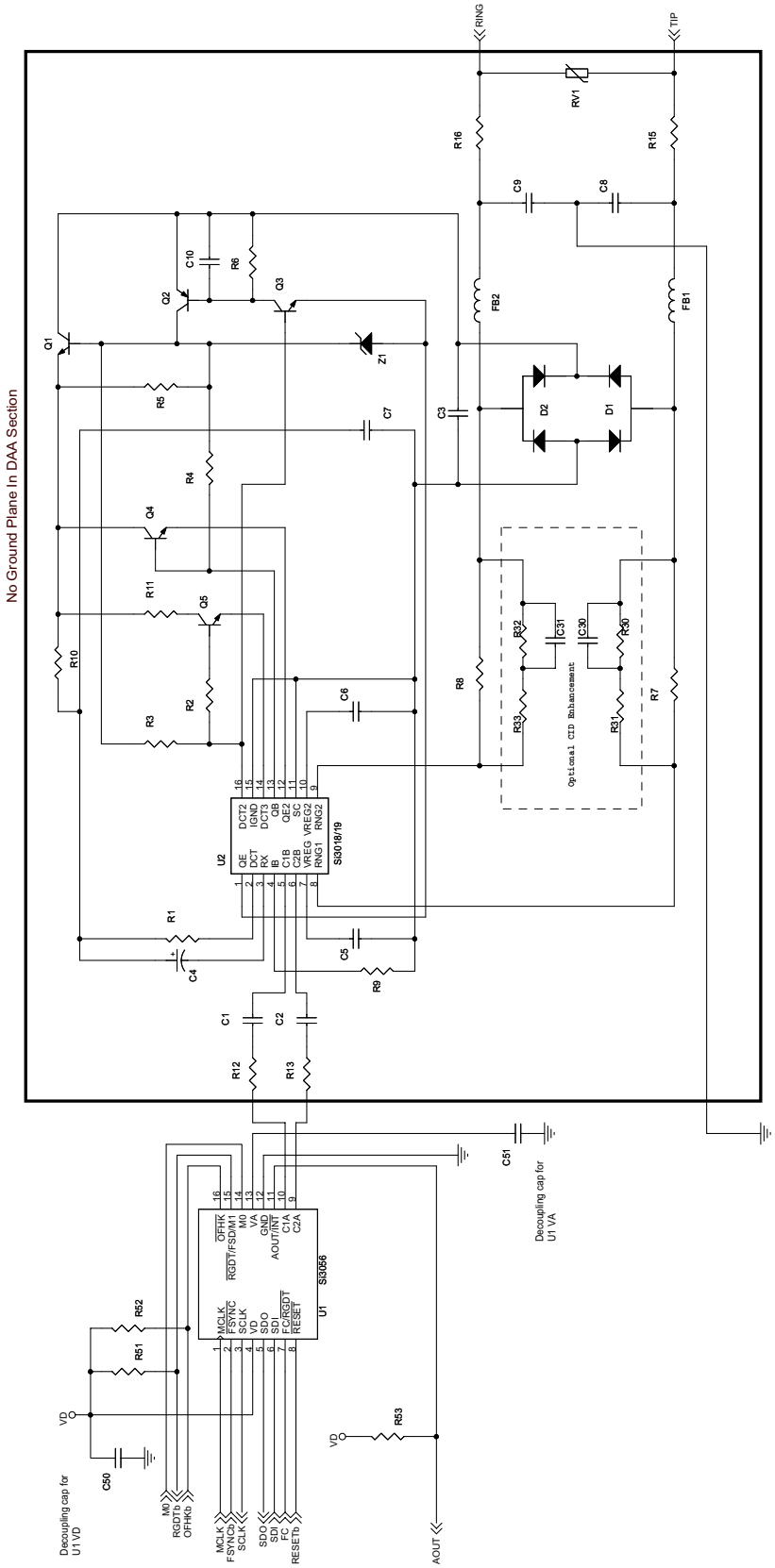


Figure 17. Typical Application Circuit for the Si3056 and Si3018/19/10 (Refer to AN67 for recommended layout guidelines)

3. Bill of Materials

Component(s)	Value	Supplier(s)
C1, C2	33 pF, Y2, X7R, ±20%	Panasonic, Murata, Vishay
C3[1]	10 nF, 250 V, X7R, ±10%	Venkel, SMEC
C4	1.0 uF, 50 V, Elec/Tant, ±20%	Panasonic
C5, C6, C50, C51	0.1 uF, 16V, X7R, ±20%	Venkel, SMEC
C7	2.7 nF, 50V, X7R, 20%	Venkel, SMEC
C8, C9	680 pF, Y2, X7R, ±10%	Panasonic, Murata, Vishay
C10	0.01 uF, 16 V, X7R, ±20%	Venkel, SMEC
C30, C31[3]	Not installed, 120 pF, 250V, X7R, ±10%	Venkel, SMEC
D1, D2[2]	Dual Diode, 225 mA, 300 V, CMPD2004S	Central Semiconductor
FB1, FB2	Ferrite Bead, BLM18AG601SN1B	Murata
Q1, Q3	NPN, 300 V, MMBTA42	OnSemi, Fairchild
Q2	PNP, 300 V, MMBTA92	OnSemi, Fairchild
Q4, Q5	NPN, 60 V, 330 mW, MMBT2484	OnSemi, Fairchild
RV1	Sidactor, 275 V, 100 A	Teccor, Protek, ST Micro
R1	1.07 kohm, 1/2 W, 1%	Venkel, SMEC, Panasonic
R2	150 ohm, 1/16 W, 5%	Venkel, SMEC, Panasonic
R3	3.65 kohm, 1/2 W, 1%	Venkel, SMEC, Panasonic
R4	2.49 kohm, 1/2 W, 1%	Venkel, SMEC, Panasonic
R5, R6	100 kohm, 1/16 W, 5%	Venkel, SMEC, Panasonic
R7, R8[3]	20 Mohm, 1/16 W, 5%	Venkel, SMEC, Panasonic
R9	1 Mohm, 1/16 W, 1%	Venkel, SMEC, Panasonic
R10	536 ohm, 1/4 W, 1%	Venkel, SMEC, Panasonic
R11	73.2 ohm, 1/2 W, 1%	Venkel, SMEC, Panasonic
R12, R13	56.2 ohm, 1/16 W, 1%	Venkel, SMEC, Panasonic
R15, R16[4]	0 ohm, 1/16 W	Venkel, SMEC, Panasonic
R30, R32[3]	Not installed, 15 Mohm,, 1/8 W, 5%	Venkel, SMEC, Panasonic
R31, R33[3]	Not installed, 5.1 Mohm,, 1/8 W, 5%	Venkel, SMEC, Panasonic
R51, R52	4.7 kohm,, 1/10 W, 5%	Venkel, SMEC, Panasonic
U1	Si3056	Silicon Labs
U2	Si3018/19/10	Silicon Labs
Z1	Zener Diode, 43 V, 1/2 W, ZMM43	General Semiconductor

1. Value for C3 above is recommended for use with the Si3018. In voice appliations, a C3 value of 3.9 nF (250 V, X7R, 20%) is recommended to improve return loss performance
2. Several diode bridge configurations are acceptable, parts such as a single DF-04S or four 1N4004 diodes may be used (suppliers include General Semiconductor, Diodes Inc., etc.)
3. C30-31 and R30-33 can be substitued for R7-8 to implent the enhanced caller ID circuit.
4. Murata BLM18AG601SN1B may be substituted for R15-R16 (0 ohm) to decrease emissions.

4. AOUT PWM Output

Figure 18 illustrates an optional circuit to support the pulse width modulation (PWM) output capability of the Si3056 for call progress monitoring purposes. Set the PWME bit (Register 1, bit 3) to enable this mode.

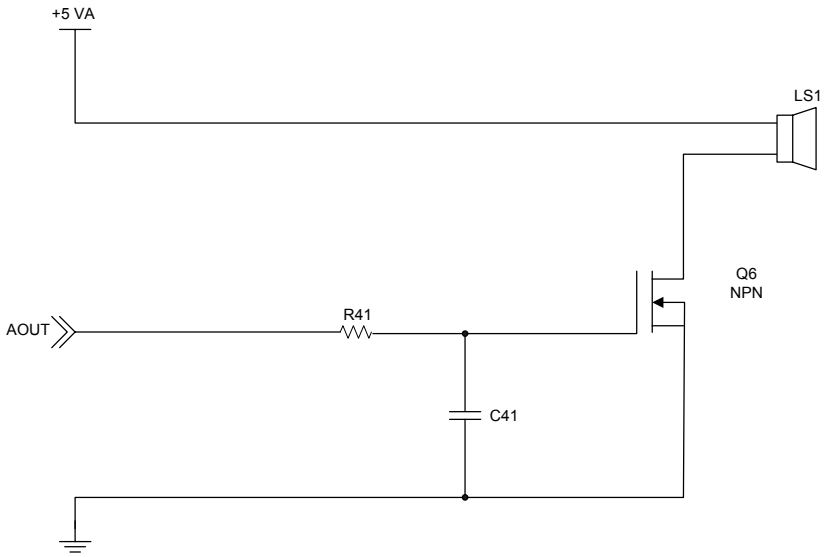


Figure 18. AOUT PWM Circuit for Call Progress

Table 13. Component Values—AOUT PWM

Component	Value	Supplier
LS1	Speaker BRT1209PF-06	Intervox
Q6	NPN KSP13	Fairchild
C41	0.1 µF, 16 V, X7R, ±20%	Venkel, SMEC
R41	150 Ω, 1/16 W, ±5%	Venkel, SMEC, Panasonic

Registers 20 and 21 allow the receive and transmit paths to be attenuated linearly. When these registers are set to all 1s, the receive and transmit paths are muted. These registers affect the call progress output only and do not affect transmit and receive operations on the telephone line.

The PWMM[1:0] bits (Register 1, bits 5:4) select one of the three different PWM output modes for the AOUT signal, including a delta-sigma data stream, a conventional 32 kHz return to zero PWM output, and balanced 32 kHz PWM output.

5. Functional Description

The Si3056 is an integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line interface requirements. The Si3056 implements Silicon Laboratories® patented isolation technology and offers the highest level of integration by replacing an analog front end (AFE), an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid with two 16-pin packages (SOIC or TSSOP).

The Si3056 DAA is software programmable to meet global requirements and is compliant with FCC, TBR21, JATE, and other country-specific PTT specifications as shown in Table 16 on page 26. In addition, the Si3056 meets the most stringent worldwide requirements for out-of-band energy, emissions, immunity, high-voltage surges, and safety, including FCC Part 15 and 68, EN55022, EN55024, and many other standards.

5.1. Upgrading from the Si3034/35/44 to Si3056

The Si3056 offers Silicon Laboratories® customers currently using Si3034/35/44 standard serial interface DAA chipsets with an upgrade path for use in new designs. The Si3056 digital interface is similar to the Si3034/35/44 DAAs, thus the Si3056 retains the ability to connect to many widely available DSPs. This also allows customers to leverage software developed for existing Si3034/35/44 designs. More importantly, the Si3056 also offers a number of new features not provided in the Si3034/35/44 DAAs. An overview of the feature differences between the Si3044 and the Si3056 is presented in Table 14. Finally, the globally-compliant Si3056 can be implemented with roughly half the external components required in the already highly integrated Si3034/35/44 DAA application circuits. The following items have changed in the Si3056 as compared to the Si3034/35/44 DAAs:

- The pinout, the application circuit, and the bill of materials. The Si3056 is not pin compatible with Si3034/35/44 DAA chipsets.
- New features have been added to the Si3056 including more ac terminations, a programmable hybrid, finer gain/attenuation step resolution, finer resolution loop current monitoring capability, ring validation, more HW interrupts, a 200 Hz low frequency filter pole. (See the appropriate functional descriptions.)
- The secondary communication data format (see "5.26.Digital Interface" on page 37).
- The low-power sleep mode, and system requirements to support wake-on-ring. (See "5.28.Power Management" on page 39.)

5.2. Line-Side Device Support

Three different line-side devices can be used with the Si3056 system-side device:

- Globally-compliant line-side device—Targets global DAA requirements. Use the Si3018 global line-side device for this configuration. This line-side device supports both FCC-compliant countries and non-FCC-compliant countries.
- Globally-compliant, enhanced features line-side device—Targets embedded and voice applications with global DAA requirements. Use the Si3019 line-side device for this configuration. The Si3019 contains all the features available on the Si3018, plus the following additional features/enhancements:
  - Sixteen selectable ac terminations to increase return loss and trans-hybrid loss performance.
  - Higher transmit and receive level mode.
  - Selectable 200 Hz low frequency pole.
  - –16 to 13.5 dB digital gain/attenuation adjustment in 0.1 dB increments for the transmit and receive paths.
  - Programmable line current/voltage threshold interrupt.
- Globally-compliant, low-speed only line-side device—Targets embedded 2400 bps soft modem applications. Use the Si3010 line-side device for this configuration. The Si3010 contains all the features available on the Si3018, except the transmit and receive paths are optimized and tested only for modem connect rates up to 2400 bps.

Table 14. New Si3056 Features

Chipset	**Si3044**	**Si3056**		
System-Side Part #	**Si3021**			
Line-Side Part #	**Si3015**	**Si3010**	**Si3018**	**Si3019**
Global DAA	Yes	Yes	Yes	Yes
Digital Interface	SSI	SSI	SSI	SSI
Power Supply	3.3 V or 5 V	3.3 V	3.3 V	3.3 V
Max Modem Connect Rate	56 kbps	2400 bps	56 kbps	56 kbps
Data Bus Width	16-bit	16-bit	16-bit	16-bit
Control Register Addressing	6-bit	8-bit	8-bit	8-bit
Max Sampling Frequency	11.025 kHz	16 kHz	16 kHz	16 kHz
AC Terminations	2	4	4	16
Programmable Gain	3 dB steps	3 dB steps	3 dB steps	0.1 dB steps
Loop Current Monitoring	3 mA/bit	1.1 mA/bit	1.1 mA/bit	1.1 mA/bit
Line Voltage Monitoring	2.75 V per bit	1 V per bit	1 V per bit	1 V per bit
Polarity Reversal Detection	Yes (SW polling)	Yes (HW interrupt)	Yes (HW interrupt)	Yes (HW interrupt)
Line I/V Threshold Detection	No	No	No	Yes
Ring Qualification	No	Yes	Yes	Yes
Wake-on-Ring Support	Yes	Yes (MCLK active)	Yes (MCLK active)	Yes (MCLK active)
HW Interrupts	Ring detect only	7 HW interrupts	7 HW interrupts	8 HW interrupts
Integrated Fixed Analog Hybrid	Yes	Yes	Yes	Yes
Programmable Digital Hybrid	No	Yes	Yes	Yes
Full Scale Transmit/Receive Level	+3.2 dBm	0 dBm	0 dBm	+3.2 dBm

Table 15. Country Specific Register Settings

Register	16	31	16	16	26	26	26	30[2]	16[3]	
Country	OHS	OHS2	RZ	RT	ILIM	DCV[1:0]	MINI[1:0]	ACIM[3:0]	ACT	ACT2
Argentina	0	0	0	0	0	11	00	0000	0	0
Australia[4]	1	0	0	0	0	01	01	0011	0	1
Austria	0	1	0	0	1	11	00	0010	0	1
Bahrain	0	1	0	0	1	11	00	0010	0	1
Belgium	0	1	0	0	1	11	00	0010	0	1
Brazil	0	0	0	0	0	11	00	0000	0	0
Bulgaria	0	1	0	0	1	11	00	0011	0	1
Canada	0	0	0	0	0	11	00	0000	0	0
Chile	0	0	0	0	0	11	00	0000	0	0
China[5]	0	0	0	0	0	11	00	0000/1010	0	0
Colombia	0	0	0	0	0	11	00	0000	0	0
Croatia	0	1	0	0	1	11	00	0010	0	1
Cyprus	0	1	0	0	1	11	00	0010	0	1
Czech Republic	0	1	0	0	1	11	00	0010	0	1
Denmark	0	1	0	0	1	11	00	0010	0	1
Ecuador	0	0	0	0	0	11	00	0000	0	0
Egypt	0	1	0	0	1	11	00	0010	0	1
El Salvador	0	0	0	0	0	11	00	0000	0	0
Finland	0	1	0	0	1	11	00	0010	0	1
France	0	1	0	0	1	11	00	0010	0	1
Germany	0	1	0	0	1	11	00	0010	0	1
Greece	0	1	0	0	1	11	00	0010	0	1
Guam	0	0	0	0	0	11	00	0000	0	0
Hong Kong	0	0	0	0	0	11	00	0000	0	0
Hungary	0	1	0	0	1	11	00	0010	0	1
Iceland	0	1	0	0	1	11	00	0010	0	1
India	0	0	0	0	0	11	00	0000	0	0
Indonesia	0	0	0	0	0	11	00	0000	0	0
Ireland	0	1	0	0	1	11	00	0010	0	1
Israel	0	1	0	0	1	11	00	0010	0	1
Italy	0	1	0	0	1	11	00	0010	0	1
Japan	0	0	0	0	0	01	01	0000	0	0
Jordan	0	0	0	0	0	01	01	0000	0	0
Kazakhstan	0	0	0	0	0	11	00	0000	0	0
Kuwait	0	0	0	0	0	11	00	0000	0	0
Latvia	0	1	0	0	1	11	00	0010	0	1
Lebanon	0	1	0	0	1	11	00	0010	0	1

Note:

1. Supported for loop current ≥ 20 mA.
2. Available with Si3019 line-side only.
3. Available with Si3018 line-side only.
4. See "5.11.DC Termination" on page 27 for DCV and MINI settings.
5. ACIM is 0000 for data applications and 1010 for voice applications.

Table 15. Country Specific Register Settings (Continued)

Register	16	31	16	16	26	26	26	30[2]	16[3]	
Country	OHS	OHS2	RZ	RT	ILIM	DCV[1:0]	MINI[1:0]	ACIM[3:0]	ACT	ACT2
Luxembourg	0	1	0	0	1	11	00	0010	0	1
Macao	0	0	0	0	0	11	00	0000	0	0
Malaysia[1]	0	0	0	0	0	01	01	0000	0	0
Malta	0	1	0	0	1	11	00	0010	0	1
Mexico	0	0	0	0	0	11	00	0000	0	0
Morocco	0	1	0	0	1	11	00	0010	0	1
Netherlands	0	1	0	0	1	11	00	0010	0	1
New Zealand	0	0	0	0	0	11	00	0100	1	1
Nigeria	0	1	0	0	1	11	00	0010	0	1
Norway	0	1	0	0	1	11	00	0010	0	1
Oman	0	0	0	0	0	01	01	0000	0	0
Pakistan	0	0	0	0	0	01	01	0000	0	0
Peru	0	0	0	0	0	11	00	0000	0	0
Philippines	0	0	0	0	0	01	01	0000	0	0
Poland	0	1	0	0	1	11	00	0010	0	1
Portugal	0	1	0	0	1	11	00	0010	0	1
Romania	0	1	0	0	1	11	00	0010	0	1
Russia	0	0	0	0	0	11	00	0000	0	0
Saudi Arabia	0	0	0	0	0	11	00	0000	0	0
Singapore	0	0	0	0	0	11	00	0000	0	0
Slovakia	0	1	0	0	1	11	00	0010	0	1
Slovenia	0	1	0	0	1	11	00	0010	0	1
South Africa	0	0	1	0	0	11	00	0011	1	0
South Korea	0	0	1	0	0	11	00	0000	0	0
Spain	0	1	0	0	1	11	00	0010	0	1
Sweden	0	1	0	0	1	11	00	0010	0	1
Switzerland	0	1	0	0	1	11	00	0010	0	1
Taiwan	0	0	0	0	0	11	00	0000	0	0
TBR21	0	0	0	0	1	11	00	0010	0	1
Thailand	0	0	0	0	0	01	01	0000	0	0
UAE	0	0	0	0	0	11	00	0000	0	0
United Kingdom	0	1	0	0	1	11	00	0101	0	1
USA	0	0	0	0	0	11	00	0000	0	0
Yemen	0	0	0	0	0	11	00	0000	0	0

Note:
1. Supported for loop current ≥ 20 mA.
2. Available with Si3019 line-side only.
3. Available with Si3018 line-side only.
4. See "5.11.DC Termination" on page 27 for DCV and MINI settings.
5. ACIM is 0000 for data applications and 1010 for voice applications.

5.3. Power Supplies

The Si3056 system-side device operates from a 3.0–3.6 V power supply. The Si3056 input pins are 5 V tolerant. The Si3056 output pins only drive 3.3 V. The line-side device derives its power from two sources: The Si3056 and the telephone line. The Si3056 supplies power over the patented isolation link between the two devices, allowing the line-side device to communicate with the Si3056 while on-hook and perform other on-hook functions such as line voltage monitoring. When off-hook, the line-side device also derives power from the line current supplied from the telephone line. This feature is exclusive to DAAs from Silicon Laboratories® and allows the most cost-effective implementation for a DAA while still maintaining robust performance over all line conditions.

5.4. Initialization

When the Si3056 is powered up, assert the $\overline{\text{RESET}}$ pin. When the $\overline{\text{RESET}}$ pin is deasserted, the registers have default values. This reset condition guarantees the line-side device is powered down without the possibility of loading the line (i.e., off-hook). An example initialization procedure is outlined in the following list:

1. Program the PLL with registers 8 and 9 (N[7:0], M[7:0]) to the appropriate divider ratios for the supplied MCLK frequency and the sample rate in register 7 (SRC), as defined in "5.25.Clock Generation" on page 36.
2. Wait 1 ms until the PLL is locked.
3. Write a 00H into Register 6 to power up the line-side device.
4. Set the required line interface parameters (i.e., DCV[1:0], MINI[1:0], ILIM, DCR, ACT and ACT2 or ACIM[3:0], OHS, RT, RZ, ATX[2:0] or TGA2 and TXG2) as defined by “Country Specific Register Settings” shown in Table 15.

When this procedure is complete, the Si3056 is ready for ring detection and off-hook.

5.5. Isolation Barrier

The Si3056 achieves an isolation barrier through low-cost, high-voltage capacitors in conjunction with Silicon Laboratories® proprietary signal processing techniques. These techniques eliminate signal degradation from capacitor mismatches, common mode interference, or noise coupling. As shown in Figure 17 on page 18, the C1, C2, C8, and C9 capacitors isolate the Si3056 (system-side) from the line-side device. Transmit, receive, control, ring detect, and caller ID data are passed across this barrier. Y2 class capacitors can be used to achieve surge performance of 5 kV or greater.

The capacitive communications link is disabled by default. To enable it, the PDL bit (Register 6, bit 4) must be cleared. No communication between the system-side and line-side can occur until this bit is cleared. The clock generator must be programmed to an acceptable sample rate before clearing the PDL bit.

5.6. Transmit/Receive Full Scale Level (Si3019 Line-Side Only)

The Si3056 supports programmable maximum transmit and receive levels. The default signal level supported by the Si3056 is 0 dBm into a 600 Ω load. Two additional modes of operation offer increased transmit and receive level capability to enable use of the DAA in applications that require higher signal levels. The full scale mode is enabled by setting the FULL bit in Register 31. With FULL = 1, the full scale signal level increases to +3.2 dBm into a 600 Ω load, or 1 dBV into all reference impedances. The enhanced full scale mode (or 2X full scale) is enabled by setting the FULL2 bit in Register 30. Will FULL2 = 1, the full scale signal level increases to +6.0 dBm into a 600 Ω load, or 1.5 dBV into all reference impedances. The full scale and enhanced full scale modes provide the ability to trade off TX power and TX distortion for a peak signal. By using the programmable digital gain registers in conjunction with the enhanced full scale signal level mode, a specific power level (+3.2 dBm for example) could be achieved across all ACT settings.

5.7. Parallel Handset Detection

The Si3056 can detect a parallel handset going off-hook. When the Si3056 is off-hook, the loop current can be monitored with the LCS bits. A significant drop in loop current signals that a parallel handset is going off-hook. If a parallel handset causes the LCS bits to read all 0s, the Drop-Out Detect (DOD) bit can be checked to verify a valid line exists.

The LVS bits can be read to determine the line voltage when on-hook and off-hook. Significant drops in line voltage can signal a parallel handset. For the Si3056 to operate in parallel with another handset, the parallel handset must have a sufficiently high dc termination to support two off-hook DAAs on the same line. Improved parallel handset operation can be achieved by changing the dc impedance from 50 to 800 Ω and reducing the DCT pin voltage with the DVC[1:0] bits.

5.8. Line Voltage/Loop Current Sensing

The Si3056 can measure loop current and line voltage with the Si3010, Si3018, and the Si3019 line-side devices. The 8-bit LCS2[7:0] and LCS[4:0] registers report loop current. The 8-bit LVS[7:0] register reports line voltage.

These registers can help determine the following:

- When on-hook, detect if a line is connected.
- When on-hook, detect if a parallel phone is off-hook.
- When off-hook, detect if a parallel phone goes on or off-hook.
- Detect if enough loop current is available to operate.
- When used in conjunction with the OPD bit, detect if an overcurrent condition exists. (See "5.22.Overload Detection" on page 35.)

5.8.1. Line Voltage Measurement

The Si3056 device reports line voltage with the LVS[7:0] bits (Register 29) in both on- and off-hook states with a resolution of 1 V per bit. The accuracy of these bits is approximately ±10%. Bits 0 through 6 of this register indicate the value of the line voltage in 2s compliment format. Bit 7 of this register indicates the polarity of the tip/ring voltage.

If the INTE bit (Register 2) and the POLM bit (Register 3) are set, a hardware interrupt is generated on the AOUT/INT pin when bit 7 of the LVS register changes state. The edge-triggered interrupt is cleared by writing 0 to the POLI bit (Register 4). The POLI bit is set each time bit 7 of the LVS register changes state and must be written to 0 to clear it.

The default state of the LVS register forces the LVS bits to 0 when the line voltage is 3 V or less. The LVFD bit (Register 31, bit 0) disables the force-to-zero function and allows the LVS register to display non-zero values of 3 V and below. This register might display unpredictable values at line voltages between 0 to 2 V. At 0 V, the LVS register displays all 0s.

5.8.2. Loop Current Measurement

When the Si3056 is off-hook, the LCS2[7:0] and LCS[4:0] bits measure loop current in 1.1 mA/bit and 3.3 mA/bit resolution respectively. These bits enable detection of another phone going off-hook by monitoring the dc loop current. The LCS bits are decoded from LCS2; so, both are available at the same time. The line current sense transfer function is shown in Figure 19 and detailed in Table 16. The LCS and LCS2 bits report loop current down to the minimum operating loop current for the DAA. Below this threshold, the reported value of loop current is unpredictable.

Table 16. Loop Current Transfer Function

LCS[4:0]	Condition
00000	Insufficient line current for normal operation. Use the DOD bit (Register 19, bit 1) to determine if a line is connected.
00100	Minimum line current for normal operation.
11111	Loop current is greater than 127 mA. An overcurrent situation may exist.

5.9. Off-Hook

The communication system generates an off-hook command by applying a logic 0 to the OFHK pin or by setting the OH bit (Register 5, bit 0).The OFHK pin must be enabled by setting the OHE bit (Register 5, bit 1). The polarity of the OFHK pin is selected by the OPOL bit (Register 5, bit 4). With OFHK asserted, the system is in an off-hook state.

The off-hook state seizes the line for incoming/outgoing calls and also can be used for pulse dialing. With OFHK deasserted, negligible dc current flows through the hookswitch. When the OFHK pin is asserted, the hookswitch transistor pair, Q1 and Q2, turn on. This applies a termination impedance across TIP and RING and causes dc loop current to flow. The termination impedance has an ac and dc component.

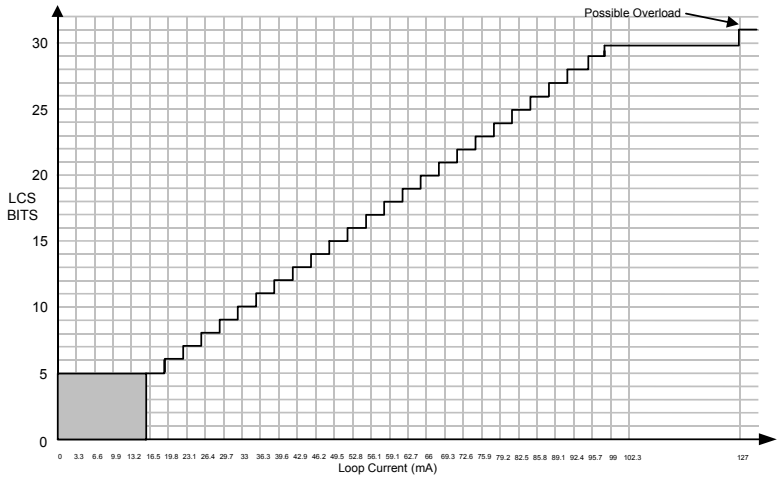


Figure 19. Typical Loop Current LCS Transfer Function

Several events occur in the DAA when the $\overline{OFHK}$ pin is asserted or the OH bit is set. There is a 250 μs latency to allow the off-hook command to be communicated to the line-side device. Once the line-side device goes off-hook, an off-hook counter forces a delay for line transients to settle before transmission or reception occurs. This off-hook counter time is controlled by the FOH[1:0] bits (Register 31, bits 6:5). The default setting for the off-hook counter time is 128 ms, but can be adjusted up to 512 ms or down to either 64 or 8 ms.

After the off-hook counter has expired, a resistor calibration is performed for 17 ms. This allows circuitry internal to the DAA to adjust to the exact conditions present at the time of going off-hook. This resistor calibration can be disabled by setting the RCALD bit (Register 25, bit 5).

After the resistor calibration is performed, an ADC calibration is performed for 256 ms. This calibration helps to remove offset in the A/D sampling the telephone line. This ADC calibration can be disabled by setting the CALD bit (Register 17, bit 5). See “5.29.Calibration” on page 39. for more information on automatic and manual calibration.

Silicon Laboratories® recommends that the resistor and the ADC calibrations not be disabled except when a fast response is needed after going off-hook, such as when responding to a Type II caller-ID signal. See “5.21.Caller ID” on page 32.

To calculate the total time required to go off-hook and start transmission or reception, the digital filter delay (typically 1.5 ms with the FIR filter) should be included in the calculation.

5.10. Interrupts

The AOUT/$\overline{INT}$ pin can be used as a hardware interrupt pin by setting the INTE bit (Register 2, bit 7). When this bit is set, the call progress output function (AOUT) is not available. The default state of this interrupt output pin is active low, but active high operation can be enabled by setting the INTP bit (Register 2, bit 6). This pin is an open-drain output when the INTE bit is set, and requires a 4.7 kΩ pullup or pulldown for correct operation. If multiple $\overline{INT}$ pins are connected to a single input, the combined pullup or pulldown resistance should equal 4.7 kΩ. Bits 7–2, and 0 in Register 3 and bit 1 in Register 44 can be set to enable hardware interrupt sources. When one or more of these bits are set, the AOUT/$\overline{INT}$ pin becomes active and stays active until the interrupts are serviced. If more than one hardware interrupt is enabled in Register 3, software polling determines the cause of the interrupts. Register 4 and bit 3 of Register 44 contain sticky interrupt flag bits. Clear these bits after being set to service the interrupt.

Registers 43 and 44 contain the line current/voltage threshold interrupt. This interrupt will trigger when either the measured line voltage or current in the LVS or LCS2 registers, as selected by the CVS bit (Register 44, bit 2), crosses the threshold programmed into the CVT[7:0] bits. An interrupt can be programmed to occur when the measured value rises above or falls below the threshold. Only the magnitude of the measured value is used to compare to the threshold programmed into the CVT[7:0] bits, and thus only positive numbers should be used as a threshold. This line current/voltage threshold interrupt is only available with the Si3019 line-side device.

5.11. DC Termination

The DAA has programmable settings for dc impedance, minimum operational loop current, and TIP/RING voltage. The dc impedance of the DAA is normally represented with a 50 Ω slope as shown in Figure 20, but can be changed to an 800 Ω slope by setting the DCR bit. This higher dc termination presents a higher resistance to the line as loop current increases.

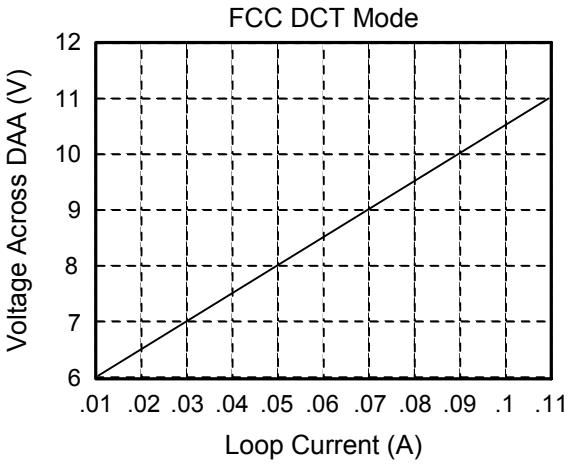


Figure 20. FCC Mode I/V Characteristics, DCV[1:0] = 11, MINI[1:0] = 00, ILIM = 0

For applications that require current limiting per the TBR21 standard, the ILIM bit can be set to select this mode. In the current limiting mode, the dc I/V curve is changed to a 2000 Ω slope above 40 mA, as shown in Figure 21. The DAA operates with a 50 V, 230 Ω feed, which is the maximum line feed specified in the TBR21 standard.

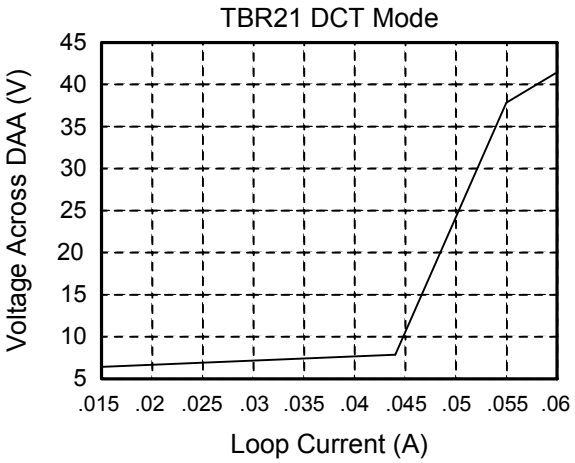


Figure 21. TBR21 Mode I/V Characteristics, DCV[1:0] = 11, MINI[1:0] = 00, ILIM = 1

The MINI[1:0] bits select the minimum operational loop current for the DAA, and the DCV[1:0] bits adjust the DCT pin voltage, which affects the TIP/RING voltage of the DAA. These bits permit important trade-offs for the system designer. Increasing the TIP/RING voltage provides more signal headroom, while decreasing the TIP/RING voltage allows compliance to PTT standards in low-voltage countries such as Japan. Increasing the minimum operational loop current above 10 mA also increases signal headroom and prevents degradation of the signal level in low-voltage countries.

Finally, Australia has separate dc termination requirements for line seizure versus line hold. Japan mode may be used to satisfy both requirements. However, if a higher transmit level for modem operation is desired, switch to FCC mode 500 ms after the initial off-hook. This satisfies the Australian dc termination requirements.

5.12. AC Termination

The Si3056 has four ac termination impedances with the Si3018 line-side device and sixteen ac termination impedances with the Si3019 line-side device. The ACT and ACT2 bits select the ac impedance on the Si3018 line-side device. The ACIM[3:0] bits select the ac impedance on the Si3019. The available ac termination settings are listed for the line-side devices in Tables 17 and 18.

The most widely used ac terminations are available as register options to satisfy various global PTT requirements. The real 600 Ω impedance satisfies the requirements of FCC part 68, JATE, and many other countries. The 270 Ω+ (750 Ω || 150 nF) satisfies the requirements of TBR21 (ACT = 0, ACT = 1, or ACIM [3:0] = 0010).

Table 17. AC Termination Settings for the Si3010 and Si3018 Line-Side Devices

ACT	ACT2	AC Termination
0	0	Real, nominal 600 Ω termination that satisfies the impedance requirements of FCC part 68, JATE, and other countries.
1	0	Complex impedance that satisfies global impedance requirements.
0	1	Complex impedance that satisfies global impedance requirements EXCEPT New Zealand. Achieves higher return loss for countries requiring complex ac termination. [220 Ω + (820 Ω || 120 nF) and 220 Ω + (820 Ω || 115 nF)]
1	1	Complex impedance for use in New Zealand. [370 Ω + (620 Ω || 310 nF)]

Table 18. AC Termination Settings for the Si3019 Line-Side Device

ACIM[3:0]	AC Termination
0000	600 Ω
0001	900 Ω
0010	270 Ω + (750 Ω || 150 nF) and 275 Ω + (780 Ω || 150 nF)
0011	220 Ω + (820 Ω || 120 nF) and 220 Ω + (820 Ω || 115 nF)
0100	370 Ω + (620 Ω || 310 nF)
0101	320 Ω + (1050 Ω || 230 nF)
0110	370 Ω + (820 Ω || 110 nF)
0111	275 Ω + (780 Ω || 115 nF)
1000	120 Ω + (820 Ω || 110 nF)
1001	350 Ω + (1000 Ω || 210 nF)
1010	200 Ω + (680 Ω || 100 nF)
1011	600 Ω + 2.16 µF
1100	900 Ω + 1 µF
1101	900 Ω + 2.16 µF
1110	600 Ω + 1 µF
1111	Global complex impedance

There are two selections that are useful for satisfying non-standard ac termination requirements. The 350 Ω + (1000 Ω || 210 nF) impedance selection is the ANSI/EIA/TIA 464 compromise impedance network for trunks. The last ac termination selection, ACIM[3:0] = 1111, is designed to satisfy minimum return loss requirements for every country in the world that requires a complex termination. For any of the ac termination settings, the programmable hybrid can be used to further reduce near-end echo. See “5.13.Transhybrid Balance” for more details.

5.13. Transhybrid Balance

The Si3056 contains an on-chip analog hybrid that performs the 2- to 4-wire conversion and near-end echo cancellation. This hybrid circuit is adjusted for each ac termination setting selected.

The Si3056 also offers a digital filter stage for additional near-end echo cancellation. For each ac termination setting selected, the eight programmable hybrid registers (Registers 45-52) can be programmed with coefficients to provide increased cancellation of real-world line anomalies. This digital filter can produce 10 dB or greater of near-end echo cancellation in addition to the echo cancellation provided by the analog hybrid circuitry.

5.14. Ring Detection

The ring signal is resistively coupled from TIP and RING to the RNG1 and RNG2 pins. The Si3056 supports either full- or half-wave ring detection. With full-wave ring detection, the designer can detect a polarity reversal of the ring signal. See “5.21.Caller ID” on page 32. The ring detection threshold is programmable with the RT bit (Register 16, bit 0) and RT2 bit (Register 17, bit 4). The ring detector output can be monitored in three ways. The first method uses the RGDT pin. The second method uses the register bits, RDTP, RDTN, and RDT (Register 5). The final method uses the DTX output.

The ring detector mode is controlled by the RFWE bit (Register 18, bit 1). When the RFWE bit is 0 (default mode), the ring detector operates in half-wave rectifier mode. In this mode, only positive ring signals are detected. A positive ring signal is defined as a voltage greater than the ring threshold across RNG1-RNG2. Conversely, a negative ring signal is defined as a voltage less than the negative ring threshold across RNG1-RNG2. When the RFWE bit is 1, the ring detector operates in full-wave rectifier mode. In this mode, both positive and negative ring signals are detected.

The first method to monitor ring detection output uses the RGDT pin. When the RGDT pin is used, it defaults to active low, but can be changed to active high by setting the RPOL bit (Register 14, bit 1). This pin is a standard CMOS output. If multiple RGDT pins are connected to a single input, the combined pullup or pulldown resistance should equal 4.7 kΩ.

When the RFWE bit is 0, the RGDT pin is asserted when the ring signal is positive, which results in an output signal frequency equal to the actual ring frequency. When the RFWE bit is 1, the RGDT pin is asserted when the ring signal is positive or negative. The output then appears to be twice the frequency of the ring waveform.

The second method to monitor ring detection uses the ring detect bits (RDTP, RDTN, and RDT). The RDTP and RDTN behavior is based on the RNG1-RNG2 voltage. When the signal on RNG1-RNG2 is above the positive ring threshold, the RDTP bit is set. When the signal on RNG1-RNG2 is below the negative ring threshold, the RDTN bit is set. When the signal on RNG1-RNG2 is between these thresholds, neither bit is set.

The RDT behavior is also based on the RNG1-RNG2 voltage. When the RFWE bit is 0, a positive ring signal sets the RDT bit for a period of time. When the RFWE bit is 1, a positive or negative ring signal sets the RDT bit.

The RDT bit acts like a one shot. When a new ring signal is detected, the one shot is reset. If no new ring signals are detected prior to the one shot counter reaching 0, then the RDT bit clears. The length of this count is approximately 5 seconds. The RDT bit is reset to 0 by an off-hook event. If the RDTM bit (Register 3, bit 7) is set, a hardware interrupt occurs on the AOUT/INT pin when RDT is triggered. This interrupt can be cleared by writing to the RDTI bit (Register 4, bit 7). When the RDI bit (Register 2, bit 2) is set, an interrupt occurs on both the beginning and end of the ring pulse. Ring validation may be enabled when using the RDI bit.

The third method to monitor detection uses the DTX data samples to transmit ring data. If the communications link is active (PDL = 0) and the device is not off-hook or in on-hook line monitor mode, the ring data is presented on DTX. The waveform on DTX depends on the state of the RFWE bit.

When RFWE is 0, DTX is –32768 (0x8000) while the RNG1-RNG2 voltage is between the thresholds. When a ring is detected, DTX transitions to +32767 when the ring signal is positive, then goes back to –32768 when the ring is near 0 and negative. Thus a near square wave is presented on DTX that swings from –32768 to +32767 in cadence with the ring signal.

When RFWE is 1, DTX sits at approximately +1228 while the RNG1-RNG2 voltage is between the thresholds. When the ring becomes positive, DTX transitions to +32767. When the ring signal goes near 0, DTX remains near 1228. As the ring becomes negative, the DTX transitions to –32768. This repeats in cadence with the ring signal.

To observe the ring signal on DTX, watch the MSB of the data. The MSB toggles at the same frequency as the ring signal independent of the ring detector mode. This method is adequate for determining the ring frequency.

5.15. Ring Validation

This feature prevents false triggering of a ring detection by validating the ring frequency. Invalid signals, such as a line voltage change when a parallel handset goes off-hook, pulse dialing, or a high-voltage line test are ignored. Ring validation can be enabled during normal operation and in low power sleep mode. The external MCLK signal is required in low power sleep mode for ring validation.

The ring validation circuit operates by calculating the time between alternating crossings of positive and negative ring thresholds to validate that the ring frequency is within tolerance. High and low frequency tolerances are programmable in the RAS[5:0] and RMX[5:0] fields. The RCC[2:0] bits define how long the ring signal must be within tolerance.

Once the duration of the ring frequency is validated by the RCC bits, the circuitry stops checking for frequency tolerance and begins checking for the end of the ring signal, which is defined by a lack of additional threshold crossings for a period of time configured by the RTO[3:0] bits. When the ring frequency is first validated, a timer defined by the RDLY[2:0] bits is started. If the RDLY[2:0] timer expires before the ring timeout, then the ring is validated and a valid ring is indicated. If the ring timeout expires before the RDLY[2:0] timer, a valid ring is not indicated.

Ring validation requires five parameters:

- Timeout parameter to place a lower limit on the frequency of the ring signal on the RAS[5:0] bits (Register 24). This is measured by calculating the time between crossings of positive and negative ring thresholds.
- Minimum count to place an upper limit on the frequency on the RMX[5:0] bits (Register 22).
- Time interval over which the ring signal must be the correct frequency on the RCC[2:0] bits (Register 23).
- Timeout period that defines when the ring pulse has ended based on the most recent ring threshold crossing.
- Delay period between when the ring signal is validated and when a valid ring signal is indicated to accommodate distinctive ringing.

The RNGV bit (Register 24, bit 7) enables or disables the ring validation feature in normal operating mode and low-power sleep mode.

Ring validation affects the behavior of the RDT status bit, the RDTI interrupt, the $\overline{\text{INT}}$ pin, and the $\overline{\text{RGDT}}$ pin.

1. When ring validation is enabled, the status bit seen in the RDT read-only bit (r5.2), represents the detected envelope of the ring. The ring validation parameters are configurable so that this envelope may remain high throughout a distinctive-ring sequence.
2. The RDTI interrupt fires when a validated ring occurs. If RDI is zero (default), the interrupt occurs on the rising edge of RDT. If RDI is set, the interrupt occurs on both rising and falling edges of RDT.
3. The $\overline{\text{INT}}$ pin follows the RDTI bit with configurable polarity.

The RGDT pin can be configured to follow the ringing signal envelope detected by the ring validation circuit by setting RFWE to 0. If RFWE is set to 1, the RGDT pin follows an unqualified ring detect one-shot signal initiated by a ring-threshold crossing and terminated by a fixed counter timeout of approximately 5 seconds. (This information is shown in Register 18).

5.16. Ringer Impedance and Threshold

The ring detector in many DAAs is ac coupled to the line with a large 1 µF, 250 V decoupling capacitor. The ring detector on the Si3056 is resistively coupled to the line. This produces a high ringer impedance to the line of approximately 20 MΩ to meet the majority of country PTT specifications, including FCC and TBR21.

Several countries including Poland, and South Africa, may require a maximum ringer impedance that can be met with an internally synthesized impedance by setting the RZ bit (Register 16, bit 1).

Some countries also specify ringer thresholds differently. The RT bit (Register 16, bit 0) selects between two different ringer thresholds: 15 V ±10% and 21.5 V ±10%. These two settings satisfy ringer threshold requirements worldwide. The thresholds are set so that a ring signal is guaranteed to not be detected below the minimum, and a ring signal is guaranteed to be detected above the maximum.

5.17. Pulse Dialing and Spark Quenching

Pulse dialing results from going off- and on-hook to generate make and break pulses. The nominal rate is 10 pulses per second. Some countries have strict specifications for pulse fidelity that include make and break times, make resistance, and rise and fall times. In a traditional solid-state dc holding circuit, there are many problems in meeting these requirements.

The Si3056 dc holding circuit actively controls the on-hook and off-hook transients to maintain pulse dialing fidelity.

Spark quenching requirements in countries such as Italy, the Netherlands, South Africa, and Australia deal with the on-hook transition during pulse dialing. These tests provide an inductive dc feed resulting in a large voltage spike. This spike is caused by the line inductance and the sudden decrease in current through the loop when going on-hook. The traditional solution to the problem is to put a parallel resistive capacitor (RC) shunt across the hookswitch relay. However, the capacitor required is large (~1 μF, 250 V) and relatively expensive. In the Si3056, loop current can be controlled to achieve three distinct on-hook speeds to pass spark quenching tests without additional BOM components. Through settings of four bits in three registers, OHS (Register 16), OHS2 (Register 31), SQ1 and SQ0 (Register 59), a slow ramp down of loop current can be achieved which induces a delay between the time OH bit is cleared and the time the DAA actually goes on-hook.

To ensure proper operation of the DAA during pulse dialing, disable the automatic resistor calibration that is performed each time the DAA enters the off-hook state by setting the RCALD bit (Register 25, bit 5).

5.18. Billing Tone Protection and Receive Overload

"Billing tones" or "metering pulses" generated by the Central Office can cause modem connection difficulties. The billing tone is typically either a 12 or 16 kHz signal and is sometimes used in Germany, Switzerland, and South Africa. Depending on line conditions, the billing tone might be large enough to cause major errors in the line data. The Si3056 chipset can provide feedback indicating the beginning and end of a billing tone.

Billing tone detection is enabled with the BTE bit (Register 17, bit 2). Billing tones less than 1.1 V_{PK} on the line are filtered out by the low pass digital filter on the Si3056. The ROV bit is set when a line signal is greater than 1.1 V_{PK}, indicating a receive overload condition. The BTD bit is set when a billing tone is large enough to excessively reduce the line-derived power supply of the line-side device.

The OVL bit (Register 19) can be polled following a billing tone detection. The OVL bit indicates that the billing tone has passed when it returns to 0. The BTD and ROV bits are sticky, and must be written to 0 to be reset. After the billing tone passes, the DAA initiates an auto-calibration sequence that must complete before data can be transmitted or received.

Certain line events, such as an off-hook event on a parallel phone or a polarity reversal, can trigger the ROV or the BTD bits. Look for multiple events before qualifying if billing tones are present. After the billing tone passes, the DAA initiates an auto-calibration sequence that must complete before data can be transmitted or received.

Although the DAA remains off-hook during a billing tone event, the received data from the line is corrupted when a large billing tone occurs. If the user wishes to receive data through a billing tone, an external LC filter must be added. A manufacturer can provide this filter to users in the form of a dongle that connects on the phone line before the DAA. This prevents the manufacturer from having to include a costly LC filter to support multiple countries and customers.

Alternatively, when a billing tone is detected, the system software notifies the user that a billing tone has occurred. Notification prompts the user to contact the telephone company to disable billing tones or to purchase an external LC filter.

Disturbance on the line other than billing tones can also cause a receive overload. Some conditions may result in a loop current collapse to a level below the minimum required operating current of the DAA. When this occurs, the dropout detect bit (DOD) is set, and an interrupt will be generated if the dropout detect interrupt mask bit (DODM) is set.

5.19. Billing Tone Filter (Optional)

To operate without degradation during billing tones in Germany, Switzerland, and South Africa, requires an external LC notch filter. The Si3056 can remain off-hook during a billing tone event, but line data is lost in the presence of large billing tone signals. The notch filter design requires two notches, one at 12 kHz and one at 16 kHz. Because these components are expensive and few countries utilize billing tones, this filter is typically placed in an external dongle or added as a population option for these countries. Figure 22 shows an example billing tone filter.

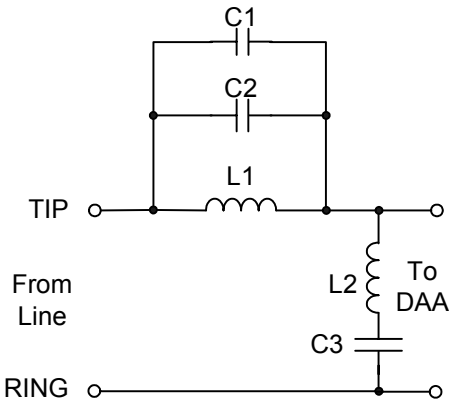


Figure 22. Billing Tone Filter

L1 must carry the entire loop current. The series resistance of the inductors is important to achieve a narrow and deep notch. This design has more than 25 dB of attenuation at both 12 kHz and 16 kHz.

Table 19. Component Values—Optional Billing Tone Filters

Symbol	Value
C1,C2	0.027 µF, 50 V, ±10%
C3	0.01 µF, 250 V, ±10%
L1	3.3 mH, >120 mA, <10 Ω, ±10%
L2	10 mH, >40 mA, <10 Ω, ±10%

The billing tone filter affects the ac termination and return loss. The global complex ac termination (ACIM = 1111) passes global return loss specifications with and without the billing tone filter by at least 3 dB.

5.20. On-Hook Line Monitor

The on-hook line monitor mode allows the Si3056 to receive line activity when in an on-hook state. A low-power ADC located on the line-side device digitizes the signal passed across the RNG1/2 pins and then sends the signal digitally across the communications link to the host. This mode is typically used to detect caller ID data and is enabled by setting the ONHM bit (Register 5, bit 3). Caller ID data can be gained up or attenuated using the receive gain control bits in registers 39 and 41.

5.21. Caller ID

The Si3056 can pass caller ID data from the phone line to a caller ID decoder connected to the serial port.

5.21.1. Type I Caller ID

Type I Caller ID sends the CID data while the phone is on-hook.

In systems where the caller ID data is passed on the phone line between the first and second rings, utilize the following method to capture the caller ID data:

1. After identifying a ring signal using one of the methods described in "5.14.Ring Detection" on page 29, determine when the first ring is complete.
2. Assert the ONHM bit (Register 5, bit 3) to enable caller ID data detection. The caller ID data passed across the RNG 1/2 pins is presented to the host via the SDO pin.
3. Clear the ONHM bit after the caller ID data is received.

In systems where the caller ID data is preceded by a line polarity (battery) reversal, use the following method to capture the caller ID data:

1. Enable full wave rectified ring detection (RFWE, Register 18, bit 1).
2. Monitor the RDTP and RDTN register bits (or the POLI bit) to identify whether a polarity reversal or ring signal has occurred. A polarity reversal trips either the RDTP or RDTN ring detection bits, and thus the full-wave ring detector must be used to distinguish a polarity reversal from a ring. The lowest specified ring frequency is 15 Hz; therefore, if a battery reversal occurs, the DSP should wait a minimum of 40 ms to verify that the event observed is a battery reversal and not a ring signal. This time is greater than half the period of the longest ring signal. If another edge is detected during this 40 ms pause, this event is characterized as a ring signal and not a battery reversal.
3. Assert the ONHM bit (Register 5, bit 3) to enable the caller ID data detection. The caller ID data passed across the RNG 1/2 pins is presented to the host via the SDO pin.
4. Clear the ONHM bit after the caller ID data is received.

5.21.2. Type II Caller ID

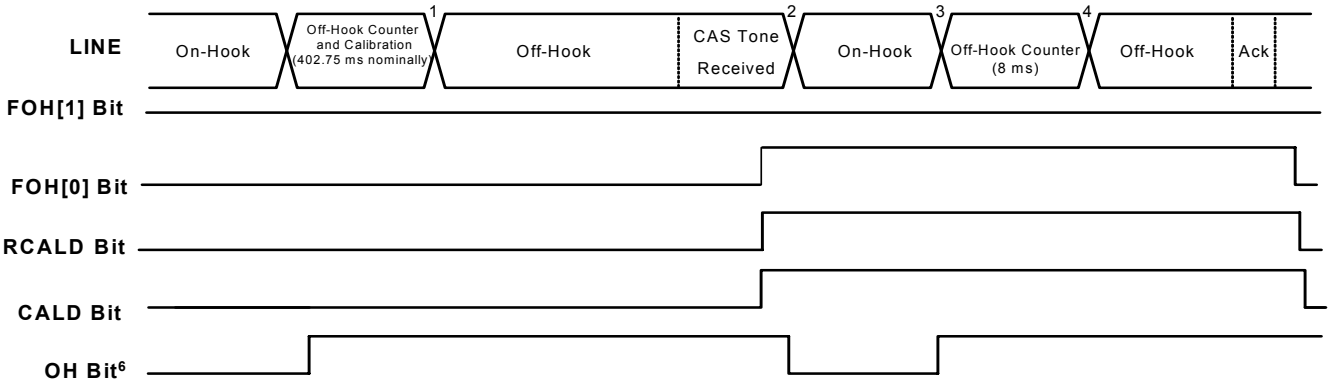
Type II Caller ID sends the CID data while the phone is off-hook and is often referred to as caller ID/call waiting (CID/CW). To receive the CID data while off-hook, use the following procedure (see Figure 23):

1. The Caller Alert Signal (CAS) tone is sent from the Central Office (CO) and is digitized along with the

line data. The host processor must detect the presence of this tone.

2. The DAA must then check for another parallel device on the same line. This is accomplished by briefly going on-hook, measuring the line voltage, and then returning to an off-hook state.
   a. Set the CALD bit (Register 17, bit 5) to disable the calibration that automatically occurs when going off-hook.
   b. Set the RCALD bit (Register 25, bit 5) to disable the resistor calibration from occurring when going off-hook.
   c. Set the FOH[1:0] bits (Register 31, bits 6:5) to 11 to reduce the off-hook counter time to 8 ms.
   d. Clear the OH bit (or drive the $\overline{\text{OFHK}}$ pin to the inactive state) to put the DAA in an on-hook state. The RXM bit (Register 19, bit 3) may also be set to mute the receive path.
   e. Read the LVS bits to determine the state of the line.
      If the LVS bits read the typical on-hook line voltage, then no parallel devices are active on the line and CID data reception can be continued.
      If the LVS bits read well below the typical on-hook line voltage, then one or more devices are present and active on the same line that are not compliant with Type II CID. Do not continue CID data reception.
   f. Set the OH bit to 1 (or drive the $\overline{\text{OFHK}}$ pin to the active state) to return to an off-hook state. After returning to an off-hook state and waiting 8 ms for the off-hook counter, normal data transmission and reception can proceed. If a non-compliant parallel device is present, then a reply tone is not sent by the host tone generator and the CO does not proceed with sending the CID data. If all devices on the line are Type II CID compliant, then the host must mute its upstream data output to avoid propagation of its reply tone and the subsequent CID data. After muting its upstream data output, the host processor should then return an acknowledgement (ACK) tone to the CO to request the transmission of the CID data.
3. The CO then responds with the CID data and the host processor unmutes the upstream data output and continues with normal operation.
4. The muting of the upstream data path by the host processor mutes the handset in a telephone application so the user cannot hear the acknowledgement tone and CID data being sent.
5. The CALD and RCALD bits can be cleared to re-enable the automatic calibration when going off-hook. The FOH[1:0] bits also can be programmed to 01 to restore the default off-hook counter time.

Because of the nature of the low-power ADC, the data presented on SDO could have up to a 10% dc offset. The caller ID decoder must either use a high pass or a band pass filter to accurately retrieve the caller ID data.



Notes:

1. The off-hook counter and calibrations prevent transmission or reception of data for 402.75 ms (default) for the line voltage to settle.
2. The caller alert signal (CAS) tone transmits from the CO to signal an incoming call.
3. The device is taken on-hook to read the line voltage in the LVS bits to detect parallel handsets. In this mode, no data is transmitted on the SDO pin.
4. When the device returns off-hook, the normal off-hook counter is reduced to 8 ms. If the CALD and RCALD bits are set, then the automatic calibrations are not performed.
5. After allowing the off-hook counter to expire (8 ms), normal transmission and reception can continue. If CID data reception is required, send the appropriate signal to the CO at this time.
6. This example uses the OH bit to put the Si3056 into an off-hook state. The $\overline{\text{OFHK}}$ pin can also be used to accomplish this. To use the $\overline{\text{OFHK}}$ pin instead of the OH bit, simply enable the OHE bit (Register 5, bit 1) and drive the $\overline{\text{OFHK}}$ pin low during the preceding sequence. This has the same effect as setting the OH bit.

Figure 23. Implementing Type II Caller ID on the Si3056

5.22. Overload Detection

The Si3056 can be programmed to detect an overload condition that exceeds the normal operating power range of the DAA circuit. To use the overload detection feature, the following steps should be followed:

1. Set the OH bit (Register 5, bit 0) to go off-hook, and wait 25 ms to allow line transients to settle.
2. Enable overload detection by then setting the OPE bit high (Register 17, bit 3).

If the DAA then senses an overload situation, it automatically presents an 800 Ω impedance to the line to reduce the hookswitch current. At this time, the DAA also sets the OPD bit (Register 19, bit 0) to indicate that an overload condition exists. The line current detector within the DAA has a threshold that is dependant upon the ILIM bit (Register 26). When ILIM = 0, the overload detection threshold equals 160 mA. When ILIM = 1, the overload detection threshold equals 60 mA. The OPE bit should always be cleared before going off-hook.

5.23. Gain Control

The Si3056 supports different gain and attenuation settings depending on the line-side device being used. For both devices, gains of 0, 3, 6, 9, and 12 dB can be selected for the receive path with the ARX[2:0] bits. The receive path can also be muted with the RXM bit. Attenuations of 0, 3, 6, 9, and 12 dB can also be selected for the transmit path with the ATX[2:0] bits. The transmit path also can be muted with the TXM bit (Register 15).

When using the Si3019 line-side device, the Si3056 provides even more flexible gain and attenuation settings. The TXG2 and RXG2 bits (registers 38–39) enable gain or attenuation in 1 dB increments up to 15 dB for the transmit and receive paths. The TGA2 and RGA2 bits select either gain or attenuation for these registers. The TXG3 and RXG3 bits (registers 40–41) enable gain or attenuation in 0.1 dB increments up to 1.5 dB for the transmit and receive paths. The TGA3 and RGA3 bits select either gain or attenuation for these registers. These additional gain/attenuation registers are active only when the ARX[2:0] and ATX[2:0] bits are set to all 0s.

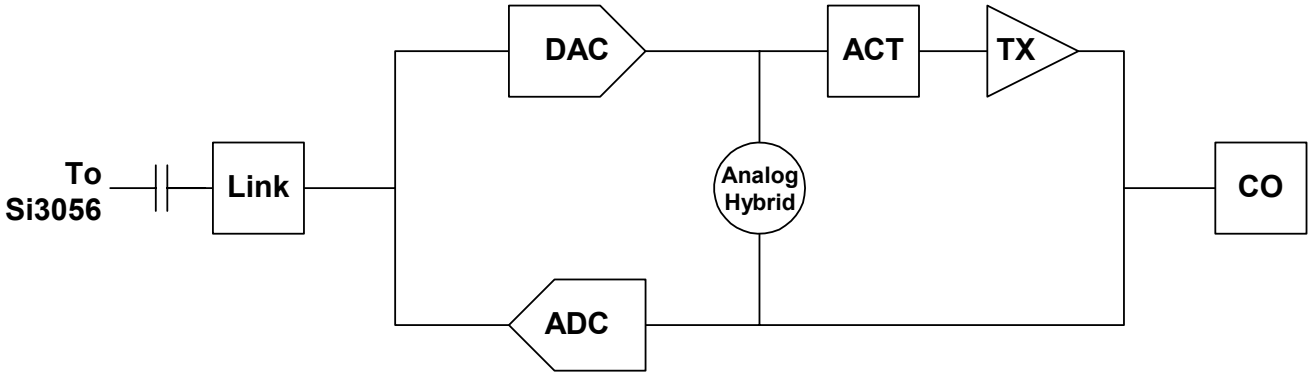


Figure 24. Si3018/19/10 Signal Flow Diagram

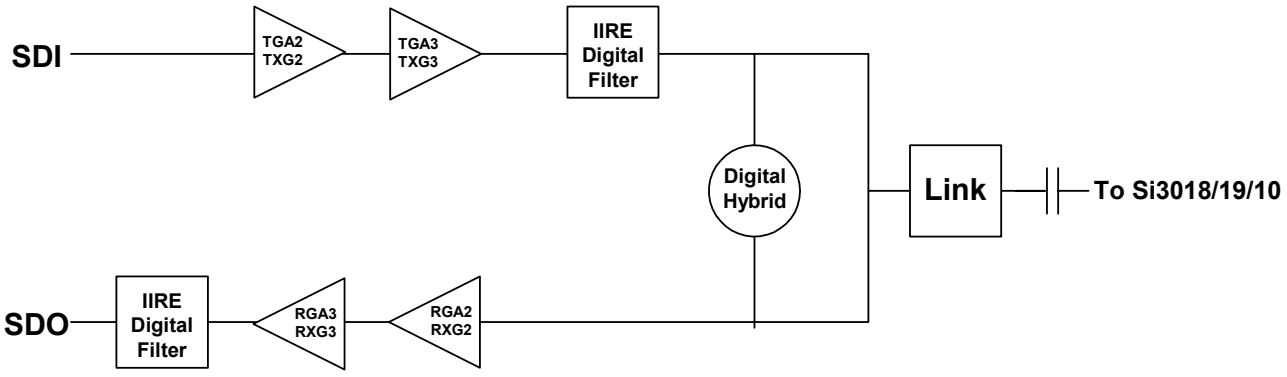


Figure 25. Si3056 Signal Flow Diagram

5.24. Filter Selection

The Si3056 supports additional filter selections for the receive and transmit signals as defined in Table 11 and Table 12 on page 15. The IIRE bit (Register 16, bit 4) selects between the IIR and FIR filters. The IIR filter provides a shorter, but non-linear, group delay alternative to the default FIR filter and only operates with an 8 kHz sample rate. Also, on the Si3019 line-side device, the FILT bit (Register 31, bit 1) selects a –3 dB low frequency pole of 5 Hz when cleared and 200 Hz when set. The FILT bit affects the receive path only.

5.25. Clock Generation

The Si3056 has an on-chip clock generator. Using a single MCLK input frequency, the Si3056 generates all the desired standard modem sample rates.

The clock generator consists of two phase-locked loops (PLL1 and PLL2) that achieve the desired sample frequencies. Figure 26 illustrates the clock generator. The architecture of the dual PLL scheme provides fast lock time on initial start-up, fast lock time when changing modem sample rates, high noise immunity, and can change modem sample rates with a single register write. Many MCLK frequencies between 1 and 60 MHz are supported. MCLK should be from a clean source, preferably directly from a crystal with a constant frequency and no dropped pulses.

In serial mode 2 (refer to the “5.26.Digital Interface” section), the Si3056 operates as a slave device. The clock generator is configured based on the SRC register to generate the required internal clock frequencies. In this mode, PLL2 is powered-down. For further details of slave mode operation, see "5.27.Multiple Device Support" on page 38.

5.25.1. Programming the Clock Generator

As shown in Figure 26, PLL1 must output a clock equal to 98.304 MHz (F_{BASE}). The F_{BASE} is determined by programming the following registers:

- Register 8: PLL1 N[7:0] divider.
- Register 9: PLL1 M[7:0] divider.

The main design consideration is the generation of a base frequency, defined as follows:

$$F_{BASE} = \frac{F_{MCLK} \times M}{N} = 98.304 \text{ MHz}$$

N (Register 8) and M (Register 9) are 8-bit unsigned values. F_{MCLK} is the frequency of the clock provided to the MCLK pin.

Table 20 lists several standard crystal oscillator rates that can be supplied to MCLK. This list represents a sample of MCLK frequency choices. Many others are possible.

After PLL1 is programmed, the SRC[3:0] bits can achieve the standard modem sampling rates with a single write to Register 7. See "Register 7.Sample Rate Control" on page 54.

When programming the registers of the clock generator, the order of register writes is important. For PLL1 updates, N (Register 8, bits 7:0) must be written first, then immediately followed by a write to M (Register 9, bits 7:0).

The values shown in Table 20 satisfy the preceding equation. However, when programming the registers for N and M, the value placed in these registers must be one less than the value calculated from the equations. For example, with an MCLK of 46.08 MHz, the values placed in the N and M registers are 0x0Dh and 0x1Fh, respectively.

Table 20. MCLK Examples

MCLK (MHz)	N	M
1.8432	3	160
4.0960	1	24
6.1440	1	16
8.1920	1	12
9.2160	3	32
10.3680	27	256
11.0592	9	80
12.288	1	8
14.7456	3	20
18.4320	3	16
24.5760	1	4
25.8048	21	80
44.2368	9	20
46.0800	15	32
47.9232	39	80
56.0000	35	36

5.25.2. PLL Lock Times

The Si3056 changes sample rates quickly. However, lock time varies based on the programming of the clock generator. The following relationships describe the boundaries on PLL locking time:

PLL1 lock time < 1 ms
PLL2 lock time 100 μs to 1 ms

For modem designs, Silicon Laboratories® recommends that PLL1 be programmed during initialization. No further programming of PLL1 is necessary. The SRC[3:0] register can be programmed for the required initial sample rate, typically 7200 Hz. Rate changes are made by writing to SRC[3:0] (Register 7, bits 3:0).

The final design consideration for the clock generator is the update rate of PLL1. The following criteria must be satisfied for the PLLs to remain stable:

$$F_{UP1} = \frac{F_{MCLK}}{N} \geq 144 \text{ kHz}$$

where F_{UP1} is shown in Figure 26.

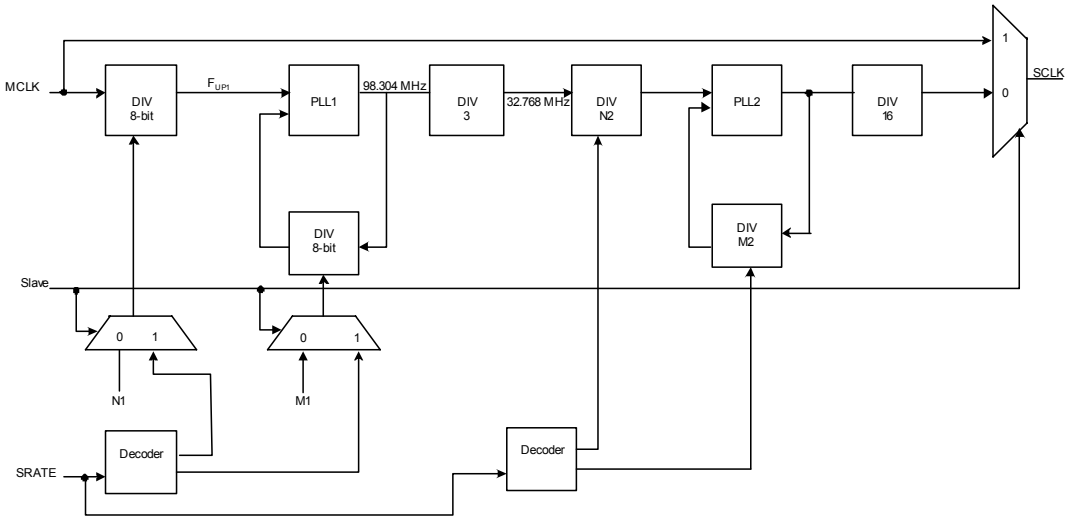


Figure 26. Update Rate of PLL1

5.26. Digital Interface

The Si3056 has two serial interface modes that support most standard modem DSPs. The M0 and M1 mode pins select the interface mode. The key difference between these two serial modes is the operation of the FSYNC signal. Table 21 summarizes the serial mode definitions.

Table 21. Serial Modes

Mode	M1 M0	Description
0	0 0	FSYNC frames data
1	0 1	FSYNC pulse starts data frame
2	1 0	Slave mode
3	1 1	Reserved

The digital interface consists of a single, synchronous serial link that communicates both telephony and control data.

In serial mode 0 or 1, the Si3056 operates as a master, where the master clock (MCLK) is an input, the serial data clock (SCLK) is an output, and the frame sync signal (FSYNC) is an output. The MCLK frequency and the value of the sample rate control registers 7, 8, and 9 determine the sample rate (Fs). The serial port clock, SCLK, runs at 256 bits per frame, where the frame rate is equivalent to the sample rate. See "5.25.Clock Generation" on page 36 for details on programming sample rates.

The Si3056 transfers 16- or 15-bit telephony data in the primary timeslot and 16-bit control data in the secondary timeslot. Figures 27 and 28 show the relative timing of the serial frames. Primary frames occur at the frame rate and are always present. To minimize overhead in the external DSP, secondary frames are present only when requested.

Two methods exist for requesting a secondary frame to transfer control information. The default powerup mode uses the LSB of the 16-bit transmit (TX) data word as a flag to request a secondary transfer. Only 15-bit TX data is transferred, which results in a small loss of SNR but

provides software control of the secondary frames. As an alternative method, the FC pin can serve as a hardware flag for requesting a secondary frame. The external DSP can turn on the 16-bit TX mode by setting the SB bit (Register 1, bit 0). In the 16-bit TX mode, the hardware FC pin must be used to request secondary transfers.

Figures 29 and 30 illustrate the secondary frame read cycle and write cycle, respectively. During a read cycle, the R/W bit is high and the 7-bit address field contains the address of the register to be read. The contents of the 8-bit control register are placed on the SDO signal. During a write cycle, the R/W bit is low and the 7-bit address field contains the address of the register to be written. The 8-bit data to be written immediately follows the address on SDI. Only one register can be read or written during each secondary frame. See "6.Control Registers" on page 48 for the register addresses and functions.

In serial mode 2, the Si3056 operates as a slave device, where MCLK is an input, SCLK is a no connect, and FSYNC is an input. In addition, the RGDT/FSD/M1 pin operates as a delayed frame sync (FSD) and the FC/RGDT pin operates as ring detect (RGDT). In this mode, FC operation is not supported. For details on operating the Si3056 as a slave device, see “5.27.Multiple Device Support” .

5.27. Multiple Device Support

The Si3056 supports the operation of up to seven additional devices on a single serial interface. Figure 35 shows the typical connection of the Si3056 and one additional serial voice codec (Si3000).

The Si3056 must be the master in this configuration. Configure the secondary codec as a slave device with the master’s SCLK used as the MCLK input to the codec, and the master’s frame sync delay signal (FSD) used as the codec’s FSYNC input. On powerup, the Si3056 master does not detect the additional codec on the serial bus. The FC/RGDT pin is an input, operating as the hardware control for secondary frames, and the RGDT/FSD/M1 pin is an output, operating as the active low ring detection signal. Program the master device for master/slave mode before enabling the isolation link, because a ring signal causes a false transition to the slave device’s FSYNC.

Register 14 provides the necessary control bits to configure the Si3056 for master/slave operation. Bit 0 (DCE) sets the Si3056 in master/slave mode, also referred to as daisy-chain mode. When the DCE bit is set, the FC/RGDT pin becomes the ring detect output and the RGDT/FSD/M1 pin becomes the frame sync delay output. When using multiple devices, secondary frame communication must be requested via software in the LSB of the transmit (TX) data word.

Bits 7:5 (NSLV2:NSLV0) set the number of slaves to be supported on the serial bus. For each slave, the Si3056 generates an FSYNC to the DSP. In daisy-chain mode, the polarity of the ring signal can be controlled by bit 1 (RPOL). When RPOL = 1, the ring detect signal (now an output on the FC/RGDT pin) is active high.

The Si3056 supports a variety of codecs and additional Si3056s. The type of slave codec(s) used is set by the SSEL[1:0] bits (Register 14, bits 4:3) and determines the type of signalling used in the LSB of SDO. This assists the host in isolating which data stream is the master and which is the slave. If the LSB is used for signalling, the master device has a unique setting relative to the slave devices. The DSP can use this information to determine which FSYNC marks the beginning of a sequence of data transfers.

The delayed frame sync (FSD) of each device is supplied as the FSYNC of each subsequent slave device in the daisy chain. The master Si3056 generates an FSYNC signal for each device every 16 or 32 SLCK periods. The delay period is set by FSD (Register 14, bit 2). Figure 31 on page 43 and Figure 34 on page 46 show the relative timing for daisy chaining operation. Primary communication frames occur in sequence, followed by secondary communication frames, if requested. When writing/reading the master device via a secondary frame, all secondary frames of the slave devices also must be written. When writing/reading a slave device via a secondary frame, the secondary frames of the master and all other slaves must be written also. “No operation” writes/reads to secondary frames are accomplished by writing/reading a 0 value to address 0.

If FSD is set for 16 SCLK periods between FSYNCs, only serial mode 1 can be used. In addition, the slave devices must delay the tri-state to active transition of their SDO sufficiently from the rising edge of SCLK to avoid bus contention.

The Si3056 supports the operation of up to eight Si3056 devices on a single serial bus. The master Si3056 must be configured in serial mode 1. Configure the slave(s) Si3056 in serial mode 2. Figure 36 on page 47 shows a typical master/slave connection using three Si3056 devices.

When in serial mode 2, FSYNC becomes an input, RGDT/FSD/M1 becomes the delay frame sync output, and FC/RGDT becomes the ring detection output. The serial interface runs at the MCLK input frequency fed from a master device (such as a master Si3056's SCLK output). To achieve the proper sampling frequency, the

SRC[3:0] bits (Register 7, bits 3:0) must be programmed with the proper sample rate value before the sampled line data is valid. The SCLK pin of the slave is a no connect in this configuration.

The delay between FSYNC input and delayed frame sync output (RGDT/FSD/M1) is 16 SCLK periods. The RGDT/FSD/M1 output has a waveform identical to the FSYNC signal in serial mode 0. In addition, the LSB of SDO is set to 0 by default for all devices in serial mode 2.

5.28. Power Management

The Si3056 supports four basic power management operation modes. The modes are normal operation, reset operation, sleep mode, and full powerdown mode. PDN and PDL bits (Register 6) control the power management modes.

On powerup, or following a reset, the Si3056 is in reset operation. The PDL bit is set, and the PDN bit is cleared. The Si3056 is operational, except for the isolation link. No communication between the Si3056 and line-side device can occur during reset operation. Bits associated with the line-side device are not valid in this mode.

In typical applications, the DAA will predominantly be operated in normal mode. In this mode, the PDL and PDN bits are cleared. The Si3056 is operational and the isolation link is passing information between the Si3056 and the line-side device.

The Si3056 supports a low-power sleep mode to support ring validation and wake-on-ring features. The clock generator registers 7, 8, and 9 must be programmed with valid, non-zero values and the PDL bit must be clear before enabling sleep mode. The PDN bit must then be set. When the Si3056 is in sleep mode the MCLK signal must remain active. In low-power sleep mode with MCLK active, the Si3056 is non-functional except for the isolation link and the RGDT signal. To take the Si3056 out of sleep mode, pulse the reset pin (RESET) low.

In summary, the powerdown/up sequence for sleep mode is as follows:

1. Ensure that Registers 7, 8, and 9 have valid non-zero values, and ensure the PDL bit (Register 6, bit 4) is cleared.
2. Set the PDN bit (Register 6, bit 3).
3. The device is now in sleep mode. MCLK must stay active.
4. To exit sleep mode, reset the Si3056 by pulsing the RESET pin.
5. Program registers to desired settings.

The Si3056 also supports an additional powerdown mode. When both the PDN (Register 6, bit 3) and PDL (Register 6, bit 4) bits are set, the chipset enters a complete powerdown mode and draws negligible current (deep sleep mode). Turn off the PLL2 before entering deep sleep mode (i.e., set Register 9 to 0 and then Register 6 to 0x18). In this mode, the Si3056 is non-functional. Normal operation is restored by the same process for taking the DAA out of sleep mode.

5.29. Calibration

The Si3056 initiates two auto-calibrations by default when the device goes off-hook or experiences a loss in line power. A 17 ms resistor calibration is performed to allow circuitry internal to the DAA to adjust to the exact line conditions present at that time. This resistor calibration can be disabled by setting the RCALD bit (Register 25, bit 5). A 256 ms ADC calibration is also performed to remove offsets that might be present in the on-chip A/D converter which could affect the A/D dynamic range. The ADC auto-calibration is initiated after the DAA dc termination stabilizes, and the resistor calibration completes. Because large variations in line conditions and line card behavior exist, it could be beneficial to use manual calibration instead of auto-calibration.

Execute manual ADC calibration as close as possible to 256 ms before valid transmit/receive data is expected.

Take the following steps to implement manual ADC calibration:

1. The CALD (auto-calibration disable—Register 17) bit must be set to 1.
2. The MCAL (manual calibration) bit must be toggled to 1 and then 0 to begin and complete the calibration.
3. The calibration is completed in 256 ms.

5.30. In-Circuit Testing

With the Si3056's advanced design the designer can determine system functionality during production line tests, and during support for end-user diagnostics. Four loopback modes allow thorough coverage of system components. Four of the test modes require a line-side power source. Although a standard phone line can be used, the test circuit in Figure 1 on page 6 is adequate. In addition, an off-hook sequence must be performed to connect the power source to the line-side device.

For the start-up loopback test mode, line-side power is not necessary and no off-hook sequence is required. The start-up test mode is enabled by default. When the PDL bit (Register 6, bit 4) is set (the default case), the line-side is in a powerdown mode and the DSP-side is in a digital loop-back mode. Data received on SDI

passes through the internal filters and transmitted on SDO which introduces approximately 0.9 dB of attenuation on the SDI signal received. The group delay of both transmit and receive filters exists between SDI and SDO. Clearing the PDL bit disables this mode and the SDO data is switched to the receive data from the line-side. When the PDL bit is cleared, the FDT bit (Register 12, bit 6) becomes active, indicating the successful communication between the line-side and DSP-side. This can be used to verify that the isolation link is operational.

The digital data loop-back mode offers a way to input data on the SDI pin and have the identical data be output on the SDO pin by bypassing the transmit and receive filters. Setting the DDL bit (Register 10, bit 0) enables this mode. No line-side power or off-hook sequence is required for this mode. The digital data loopback mode is useful to verify communication between the host processor/DSP and the DAA.

The remaining test modes require an off-hook sequence to operate. The following sequence describes the off-hook procedure required for the following test modes:

1. Powerup or reset.
2. Program the clock generator to the chosen sample rate.
3. Enable line-side by clearing the PDL bit.
4. Issue an off-hook command.
5. Delay 402.75 ms to allow calibration to occur.
6. Set the desired test mode.

In the communications link loopback mode, the host sends a digital input test pattern on SDI and receives that digital test pattern back on SDO. To enable this mode, set the IDL bit (Register 1, bit 1). In this mode, the communication link is tested. The digital stream is delivered across the isolation capacitors, C1 and C2 of Figure 16 on page 17, to the line-side device and returned across the same interface. In this mode, the 0.9 dB attenuation and filter group delays also exist.

The final testing mode, internal analog loopback, allows the system to test the operation of the transmit and receive paths through the line-side device and the external components shown in Figure 16 on page 17. In this test mode, the host provides a digital test waveform on SDI. This data passes across the communications link, is transmitted to and received from the line, passes back across the communications link, and is presented to the host on SDO. To enable this mode, clear the HBE bit (Register 2, bit 1).

When the HBE bit is cleared, this causes a dc offset that affects the signal swing of the transmit signal. Silicon Laboratories® recommends that the transmit signal be 12 dB lower than normal transmit levels. A lower level eliminates clipping from the dc offset that results from disabling the hybrid. It is assumed in this test that the line ac impedance is nominally 600 Ω.

Note: All test modes are mutually exclusive. If more than one test mode is enabled concurrently, the results are unpredictable.

5.31. Exception Handling

The Si3056 provides several mechanisms to determine if an error occurs during operation. Through the secondary frames of the serial link, the controlling systems can read several status bits.

The bit of highest importance is the frame detect bit (FDT, Register 12, bit 6), which indicates that the system-side (Si3056) and line-side devices are communicating.

During normal operation, the FDT bit can be checked before reading bits for information about the line-side. If FDT is not set, the following bits related to the line-side are invalid—RDT, RDTN, RDTP, LCS[4:0], LSID[1:0], REVB[3:0], LCS2[7:0], LVS[7:0], ROV, BTD, DOD, and OVL; the RGDT operation is also non-functional.

Following Powerup and reset, the FDT bit is not set because the PDL bit (Register 6 bit 4) defaults to 1. The communications link does not operate and no information about the line-side can be determined. The user must program the clock generator to a valid configuration for the system and clear the PDL bit to activate the communications link. As the system- and line-side devices are establishing communication, the system-side device does not generate FSYNC signals. Establishing communication takes less than 10 ms. Therefore, if the controlling DSP serial interface is interrupt driven based on the FSYNC signal, the controlling DSP does not require a special delay loop to wait for this event to complete.

The FDT bit also can indicate if the line-side device executes an off-hook request successfully. If the line-side device is not connected to a phone line, the FDT bit remains cleared. The controlling DSP must provide sufficient time for the line-side to execute the off-hook request. The maximum time for FDT to be valid following an off-hook request is 10 ms. If the FDT bit is high, the LCS[4:0] bits indicate the amount of loop current flowing. If the FDT fails to be set following an off-hook request, the PDL bit (Register 6) must be set high for at least 1 ms to reset the line-side.

5.32. Revision Identification

With the Si3056 the system designer can determine the revision of the Si3056 and/or the line-side device. The REVA[3:0] bits (Register 11, bits 3:0) identify the

revision of the Si3056. The REVB[3:0] bits (Register 13, bits 3:0) identify the revision of the line-side device. Table 22 lists revision values for all devices and might contain future revisions not yet in existence.

Table 22. Revision Values

Revision	Si3056	Si3018	Si3019	Si3010
A	0001	0001	0001	0001
B	0010	0010	0010	0010
C	0011	0011	0011	0011
D	0100	0100	0100	0100
E	0101	0101	0101	0101
F	0110	0110	0110	0110

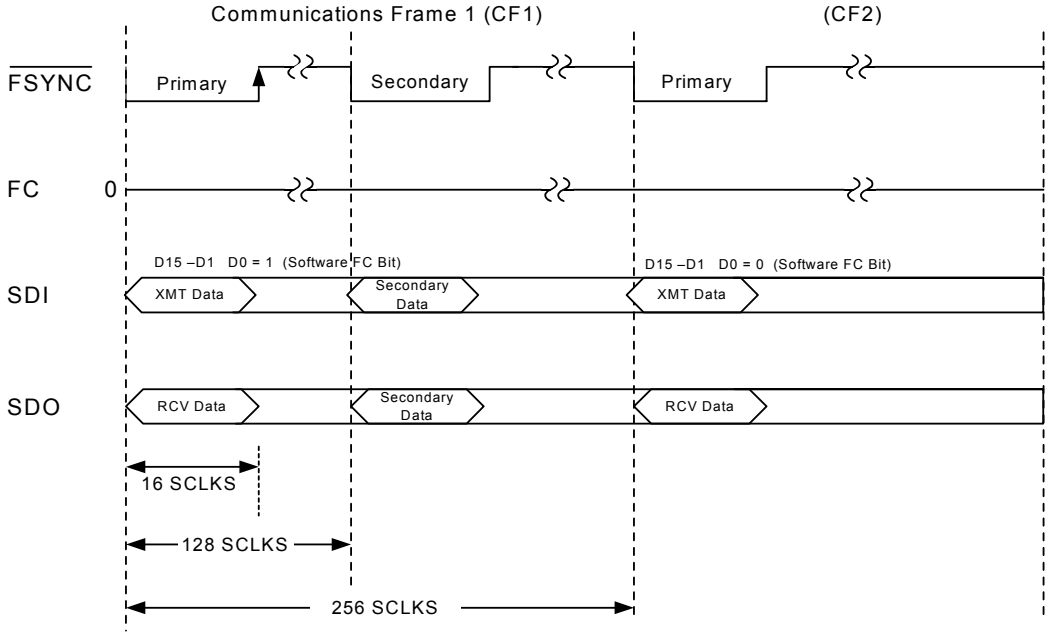


Figure 27. Software FC/RGDT Secondary Request

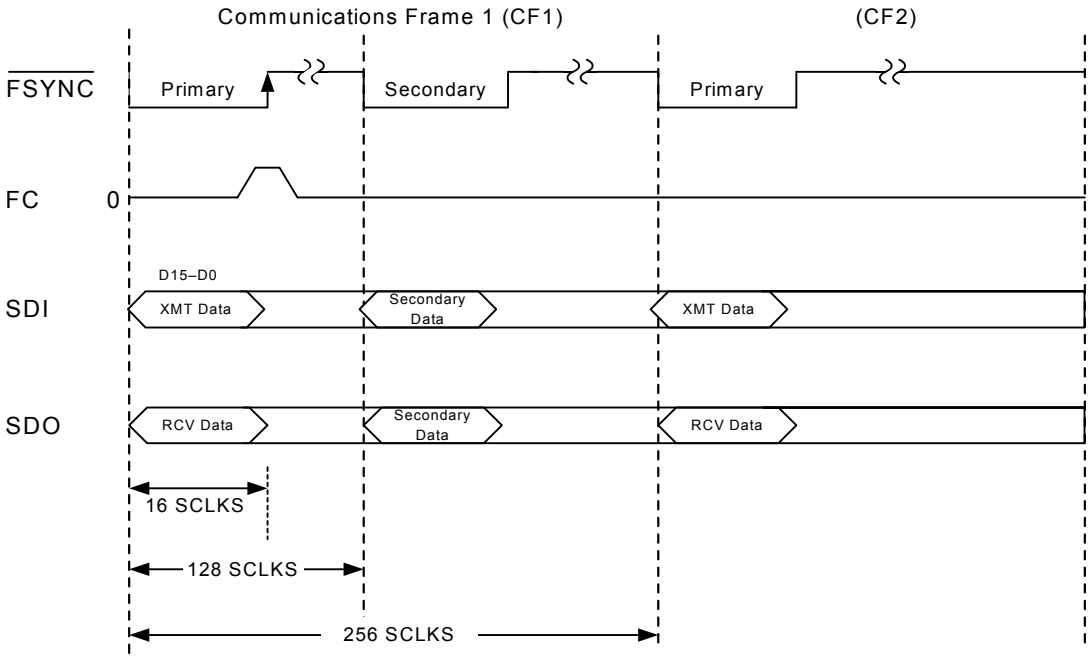


Figure 28. Hardware FC/$\overline{\text{RGDT}}$ Secondary Request

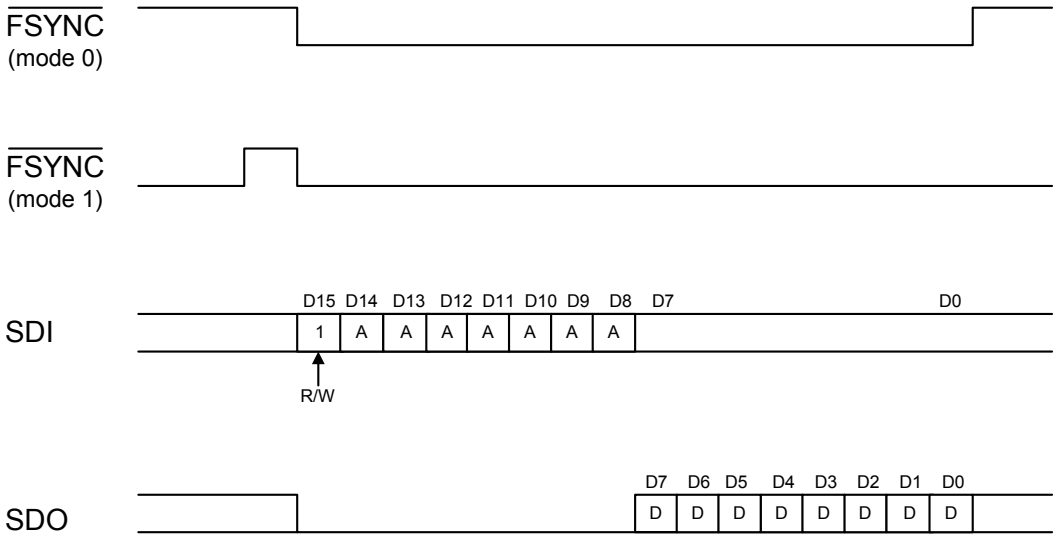


Figure 29. Secondary Communication Data Format—Read Cycle

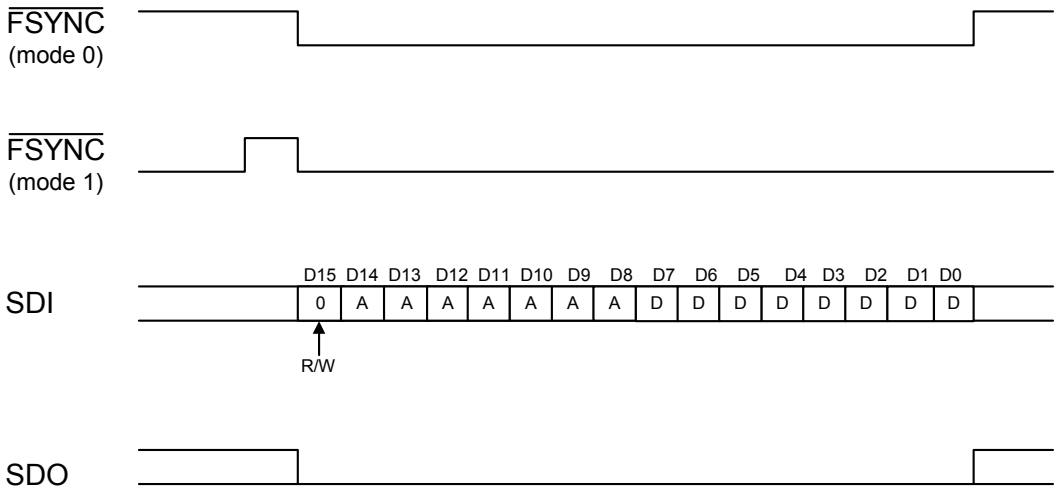


Figure 30. Secondary Communication Data Format—Write Cycle

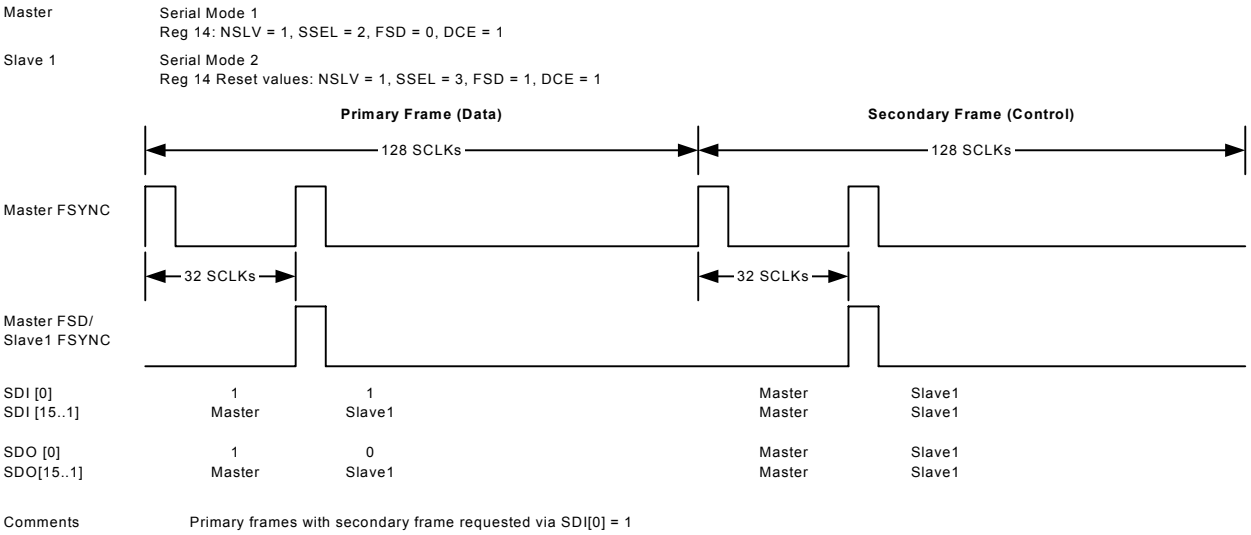


Figure 31. Daisy Chaining of a Single Slave (Pulse FSD)

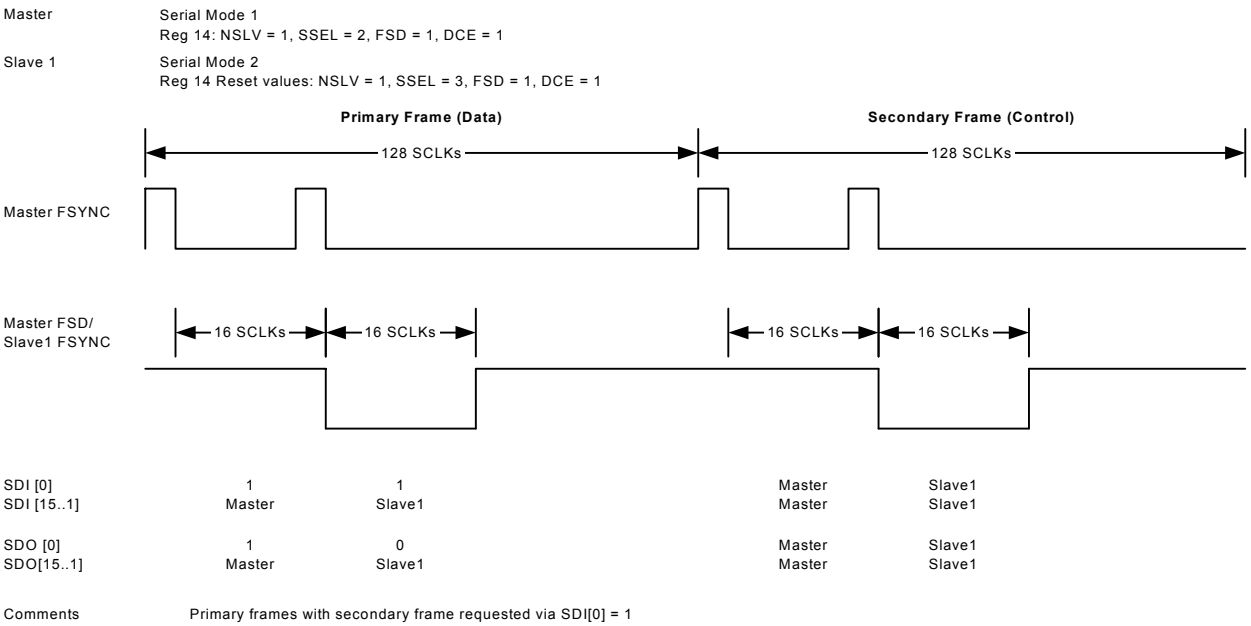


Figure 32. Daisy Chaining of a Single Slave (Frame FSD)

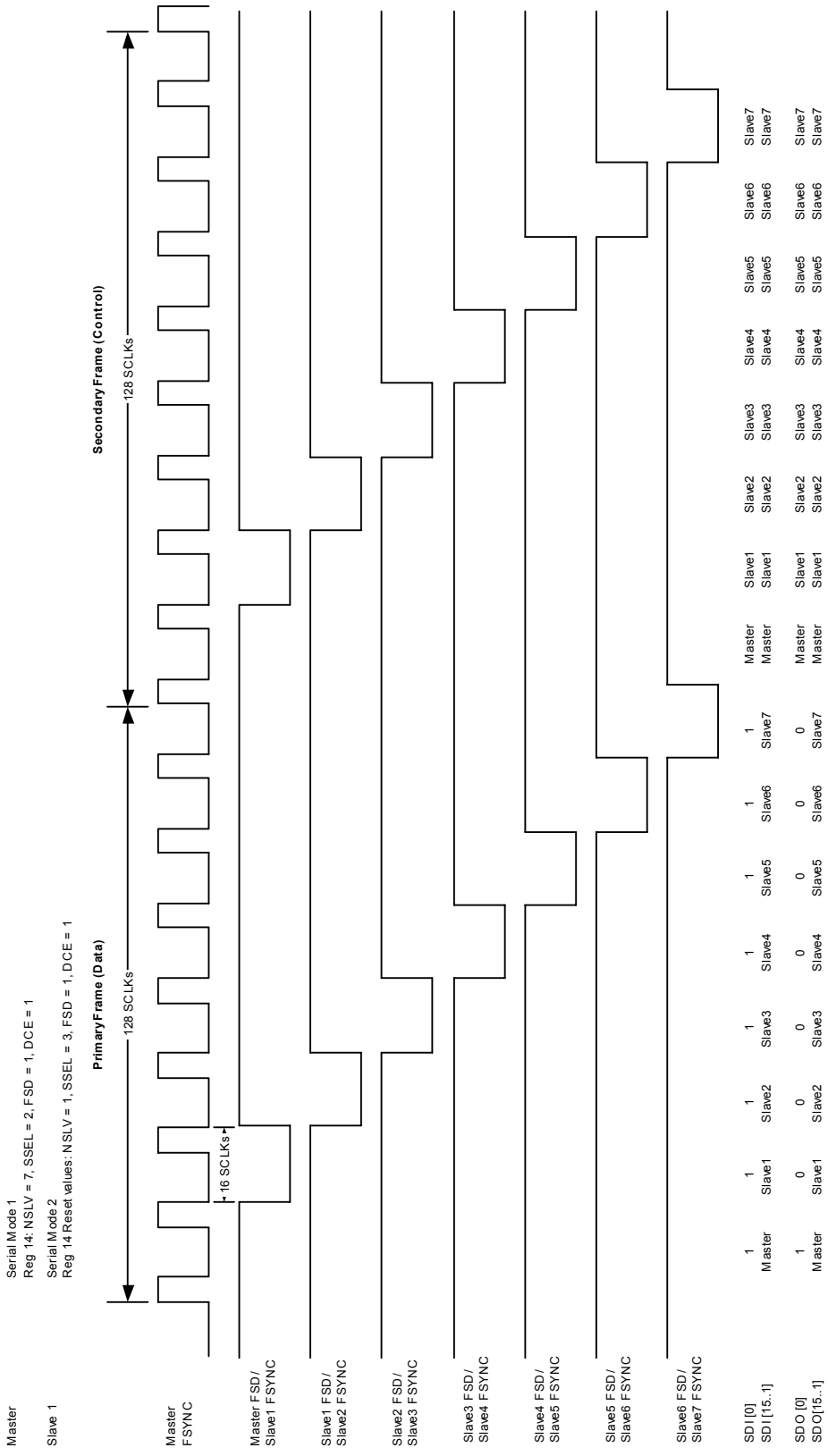


Figure 33. Daisy Chaining of Eight DAAs

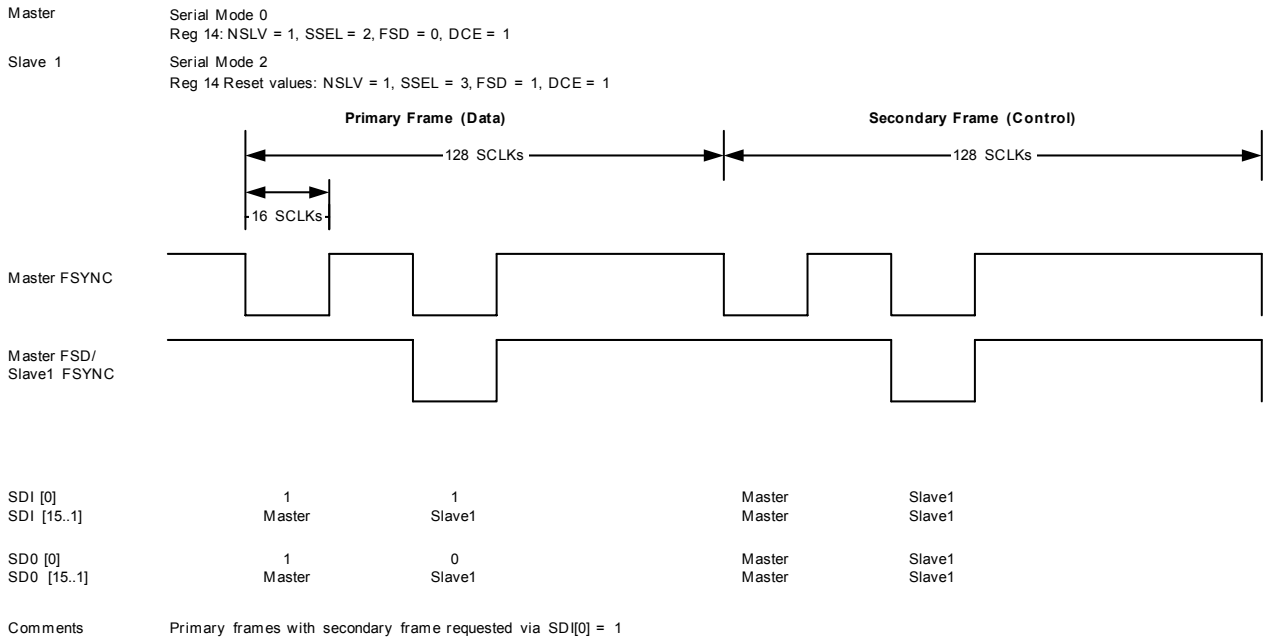


Figure 34. Daisy Chaining with Framed $\overline{\text{FSYNC}}$ and Framed FSD

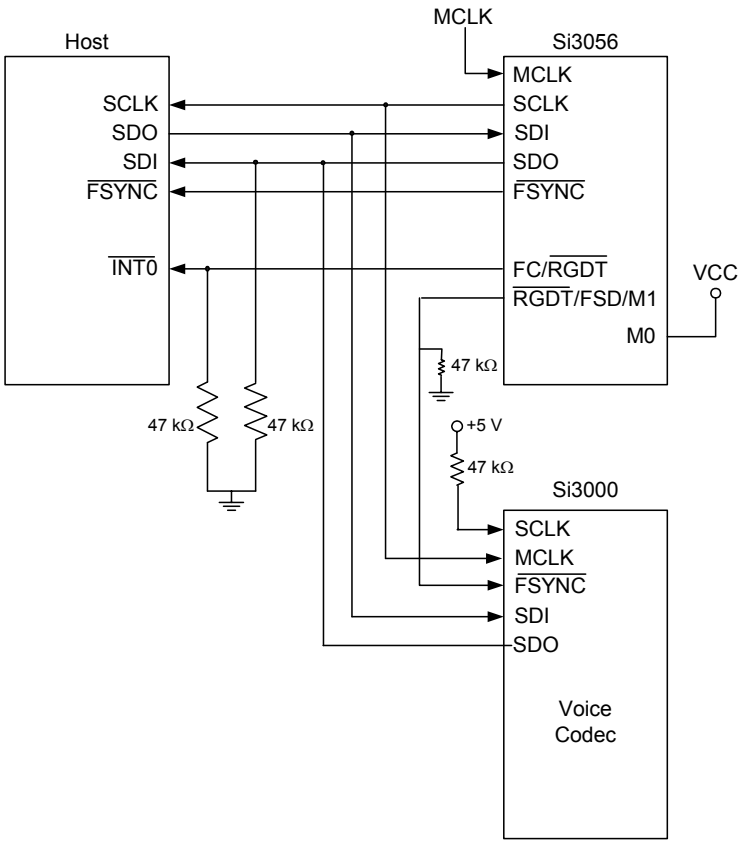


Figure 35. Typical Connection for Master/Slave Operation (e.g., Data/Fax/Voice Modem)

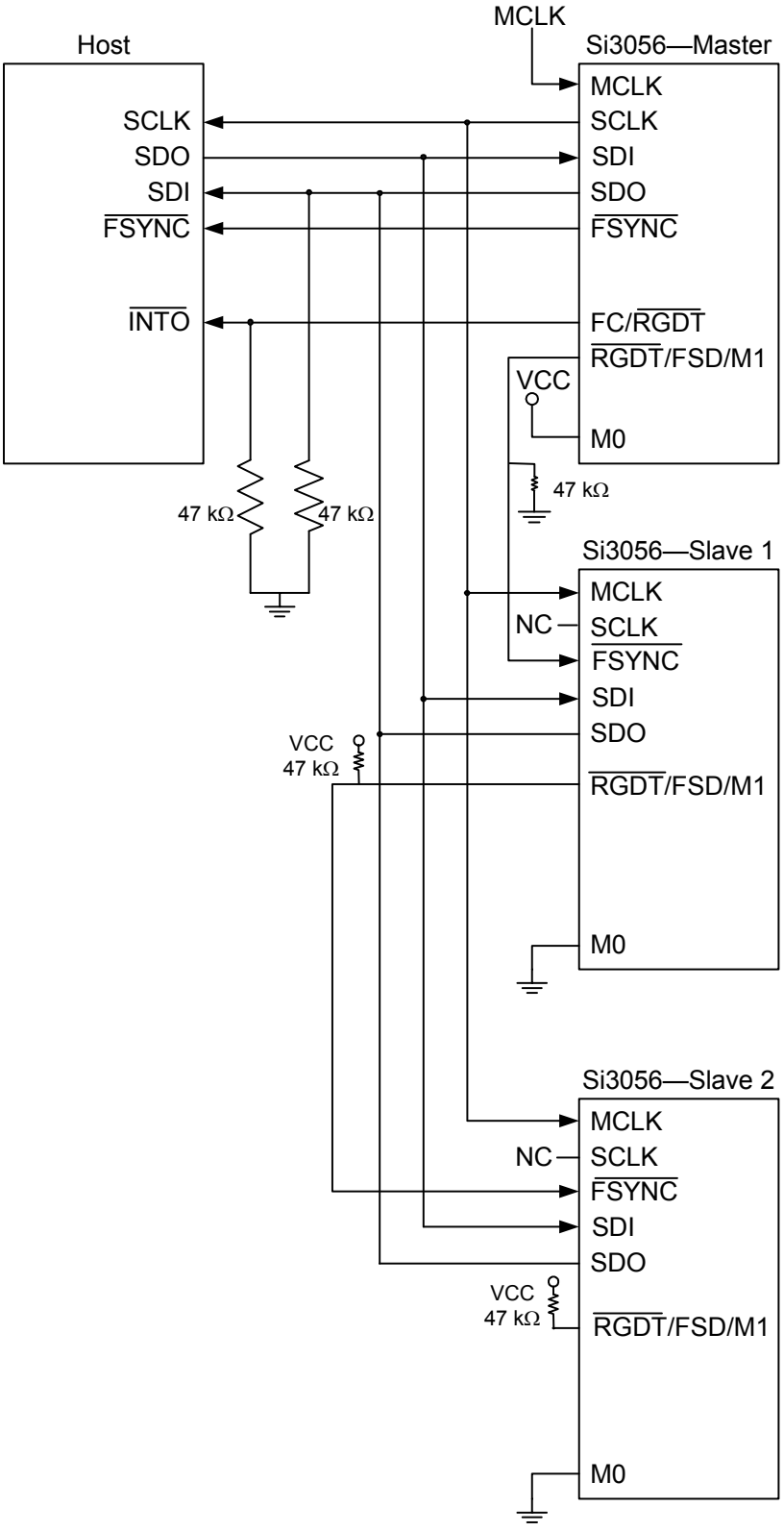


Figure 36. Typical Connection for Multiple DAAS

6. Control Registers

Table 23. Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Control 1	SR		PWMM[1:0]		PWME		IDL	SB
2	Control 2	INTE	INTP		WDTEN		RDI	HBE	RXE
3	Interrupt Mask	RDTM	ROVM	FDTM	BTDM	DODM	LCSOM	DLCSM	POLM
4	Interrupt Source	RDTI	ROVI	FDTI	BTDI	DODI	LCSOI	DLCSI	POLI
5	DAA Control 1		RDTN	RDTP	OPOL	ONHM	RDT	OHE	OH
6	DAA Control 2				PDL	PDN			
7	Sample Rate Control					SRC[3:0]			
8	PLL Divide N	N[7:0]							
9	PLL Divide M	M[7:0]							
10	DAA Control 3								DDL
11	System-Side and Line-Side Revision	LSID[3:0]				REVA[3:0]			
12	Line-Side Device Status		FDT		LCS[4:0]				
13	Line-Side Device Revision		0	REVB[3:0]					
14	Serial Interface Control	NSLV[2:0]			SSEL[1:0]		FSD	RPOL	DCE
15	TX/RX Gain Control 1	TXM	ATX[2:0]			RXM	ARX[2:0]		
16	International Control 1	ACT2[2]	OHS	ACT[2]	IIRE			RZ	RT
17	International Control 2	CALZ	MCAL	CALD		OPE	BTE	ROV	BTD
18	International Control 3							RFWE	
19	International Control 4						OVL	DOD	OPD
20	Call Progress Rx Attenuation	ARM[7:0]							
21	Call Progress Tx Attenuation	ATM[7:0]							
22	Ring Validation Control 1	RDLY[1:0]		RMX[5:0]					
23	Ring Validation Control 2	RDLY[2]	RTO[3:0]				RCC[2:0]		
24	Ring Validation Control 3	RNGV		RAS[5:0]					
25	Resistor Calibration	RCALS	RCALM	RCALD		RCAL[3:0]			
26	DC Termination Control	DCV[1:0]		MINI[1:0]				ILIM	DCR
27	Reserved								
28	Loop Current Status	LCS2[7:0]							
29	Line Voltage Status	LVS[7:0]							
30	AC Termination Control				FULL2	ACIM[3:0][1]			
31	DAA Control 4	FULL[1]	FOH[1:0]			OHS2		FILT[1]	LVFD[1]
32–37	Reserved								
38	TX Gain Control 2				TGA2[1]	TXG2[3:0][1]			
39	RX Gain Control 2				RGA2[1]	RXG2[3:0][1]			
40	TX Gain Control 3				TGA3[1]	TXG3[3:0][1]			
41	RX Gain Control 3				RGA3[1]	RXG3[3:0][1]			
42	Reserved								
43	Line Current/Voltage Threshold Interrupt	CVT[7:0][1]							
44	Line Current/Voltage Threshold Interrupt Control					CVI[1]	CVS[1]	CVM[1]	CVP[1]
45–52	Programmable Hybrid Register 1–8	HYB1–8[7:0]							
53–58	Reserved								
59	Spark Quenching Control		SQ1		SQ0		RG1	GCE	

Notes:
1. Bit is available for Si3019 line-side device only.
2. Bit is available for Si3010 and Si3018 line-side device only.

Register 1. Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR		PWMM[1:0]		PWME		IDL	SB
Type	R/W		R/W		R/W		R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	SR	**Software Reset.** 0 = Enables the DAA for normal operation. 1 = Sets all registers to their reset value. **Note:** Bit automatically clears after being set.
6	Reserved	Read returns zero.
5:4	PWMM[1:0]	**Pulse Width Modulation Mode.** Used to select the type of signal output on the call progress AOUT pin. 00 = PWM output is clocked at 16.384 MHz as a delta-sigma data stream. A local density of 1s and 0s tracks the combined transmit and receive signals. 01 = Balanced conventional PWM output signal has high and low portions of the modulated pulse that are centered on the 16 kHz sample clock. 10 = Conventional PWM output signal returns to logic 0 at regular 32 kHz intervals and rises at a time in the 32 kHz period proportional to its instantaneous amplitude. 11 = Reserved.
3	PWME	**Pulse Width Modulation Enable.** Sums the transmit and receive audio paths and presents it as a CMOS digital-level output of PWM data. Use the circuit in “Figure 18. AOUT PWM Circuit for Call Progress” . 0 = Pulse width modulation signal for AOUT disabled. 1 = Pulse width modulation signal for call progress analog output (AOUT) enabled.
2	Reserved	Read returns zero.
1	IDL	**Isolation Digital Loopback.** 0 = Digital loopback across the isolation barrier is disabled. 1 = Enables digital loopback mode across the isolation barrier. The line-side device must be enabled and off hook before setting this mode. This data path includes the TX and RX filters.
0	SB	**Serial Digital Interface Mode.** 0 = Operation is in 15-bit mode, and the LSB of the data field indicates that a secondary frame is required. 1 = The serial port is operating in 16-bit mode and requires a secondary frame sync signal, FC, to initiate control data reads/writes.

Register 2. Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	INTE	INTP		WDTEN		RDI	HBE	RXE
Type	R/W	R/W		R/W		R/W	R/W	R/W

Reset settings = 0000_0011

Bit	Name	Function
7	INTE	**Interrupt Pin Enable.** 0 = The AOUT/$\overline{\text{INT}}$ pin functions as an analog output for call progress monitoring purposes. 1 = The AOUT/$\overline{\text{INT}}$ pin functions as a hardware interrupt pin.
6	INTP	**Interrupt Polarity Select.** 0 = The AOUT/$\overline{\text{INT}}$ pin, when used in hardware interrupt mode, is active low. 1 = The AOUT/$\overline{\text{INT}}$ pin, when used in hardware interrupt mode, is active high.
5	Reserved	Returns to zero.
4	WDTEN	**Watchdog Timer Enable.** When set, this bit can only be cleared by a hardware reset. The watchdog timer monitors register accesses. If no register accesses occur within a 4 second window, the DAA is put into an on-hook state. A write of a DAA register restarts the watchdog timer counter. If the watchdog timer times out, the OH and OHE bits are cleared, placing the DAA into an on-hook state. Setting the OH bit or setting the OHE bit and asserting the $\overline{\text{OFHK}}$ pin places the DAA back into an off-hook state. 0 = Watchdog timer disabled. 1 = Watchdog timer enabled.
3	Reserved	Returns to zero.
2	RDI	**Ring Detect Interrupt Mode.** This bit operates in conjunction with the RDTM and RDTI bits. This bit is selected if one or two interrupts are generated for every ring burst. 0 = An interrupt is generated at the beginning of every ring burst. 1 = An interrupt is generated at the beginning and end of every ring burst. The interrupt at the beginning of the ring burst must be serviced (by writing a 0 to the RDTI bit) before the end of the ring burst for both interrupts to occur.
1	HBE	**Hybrid Enable.** 0 = Disconnects hybrid in transmit path. 1 = Connects hybrid in transmit path.
0	RXE	**Receive Enable.** 0 = Receive path disabled. 1 = Enables receive path.

Register 3. Interrupt Mask

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDTM	ROVM	FDTM	BTDM	DODM	LCSOM	DLCSM	POLM
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	RDTM	**Ring Detect Mask.** 0 = A ring signal does not cause an interrupt on the AOUT/$\overline{\text{INT}}$ pin. 1 = A ring signal causes an interrupt on the AOUT/$\overline{\text{INT}}$ pin.
6	ROVM	**Receive Overload Mask.** 0 = A receive overload does not cause an interrupt on the AOUT/$\overline{\text{INT}}$ pin. 1 = A receive overload causes an interrupt on the AOUT/$\overline{\text{INT}}$ pin.
5	FDTM	**Frame Detect Mask.** 0 = The communications link achieving frame lock does not cause an interrupt on the AOUT/$\overline{\text{INT}}$ pin. 1 = The communications link achieving frame lock causes an interrupt on the AOUT/$\overline{\text{INT}}$ pin.
4	BTDM	**Billing Tone Detect Mask.** 0 = A detected billing tone does not cause an interrupt on the AOUT/$\overline{\text{INT}}$ pin. 1 = A detected billing tone causes an interrupt on the AOUT/$\overline{\text{INT}}$ pin.
3	DODM	**Drop Out Detect Mask.** 0 = A line supply dropout does not cause an interrupt on the AOUT/$\overline{\text{INT}}$ pin. 1 = A line supply dropout causes an interrupt on the AOUT/$\overline{\text{INT}}$ pin.
2	LCSOM	**Loop Current Sense Overload Mask.** 0 = An interrupt does not occur when the LCS bits are all 1s. 1 = An interrupt occurs when the LCS bits are all 1s.
1	DLCSM	**Delta Loop Current Sense Mask.** 0 = An interrupt does not occur when the LCS bits change. 1 = An interrupt does occur when the LCS bits change.
0	POLM	**Polarity Reversal Detect Mask.** Generated from bit 7 of the LVS register. When this bit transitions, it indicates that the polarity of TIP and RING was switched. 0 = A polarity change on TIP and RING does not cause an interrupt on the AOUT/$\overline{\text{INT}}$ pin. 1 = A polarity change on TIP and RING causes an interrupt on the AOUT/$\overline{\text{INT}}$ pin.

Register 4. Interrupt Source

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDTI	ROVI	FDTI	BTDI	DODI	LCSOI	DLCSI	POLI
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	RDTI	**Ring Detect Interrupt.** 0 = A ring signal is not occurring. 1 = A ring signal is detected. If the RDTM (Register 3) and INTE (Register 2) bits are set a hardware interrupt occurs on the AOUT/$\overline{\text{INT}}$ pin. This bit must be written to a 0 to be cleared. The RDI bit (Register 2) determines if this bit is set only at the beginning of a ring pulse, or at the end of a ring pulse as well. This bit should be cleared after clearing the PDL bit (Register 6) because powering up the line-side device may cause this interrupt to be triggered.
6	ROVI	**Receive Overload Interrupt.** 0 = An excessive input level on the receive pin is not occurring. 1 = An excessive input level on the receive pin is detected. If the ROVM and INTE bits are set a hardware interrupt occurs on the AOUT/$\overline{\text{INT}}$ pin. This bit must be written to 0 to clear it. This bit is identical in function to the ROV bit (Register 17). Clearing this bit also clears the ROV bit.
5	FDTI	**Frame Detect Interrupt**. 0 = Frame detect is established on the communications link. 1 = This bit is set when the communications link does not have frame lock. If the FDTM and INTE bits are set, a hardware interrupt occurs on the AOUT/$\overline{\text{INT}}$ pin. Once set, this bit must be written to a 0 to be cleared.
4	BTDI	**Billing Tone Detect Interrupt.** 0 = A billing tone has not occurred. 1 = A billing tone has been detected. If the BTDM and INTE bits are set, a hardware interrupt occurs on the AOUT/$\overline{\text{INT}}$ pin. This bit must be written to 0 to clear it.
3	DODI	**Drop Out Detect Interrupt**. 0 = The line-side power supply has not collapsed. 1 = The line-side power supply has collapsed (The DOD bit in Register 19 has fired). If the DODM and INTE bits are set, a hardware interrupt occurs on the AOUT/$\overline{\text{INT}}$ pin. This bit must be written to 0 to be cleared. This bit should be cleared after clearing the PDL bit (Register 6) because powering as the line-side device can cause this interrupt to be triggered.
2	LCSOI	**Loop Current Sense Overload Interrupt**. 0 = The LCS bits have not reached max value (all ones). 1 = The LCS bits have reached max value. If the LCSOM bit (Register 3) and the INTE bit are set, a hardware interrupt occurs on the AOUT/$\overline{\text{INT}}$ pin. This bit must be written to 0 to be cleared. LCSOI does not necessarily imply that an overcurrent situation has occurred. An overcurrent situation in the DAA is determined by the status of the OPD bit (Register 19). After the LCSOI interrupt fires, the OPD bit should be checked to determine if an overcurrent situation exists.

Bit	Name	Function
1	DLCSI	Delta Loop Current Sense Interrupt 0 = The LCS bits have not changed value. 1 = The LCS bits have changed value; a hardware interrupt occurs on the AOUT/$\overline{\text{INT}}$ pin. This bit must be written to a 0 to be cleared.
0	POLI	Polarity Reversal Detect Interrupt. 0 = Bit 7 of the LVS register does not change states. 1 = Bit 7 of the LVS register changes from a 0 to a 1, or from a 1 to a 0, indicating the polarity of TIP and RING is switched. If the POLM and INTE bits are set, a hardware interrupt occurs on the AOUT/$\overline{\text{INT}}$ pin. To clear the interrupt, write this bit to 0.

Register 5. DAA Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		RDTN	RDTP	OPOL	ONHM	RDT	OHE	OH
Type		R	R	R/W	R/W	R	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	RDTN	**Ring Detect Signal Negative.** 0 = No negative ring signal is occurring. 1 = A negative ring signal is occurring.
5	RDTP	**Ring Detect Signal Positive.** 0 = No positive ring signal is occurring. 1 = A positive ring signal is occurring.
4	OPOL	**Off-hook Polarity.** 0 = Off-hook pin is active low. 1 = Off-hook pin is active high.
3	ONHM	**On-Hook Line Monitor.** 0 = Normal on-hook mode. 1 = Enables low-power on-hook monitoring mode allowing the host to receive line activity without going off-hook. This mode is used for caller-ID detection.
2	RDT	**Ring Detect.** 0 = Reset either 5 seconds after last positive ring is detected or when the system executes an off-hook. Only a positive ring sets this bit when RFWE = 0. When RFWE = 1, either a positive or negative ring sets this bit. 1 = Indicates a ring is occurring.
1	OHE	**Off-hook Pin Enable.** 0 = Off-hook pin is ignored. 1 = Enables operation of the off-hook pin.
0	OH	**Off-Hook.** 0 = Line-side device on-hook. 1 = Causes the line-side device to go off-hook. This bit operates independently of the OHE bit and is a logic OR with the off-hook pin when enabled.

Register 6. DAA Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				PDL	PDN			
Type				R/W	R/W			

Reset settings = 0001_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	PDL	**Powerdown Line-Side Device.** 0 = Normal operation. Program the clock generator before clearing this bit. 1 = Places the line-side device in lower power mode.
3	PDN	**Powerdown System-Side Device.** 0 = Normal operation. 1 = Powers down the system-side device. A pulse on $\overline{\text{RESET}}$ is required to restore normal operation.
2:0	Reserved	Read returns zero.

Register 7. Sample Rate Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						SRC[3:0]		
Type						R/W		

Reset settings = 0000_0000

Bit	Name	Function
7:4	Reserved	Read returns zero.
3:0	SRC[3:0]	**Sample Rate Control.** Sets the sample rate of the line-side device. 0000 = 7200 Hz 0001 = 8000 Hz 0010 = 8229 Hz 0011 = 8400 Hz 0100 = 9000 Hz 0101 = 9600 Hz 0110 = 10286 Hz 0111 = 12000 Hz 1000 = 13714 Hz 1001 = 16000 Hz 1010–1111 = Reserved

Register 8. PLL Divide N

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N[7:0]							
Type	R/W							

Reset settings = 0000_0000 (serial mode 0, 1)

Reset settings = 0001_0011 (serial mode 2)

Bit	Name	Function
7:0	N[7:0]	**PLL N Divider.** Contains the (value –1) for determining the output frequency on PLL1.

Register 9. PLL Divide M

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	M[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	M[7:0]	**PLL M Divider.** Contains the (value –1) for determining the output frequency on PLL1.

Register 10. DAA Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								DDL
Type								R/W

Reset settings = 0000_0000

Bit	Name	Function
7:1	Reserved	Read returns zero.
0	DDL	Digital Data Loopback. 0 = Normal operation. 1 = Audio data received on SDI and loops it back out to SDO before the TX and RX filters. Outputted data is identical to inputted data.

Register 11. System-Side and Line-Side Device Revision

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LSID[3:0]				REVA[3:0]			
Type	R				R			

Reset settings = xxxx_xxxx

Bit	Name	Function
7:4	LSID[3:0]	**Line-Side ID Bits.** These four bits will always read one of the following values depending on which line-side device is used. LSID[3:0] Si3018 0001 Si3019 0011 Si3010 0101
3:0	REVA[3:0]	**System-Side Revision.** Four-bit value indicating the revision of the system-side device.

Register 12. Line-Side Device Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		FDT		LCS[4:0]				
Type	R			R				

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	FDT	**Frame Detect.** 0 = Indicates the communications link has not established frame lock. 1 = Indicates the communications link frame lock is established.
5	Reserved	Read returns zero.
4:0	LCS[4:0]	**Loop Current Sense.** 5-bit value returning the loop current when the DAA is in an off-hook state. 00000 = Loop current is less than required for normal operation. 00100 = Minimum loop current for normal operation. 11111 = Loop current is >127 mA, and a current overload condition may exist.

Register 13. Line-Side Device Revision

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		0	REVB[3:0]					
Type	R							

Reset settings = xxxx_xxxx

Bit	Name	Function
7	Reserved	Read returns zero.
6	0	This bit always reads a zero.
5:2	REVB[3:0]	**Line-Side Device Revision.** Four-bit value indicating the revision of the line-side device.
1:0	Reserved	Read returns zero.

Register 14. Serial Interface Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NSLV[2:0]			SSEL[1:0]		FSD	RPOL	DCE
Type	R/W			R/W		R/W	R/W	R/W

Reset settings = 0000_0000 (serial mode 0,1)

Reset settings = 0011_1101 (serial mode 2)

Bit	Name	Function
7:5	NSLV[2:0]	**Number of Slaves devices.** 000 = 0 slaves. Redefines the FC/$\overline{\text{RGDT}}$ and $\overline{\text{RGDT}}$/FSD pins. 001 = 1 slave device 010 = 2 slave devices 011 = 3 slave devices 100 = 4 slave devices (For four or more slave devices, the FSD bit *MUST* be set.) 101 = 5 slave devices 110 = 6 slave devices 111 = 7 slave devices
4:3	SSEL[1:0]	**Slave device select.** 00 = 16-bit SDO receive data 01 = Reserved 10 = 15-bit SDO receive data, LSB = 1 11 = 15-bit SDO receive data, LSB = 0
2	FSD	**Delayed Frame Sync Control.** 0 = Sets the number of SCLK periods between frame syncs to 32. 1 = Sets the number of SCLK periods between frame syncs to 16. This bit *MUST* be set when Si3056 devices are slaves. For the master Si3056, only serial mode 1 is allowed when this bit is set.
1	RPOL	**Ring Detect Polarity.** 0 = The FC/$\overline{\text{RGDT}}$ pin (operating as ring detect) is active low. 1 = The FC/$\overline{\text{RGDT}}$ pin (operating as ring detect) is active high.
0	DCE	**Daisy-Chain Enable.** 0 = Daisy-chaining disabled. 1 = Enables the Si3056 to operate with slave devices on the same serial bus. The FC/$\overline{\text{RGDT}}$ signal (pin 7) becomes the ring detect output and the $\overline{\text{RDGT}}$/FSD signal (pin 15) becomes the delayed frame sync signal. *ALL* other bits in this register are ignored if DCE = 0.

Register 15. TX/RX Gain Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXM	ATX[2:0]			RXM	ARX[2:0]		
Type	R/W	R/W			R/W	R/W		

Reset settings = 0000_0000

Bit	Name	Function
7	TXM	**Transmit Mute.** 0 = Transmit signal is not muted. 1 = Mutes the transmit signal.
6:4	ATX[2:0]	**Analog Transmit Attenuation.** 000 = 0 dB attenuation 001 = 3 dB attenuation 010 = 6 dB attenuation 011 = 9 dB attenuation 1xx = 12 dB attenuation **Note:** Write these bits to zero when using the finer resolution transmit and receive gain/attenuation registers 38–41 available only with the Si3019 line-side device.
3	RXM	**Receive Mute.** 0 = Receive signal is not muted. 1 = Mutes the receive signal.
2:0	ARX[2:0]	**Analog Receive Gain.** 000 = 0 dB gain 001 = 3 dB gain 010 = 6 dB gain 011 = 9 dB gain 1xx = 12 dB gain **Note:** Write these bits to zero when using the finer resolution transmit and receive gain/attenuation registers 38–41 available only with the Si3019 line-side device.

Register 16. International Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ACT2	OHS	ACT	IIRE			RZ	RT
Type	RW	R/W	R/W	R/W			R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	ACT2	**AC Termination Select 2 (Si3018 line-side device only).** Works with the ACT bit to select one of four ac terminations: **ACT2 ACT AC Termination** 0 0 Real, 600 Ω 0 1 Global complex impedance 1 0 Global complex impedance, except New Zealand 1 1 New Zealand complex impedance The global complex impedance meets minimum return loss requirements in countries that require a complex ac termination. For improved return loss performance, the other complex impedances can be used.
6	OHS	**On-Hook Speed.** This bit, in combination with the OHS2 bit (Register 31) and the SQ[1:0] bits (Register 59), sets the amount of time for the line-side device to go on-hook. The on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **OHS OHS2 SQ[1:0] Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms ±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec)
5	ACT	**AC Termination Select. (Si3018 line-side device only).** When the ACT2 bit is cleared, the ACT bit selects the following: 0 = Selects the real ac impedance (600 Ω) 1 = Selects the global complex impedance.
4	IIRE	**IIR Filter Enable.** 0 = FIR filter enabled for transmit and receive filters. See Figures 7–10 on page 16. 1 = IIR filter enabled for transmit and receive filters. See Figures 11–16 on page 17.
3:2	Reserved	Read returns zero.
1	RZ	**Ringer Impedance.** 0 = Maximum (high) ringer impedance. 1 = Synthesized ringer impedance enabled. See "5.16.Ringer Impedance and Threshold" on page 30.
0	RT	**Ringer Threshold Select.** This bit is used to satisfy country requirements on ring detection. Signals below the lower level do not generate a ring detection; signals above the upper level are guaranteed to generate a ring detection. **RT RT Lower level RT Upper level** 0 13.5 V_{rms} 16.5 V_{rms} 1 19.35 V_{rms} 23.65 V_{rms}

Register 17. International Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CALZ	MCAL	CALD		OPE	BTE	ROV	BTD
Type	R/W	R/W	R/W		R/W	R/W	R/W	R

Reset settings = 0000_0000

Bit	Name	Function
7	CALZ	**Clear ADC Calibration.** 0 = Normal operation. 1 = Clears the existing calibration data. This bit must be written back to 0 after being set.
6	MCAL	**Manual ADC Calibration.** 0 = No calibration. 1 = Initiate manual ADC calibration.
5	CALD	**ADC Auto-Calibration Disable.** 0 = Enable auto-calibration. 1 = Disable auto-calibration.
4	Reserved	Read returns zero.
3	OPE	**Overload Protect Enable.** 0 = Disabled. 1 = Enabled. The OPE bit should always be cleared before going off-hook.
2	BTE	**Billing Tone Detect Enable.** When set, the DAA can detect a billing tone signal on the line and maintain on off-hook state through the billing tone. If a billing tone is detected, the BTD bit (Register 17) is set to indicate the event. Writing this bit to zero clears the BTD bit. 0 = Billing tone detection disabled. The BDT bit is not function. 1 = Billing tone detection enabled. The BDT is functional.
1	ROV	**Receive Overload.** This bit is set when the receive input has an excessive input level (i.e., receive pin goes below ground). Writing a zero to this location clears this bit and the ROVI bit (Register 4, bit 6). 0 = Normal receive input level. 1 = Excessive receive input level.
0	BTD	**Billing Tone Detected.** This bit is set if a billing tone is detected. Writing a zero to BTE clears this bit. 0 = No billing tone detected. 1 = Billing tone detected.

Register 18. International Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							RFWE	
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:2	Reserved	Read returns zero or one.
1	RFWE	**Ring Detector Full-Wave Rectifier Enable.** When RNGV (Register 24) is disabled, this bit controls the ring detector mode and the assertion of the RGDT pin. When RNGV is enabled, this bit configures the RGDT pin to either follow the ringing signal detected by the ring validation circuit, or to follow an unqualified ring detect one-shot signal initiated by a ring-threshold crossing and terminated by a fixed counter time-out of approximately five seconds. **RNGV** **RFWE** **RGDT** 0 0 Half-Wave 0 1 Full-Wave 1 0 Validated Ring Envelope 1 1 Ring Threshold Crossing One-Shot
0	Reserved	Read returns zero or one.

Register 19. International Control 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						OVL	DOD	OPD
Type						R	R	R

Reset settings = 0000_0000

Bit	Name	Function
7:3	Reserved	Read returns zero.
2	OVL	**Receive Overload Detect.** This bit has the same function as ROV in Register 17, but clears itself after the overload is removed. See "5.18.Billing Tone Protection and Receive Overload" on page 31. This bit is only masked by the off-hook counter and is not affected by the BTE bit. 0 = Normal receive input level. 1 = Excessive receive input level.
1	DOD	**Recal/Dropout Detect.** When the line-side device is off-hook, it is powered from the line itself. This bit will read 1 when loop current is not flowing. For example, if the line-derived power supply collapses, such as when the line is disconnected, this bit is set to 1. Additionally, when on-hook and the line-side device is enabled, this bit is set to 1. 0 = Normal operation. 1 = Line supply dropout detected when off-hook.
0	OPD	**Overload Protection Detect.** This bit is used to indicate that the DAA has detected a loop current overload. The detector firing threshold depends on the setting of the ILIM bit (Register 26). **OPD** **ILIM** **Overcurrent Threshold** **Overcurrent Status** 0 0 160 mA No overcurrent condition exists 0 1 60 mA No overcurrent condition exists 1 0 160 mA An overcurrent condition has been detected 1 1 60 mA An overcurrent condition has been detected

Register 20. Call Progress Receive Attenuation

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ARM[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	ARM[7:0]	**AOUT Receive Path Attenuation.** When decremented from the default setting, these bits linearly attenuate the AOUT receive path signal used for call progress monitoring. Setting the bits to all 0s mutes the AOUT receive path. Attenuation = 20 log(ARM[7:0]/64) 1111_1111 = +12 dB (gain) 0111_1111 = +6 dB (gain) 0100_0000 = 0 dB 0010_0000 = –6 dB (attenuation) 0001_0000 = –12 dB . . . 0000_0000 = Mute

Register 21. Call Progress Transmit Attenuation

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ATM[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	ATM[7:0]	**AOUT Transmit Path Attenuation.** When decremented from the default settings, these bits linearly attenuate the AOUT transmit path signal used for call progress monitoring. Setting the bits to all 0s mutes the AOUT transmit path. Attenuation = 20 log(ATM[7:0]/64) 1111_1111 = +12 dB (gain) 0111_1111 = +6 dB (gain) 0100_0000 = 0 dB 0010_0000 = –6 dB (attenuation) 0001_0000 = –12 dB . . . 0000_0000 = Mute

Register 22. Ring Validation Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDLY[1:0]		RMX[5:0]					
Type	R/W		R/W					

Reset settings = 1001_0110

Bit	Name	Function
7:6	RDLY[1:0]	**Ring Delay Bits 1 and 0.** These bits, in combination with the RDLY[2] bit (Register 23), set the amount of time between when a ring signal is validated and when a valid ring signal is indicated. **RDLY[2] RDLY[1:0] Delay** 0 00 0 ms 0 01 256 ms 0 10 512 ms . . . 1 11 1792 ms
5:0	RMX[5:0]	**Ring Assertion Maximum Count.** These bits set the maximum ring frequency for a valid ring signal within a 10% margin of error. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. When a subsequent TIP/RING event occurs, the timer value is compared to the RMX[5:0] field and if it exceeds the value in RMX[5:0] then the frequency of the ring is too high and the ring is invalidated. The difference between RAS[5:0] and RMX[5:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/ (2 x 20 Hz) = 25 ms. To calculate the correct RMX[5:0] value for a frequency range [f_min, f_max], the following equation should be used: $RMX[5:0] \geq RAS[5:0] - \frac{1}{2 \times f\_max \times 2\ ms}, RMX \leq RAS$ To compensate for error margin and ensure a sufficient ring detection window, it is recommended that the calculated value of RMX[5:0] be incremented by 1.

Register 23. Ring Validation Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDLY[2]	RTO[3:0]				RCC[2:0]		
Type	R/W	R/W				R/W		

Reset settings = 0010_1101

Bit	Name	Function
7	RDLY[2]	**Ring Delay Bit 2.** This bit, in combination with the RDLY[1:0] bits (Register 22), set the amount of time between when a ring signal is validated and when a valid ring signal is indicated. **RDLY[2] RDLY[1:0] Delay** 0 00 0 ms 0 01 256 ms 0 10 512 ms . . . 1 11 1792 ms
6:3	RTO[3:0]	**Ring Timeout.** These bits set when a ring signal is determined to be over after the most recent ring threshold crossing. **RTO[3:0] Ring Timeout** 0000 80 ms 0001 128 ms 0010 256 ms . . . 1111 1920 ms
2:0	RCC[2:0]	**Ring Confirmation Count.** These bits set the amount of time that the ring frequency must be within the tolerances set by the RAS[5:0] bits and the RMX[5:0] bits to be classified as a valid ring signal. **RCC[2:0] Ring Confirmation Count Time** 000 100 ms 001 150 ms 010 200 ms 011 256 ms 100 384 ms 101 512 ms 110 640 ms 111 1024 ms

Register 24. Ring Validation Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RNGV		RAS[5:0]					
Type	R/W	R	R/W					

Reset settings = 0001_1001

Bit	Name	Function
7	RNGV	**Ring Validation Enable.** 0 = Ring validation feature is disabled. 1 = Ring validation feature is enabled in both normal operating mode and low-power mode.
6	Reserved	Reserved and may read either a 1 or 0.
5:0	RAS[5:0]	**Ring Assertion Time.** These bits set the minimum ring frequency for a valid ring signal within a 10% margin of error. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. When a subsequent TIP/RING event occurs, the timer value is compared to the RMX[5:0] field and if it exceeds the value in RMX[5:0] then the frequency of the ring is too high and the ring is invalidated. The difference between RAS[5:0] and RMX[5:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/ (2 x 20 Hz) = 25 ms. To calculate the correct RMX[5:0] value for a frequency range [f_min, f_max], the following equation should be used: $$RMX[5:0] \geq RAS[5:0] - \frac{1}{2 \times f\_min \times 2\ ms}, RMX \leq RAS$$ To compensate for error margin and ensure a sufficient ring detection window, it is recommended that the calculated value of RMX[5:0] be incremented by 1.

Register 25. Resistor Calibration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RCALS	RCALM	RCALD		RCAL[3:0]			
Type	R	R/W	R/W	R	R/W			

Reset settings = xx0x_xxxx

Bit	Name	Function
7	RCALS	**Resistor Auto Calibration.** 0 = Resistor calibration is not in progress. 1 = Resistor calibration is in progress.
6	RCALM	**Manual Resistor Calibration.** 0 = No calibration. 1 = Initiate manual resistor calibration. (After a manual calibration has been initiated, this bit must be cleared within 1 ms.)
5	RCALD	**Resistor Calibration Disable.** 0 = Internal resistor calibration enabled. 1 = Internal resistor calibration disabled.
4	Reserved	Do not write to this register bit. This bit always reads a zero.
3:0	RCAL[3:0]	Always write back the value read.

Register 26. DC Termination Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DCV[1:0]		MINI[1:0]				ILIM	DCR
Type	R/W		R/W				R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7:6	DCV[1:0]	**TIP/RING Voltage Adjust.** Adjust the voltage on the DCT pin of the line-side device, which affects the TIP/RING voltage on the line. Low voltage countries should use a lower TIP/RING voltage. Raising the TIP/RING voltage improves signal headroom. **DCV[1:0] DCT Pin Voltage** 00 3.1 V 01 3.2 V 10 3.35 V 11 3.5 V
5:4	MINI[1:0]	**Minimum Operational Loop Current.** Adjusts the minimum loop current so the DAA can operate. Increasing the minimum operational loop current improves signal headroom at a lower TIP/RING voltage. **MINI[1:0] Min Loop Current** 00 10 mA 01 12 mA 10 14 mA 11 16 mA
3:2	Reserved	Do not write to these register bits.
1	ILIM	**Current Limiting Enable.** 0 = Current limiting mode disabled. 1 = Current limiting mode enabled. Limits loop current to a maximum of 60 mA per the TBR21 standard.
0	DCR	**DC Impedance Selection.** 0 = 50 Ω dc termination is selected. Use this mode for all standard applications. 1 = 800 Ω dc termination is selected.

Register 27. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	Reserved	Do not read or write.

Register 28. Loop Current Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LCS2[7:0]							
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:0	LCS2[7:0]	**Loop Current Status.** Eight-bit value returning the loop current. Each bit represents 1.1 mA of loop current. 0000_0000 = Loop current is less than required for normal operation.

Register 29. Line Voltage Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LVS[7:0]							
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:0	LVS[7:0]	**Line Voltage Status.** Eight-bit value returning the loop voltage. Each bit represents 1 V of loop voltage. This register operates in on-hook and off-hook modes. Bit seven of this register indicates the polarity of the TIP/RING voltage. When this bit changes state, it indicates that a polarity reversal has occurred. The value returned is represented in 2s compliment format. 0000_0000 = No line is connected.

Register 30. AC Termination Control (Si3019 line-side device only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				FULL2	ACIM[3:0]			
Type	R/W				R/W			

Reset settings = 0000_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	FULL2	**Enhanced Full Scale (2X) Transmit and Receive Mode (line-side Revision E or later).** 0 = Default 1 = Transmit/Receive 2X Full Scale This bit changes the full scale of the ADC and DAC from 0 min to +6 dBm into 600 Ω load (or 1.5 dBV into all reference impedances). When this bit is set, the DCV[1:0] bits (Register 26) should be set to all 1s to avoid distortion at low loop currents.
3:0	ACIM[3:0]	**AC Impedance Selection (Si3019 line-side device only).** The off-hook ac termination is selected from the following: 0000 = 600 Ω 0001 = 900 Ω 0010 = 270 Ω + (750 Ω || 150 nF) (TBR21) and 275 Ω + (780 Ω || 150 nF) 0011 = 220 Ω + (820 Ω || 120 nF) (Australia/New Zealand) and 220 Ω + (820 Ω || 115 nF) (Slovakia/Slovenia/South Africa/Germany/Austria/Bulgaria) 0100 = 370 Ω + (620 Ω || 310 nF) (New Zealand #2/India) 0101 = 320 Ω + (1050 Ω || 230 nF) (England) 0110 = 370 Ω + (820 Ω || 110 nF) 0111 = 275 Ω + (780 Ω || 115 nF) 1000 = 120 Ω + (820 Ω || 110 nF) 1001 = 350 Ω + (1000 Ω || 210 nF) 1010 = 0 Ω + (900 Ω || 30 nF) (line-side Revision C or earlier) 1010 = 200 Ω + (680 Ω || 100 nF) (China) (line-side Revision E or later) 1011 = 600 Ω + 2.16 µF 1100 = 900 Ω + 1 µF 1101 = 900 Ω + 2.16 µF 1110 = 600 Ω + 1 µF 1111 = Global impedance

Register 31. DAA Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FULL	FOH[1:0]			OHS2		FILT	LVFD
Type	R/W	R/W			R/W		R/W	R/W

Reset settings = 0010_0000

Bit	Name	Function
7	FULL	**Full Scale Transmit and Receive Mode (Si3019 line-side device only).** 0 = Default. 1 = Transmit/receive full scale. This bit changes the full scale of the ADC and DAC from 0 min to +3.2 dBm into a 600 Ω load (or 1 dBV into all reference impedances). When this bit is set, the DCV[1:0] bits (Register 26) should be set to all 1s to avoid distortion at low loop currents.
6:5	FOH[1:0]	**Fast Off-Hook Selection.** These bits determine the length of the off-hook counter. The default setting is 128 ms. 00 = 512 ms. 01 = 128 ms. 10 = 64 ms. 11 = 8 ms.
4	Reserved	Read returns zero.
3	OHS2	**On-Hook Speed 2.** This bit, in combination with the OHS bit (Register 16) and the SQ[1:0] bits on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **OHS** **OHS2** **SQ[1:0]** **Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms ±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec)
2	Reserved	Read returns zero.
1	FILT	**Filter Pole Selection (Si3019 line-side device only).** 0 = The receive path has a low –3 dBFS corner at 5 Hz. 1 = The receive path has a low –3 dBFS corner at 200 Hz.
0	LVFD	**Line Voltage Force Disable (Si3019 line-side device only).** 0 = Normal operation. 1 = The circuitry that forces the LVS register (Register 29) to all 0s at 3 V or less is disabled. The LVS register may display unpredictable values at voltages between 0 to 2 V. All 0s are displayed if the line voltage is 0 V.

Register 32-37. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

Register 38. TX Gain Control 2 (Si3019 Line-Side Device Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				TGA2	TXG2[3:0]			
Type				R/W	R/W			

Reset settings = 0000_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	TGA2	**Transmit Gain or Attenuation 2.** 0 = Incrementing the TXG2[3:0] bits results in gaining up the transmit path. 1 = Incrementing the TXG2[3:0] bits results in attenuating the transmit path.
3:0	TXG2[3:0]	**Transmit Gain 2.** Each bit increment represents 1 dB of gain or attenuation, up to a maximum of +12 dB and –15 dB respectively. For example: **TGA2 TXG2[3:0] Result** X 0000 0 dB gain or attenuation is applied to the transmit path. 0 0001 1 dB gain is applied to the transmit path. 0 : 0 11xx 12 dB gain is applied to the transmit path. 1 0001 1 dB attenuation is applied to the transmit path. 1 : 1 1111 15 dB attenuation is applied to the transmit path.

Register 39. RX Gain Control 2 (Si3019 Line-Side Device Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				RGA2	RXG2[3:0]			
Type	R/W				R/W			

Reset settings = 0000_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	RGA2	**Receive Gain or Attenuation 2.** 0 = Incrementing the RXG2[3:0] bits results in gaining up the receive path. 1 = Incrementing the RXG2[3:0] bits results in attenuating the receive path.
3:0	RXG2[3:0]	**Receive Gain 2.** Each bit increment represents 1 dB of gain or attenuation, up to a maximum of +12 dB and –15 dB respectively. For example: **RGA2** **RXG2[3:0]** **Result** X 0000 0 dB gain or attenuation is applied to the receive path. 0 0001 1 dB gain is applied to the receive path. 0 : 0 11xx 12 dB gain is applied to the receive path. 1 0001 1 dB attenuation is applied to the receive path. 1 : 1 1111 15 dB attenuation is applied to the receive path.

Register 40. TX Gain Control 3 (Si3019 Line-Side Device Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				TGA3	TXG3[3:0]			
Type	R/W				R/W			

Reset settings = 0000_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	TGA3	**Transmit Gain or Attenuation 3.** 0 = Incrementing the TXG3[3:0] bits results in gaining up the transmit path. 1 = Incrementing the TXG3[3:0] bits results in attenuating the transmit path.
3:0	TXG3[3:0]	**Transmit Gain 3.** Each bit increment represents 0.1 dB of gain or attenuation, up to a maximum of 1.5 dB. For example: **TGA3** **TXG3[3:0]** **Result** X 0000 0 dB gain or attenuation is applied to the transmit path. 0 0001 0.1 dB gain is applied to the transmit path. 0 : 0 1111 1.5 dB gain is applied to the transmit path. 1 0001 0.1 dB attenuation is applied to the transmit path. 1 : 1 1111 1.5 dB attenuation is applied to the transmit path.

Register 41. RX Gain Control 3 (Si3019 Line-Side Device Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				RGA3	RXG3[3:0]			
Type	R/W				R/W			

Reset settings = 0000_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	RGA3	**Receive Gain or Attenuation 2.** 0 = Incrementing the RXG3[3:0] bits results in gaining up the receive path. 1 = Incrementing the RXG3[3:0] bits results in attenuating the receive path.
3:0	RXG3[3:0]	**Receive Gain 3.** Each bit increment represents 0.1 dB of gain or attenuation, up to a maximum of 1.5 dB. For example: **RGA3 RXG3[3:0] Result** X 0000 0 dB gain or attenuation is applied to the receive path. 0 0001 0.1 dB gain is applied to the receive path. 0 : 0 1111 1.5 dB gain is applied to the receive path. 1 0001 0.1 dB attenuation is applied to the receive path. 1 : 1 1111 1.5 dB attenuation is applied to the receive path.

Register 42. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

Register 43. Line Current/Voltage Threshold Interrupt (Si3019 Line-Side Device Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CVT[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	CVT[7:0]	**Current/Voltage Threshold.** Determines the threshold at which an interrupt is generated from either the LCS or LVS register. Generate this interrupt to occur when the line current or line voltage rises above or drops below the value in the CVT[7:0] register.

Register 44. Line Current/Voltage Threshold Interrupt Control (Si3019 Line-Side Device Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					CVI	CVS	CVM	CVP
Type					R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7:4	Reserved	Read returns zero.
3	CVI	**Current/Voltage Interrupt.** 0 = The current / voltage threshold has not been crossed. 1 = The current / voltage threshold is crossed. If the CVM and INTE bits are set, a hardware interrupt occurs on the AOUT/$\overline{\text{INT}}$ pin. Once set, this bit must be written to 0 to be cleared.
2	CVS	**Current/Voltage Select.** 0 = The line current shown in the LCS2 register generates an interrupt. 1 = The line voltage shown in the LVS register generates an interrupt.
1	CVM	**Current/Voltage Interrupt Mask.** 0 = The current / voltage threshold being triggered does not cause a hardware interrupt on the AOUT/$\overline{\text{INT}}$ pin. 1 = The current / voltage threshold being triggered causes a hardware interrupt on the AOUT/$\overline{\text{INT}}$ pin.
0	CVP	**Current/Voltage Interrupt Polarity.** 0 = The current / voltage threshold is triggered by the absolute value of the number in either the LCS2 or LVS register falling below the value in the CVT[7:0] register. 1 = The current / voltage threshold is triggered by the absolute value of the number in the either the LCS2 or LVS register rising above the value in the CVT[7:0] Register.

Register 45. Programmable Hybrid Register 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB1 [7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB1[7:0]	**Programmable Hybrid Register 1.** These bits are programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the first tap in the 8-tap filter. When this register is set to all 0s, this filter stage does not effect on the hybrid response. See "5.13.Transhybrid Balance" on page 29 for more information on selecting coefficients for the programmable hybrid.

Register 46. Programmable Hybrid Register 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB2[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB2[7:0]	**Programmable Hybrid Register 2.** These bits are programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the second tap in the 8-tap filter. When this register is set to all 0s, this filter stage does not effect on the hybrid response. See "5.13.Transhybrid Balance" on page 29 for more information on selecting coefficients for the programmable hybrid.

Register 47. Programmable Hybrid Register 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB3[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB3[7:0]	**Programmable Hybrid Register 3.** These bits are programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the third tap in the 8-tap filter. When this register is set to all 0s, this filter stage does not effect on the hybrid response. See "5.13.Transhybrid Balance" on page 29 for more information on selecting coefficients for the programmable hybrid.

Register 48. Programmable Hybrid Register 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB4[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB4[7:0]	**Programmable Hybrid Register 4.** These bits are programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the fourth tap in the 8-tap filter. When this register is set to all 0s, this filter stage does not effect on the hybrid response. See "5.13.Transhybrid Balance" on page 29 for more information on selecting coefficients for the programmable hybrid.

Register 49. Programmable Hybrid Register 5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB5[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB5[7:0]	**Programmable Hybrid Register 5.** These bits are programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the fifth tap in the 8-tap filter. When this register is set to all 0s, this filter stage does not effect on the hybrid response. See "5.13.Transhybrid Balance" on page 29 for more information on selecting coefficients for the programmable hybrid.

Register 50. Programmable Hybrid Register 6

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB6[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB6[7:0]	**Programmable Hybrid Register 6.** These bits are programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the sixth tap in the 8-tap filter. When this register is set to all 0s, this filter stage does not effect on the hybrid response. See"5.13.Transhybrid Balance" on page 29 for more information on selecting coefficients for the programmable hybrid.

Register 51. Programmable Hybrid Register 7

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB7[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB7[7:0]	**Programmable Hybrid Register 7.** These bits are programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the seventh tap in the 8-tap filter. When this register is set to all 0s, this filter stage does not effect on the hybrid response. See "5.13.Transhybrid Balance" on page 29 for more information on selecting coefficients for the programmable hybrid.

Register 52. Programmable Hybrid Register 8

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HYB8[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	HYB8[7:0]	**Programmable Hybrid Register 8.** These bits are programmed with a coefficient value to adjust the hybrid response to reduce near-end echo. This register represents the eighth tap in the 8-tap filter. When this register is set to all 0s, this filter stage does not effect on the hybrid response. See "5.13.Transhybrid Balance" on page 29 for more information on selecting coefficients for the programmable hybrid.

Register 53-58 Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	Reserved	Do not write to these register bits.

Register 59. Spark Quenching Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		SQ1		SQ0		RG1	GCE	
Type		R/W		R/W		R/W	R/W	

Reset settings = xxxx_xxxx

Bit	Name	Function
7	Reserved	Always write this bit to zero.
6	SQ1	**Spark Quenching.** This bit, in combination with the OHS bit (Register 16), and the OHS2 bit (Register 31), sets the amount of time for the line-side device to go on-hook. The on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **OHS** **OHS2** **SQ[1:0]** **Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms ±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec)
5	Reserved	Always write this bit to zero.
4	SQ0	**Spark Quenching.** This bit, in combination with the OHS bit (Register 16), and the OHS2 bit (Register 31), sets the amount of time for the line-side device to go on-hook. The on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **OHS** **OHS2** **SQ[1:0]** **Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms ±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec)
3	Reserved	Always write this bit to zero.
2	RG1	**Receive Gain 1 (Line-side Revision E or later).** This bit enables receive path gain adjustment. 0 = No gain applied to hybrid, full scale RX on line = 0 dBm. 1 = 1 dB of gain applied to hybrid, full scale RX on line = –1 dBm.
1	GCE	**Guarded Clear Enable (Line-side Revision E or later).** This bit (in conjunction with the R2 bit set to 1), enables the Si3056 to meet BT's Guarded Clear Spec (B5 6450, Part 1: 1993, Section 15.4.3.3). With these bits set, the DAA will draw approximately 2.5 mA of current from the line while on-hook. 0 = default, DAA does not draw loop current. 1 = Guarded Clear enabled, DAA draws 2.5 mA while on-hook to meet Guarded Clear requirement.
0	Reserved	Always write this bit to zero.

APPENDIX—UL1950 3RD EDITION

Although designs using the Si3056 comply with the UL1950 3rd edition and pass all overcurrent and overvoltage tests, there are still several issues to consider.

Figure 37 shows two designs that can pass the UL1950 overvoltage tests and electromagnetic emissions. The top schematic shows the configuration in which the ferrite beads (FB1 and FB2) are on the unprotected side of the sidactor (RV1). For this configuration, the current rating of the ferrite beads needs to be 6 A. However, the higher current ferrite beads are less effective in reducing electromagnetic emissions.

The bottom schematic of Figure 37 shows the configuration in which the ferrite beads (FB1 and FB2) are on the protected side of the sidactor (RV1). For this design, the ferrite beads can be rated at 200 mA.

In a cost-optimized design, compliance to UL1950 does not always require overvoltage tests. Plan ahead to know which overvoltage tests apply to the system. System-level elements in the construction, such as fire enclosure and spacing requirements, need to be considered during the design stages. Consult with a professional testing agency during the design of the product to determine which tests apply to the system.

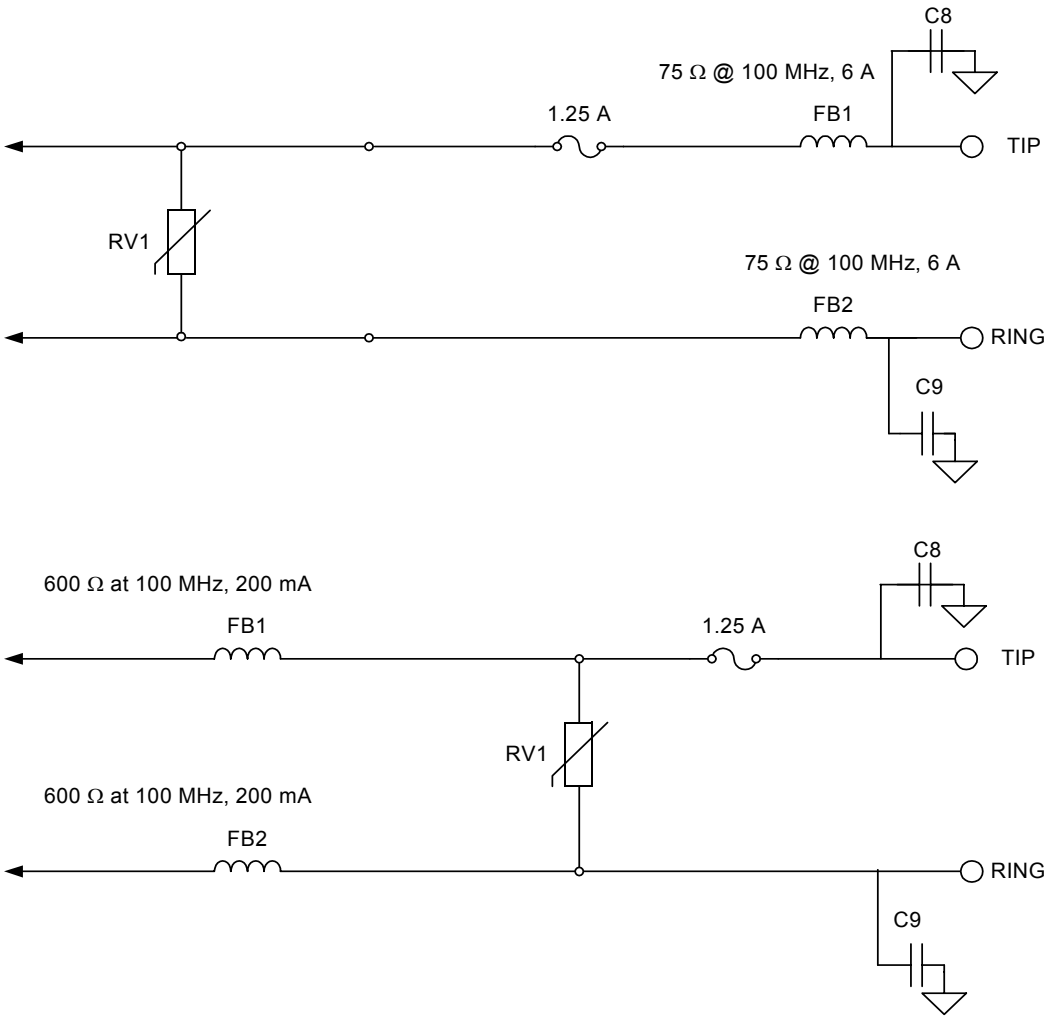


Figure 37. Circuits that Pass all UL1950 Overvoltage Tests

7. Pin Descriptions: Si3056

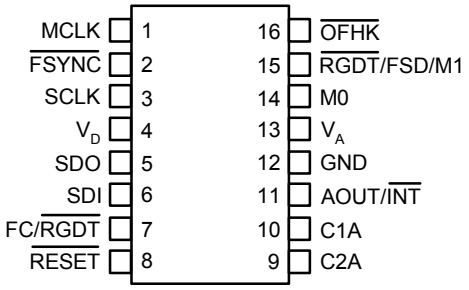


Table 24. Si3056 Pin Descriptions

Pin #	Pin Name	Description
1	MCLK	**Master Clock Input.** High speed master clock input. Generally supplied by the system crystal clock or modem/DSP.
2	$\overline{\text{FSYNC}}$	**Frame Sync Output.** Data framing signal that indicates the start and stop of a communication/data frame.
3	SCLK	**Serial Port Bit Clock Output.** Controls the serial data on SDO and latches the data on SDI.
4	V_D	**Digital Supply Voltage.** Provides the 3.3 V digital supply voltage to the Si3056.
5	SDO	**Serial Port Data Out.** Serial communication data that is provided by the Si3056 to the modem/DSP.
6	SDI	**Serial Port Data In.** Serial communication and control data that is generated by the modem/DSP and presented as an input to the Si3056.
7	FC/$\overline{\text{RGDT}}$	**Secondary Transfer Request Input/Ring Detect.** An optional signal to instruct the Si3056 that control data is being requested in a secondary frame. When daisy chain is enabled, this pin becomes the ring detect output. Produces an active low rectified version of the ring signal.
8	$\overline{\text{RESET}}$	**Reset Input.** An active low input that resets all control registers to a defined, initialized state. Also used to bring the Si3056 out of sleep mode.
9	C2A	**Isolation Capacitor 2A.** Connects to one side of the isolation capacitor C2. Used to communicate with the line-side device.
10	C1A	**Isolation Capacitor 1A.** Connects to one side of the isolation capacitor C1. Used to communicate with the line-side device.

Table 24. Si3056 Pin Descriptions (Continued)

Pin #	Pin Name	Description
11	AOUT/$\overline{\text{INT}}$	**Analog Speaker Out/Interrupt.** Provides an analog output signal for driving a call progress speaker or a hardware interrupt for multiple sources of interrupts.
12	GND	**Ground.** Connects to the system digital ground.
13	V_A	**Analog Supply Voltage.** Provides the analog supply voltage for the Si3056.
14	M0	**Mode Select 0.** The first of two mode select pins that selects the operation of the serial port/DSP interface.
15	$\overline{\text{RGDT}}$/FSD/M1	**Ring Detect/Delayed Frame Sync/Mode Select 1.** Output signal that indicates the status of a ring signal. Produces an active low rectified version of the ring signal. When daisy chain is enabled, this signal becomes a delayed frame sync to drive a slave device. It is also the second of two mode select pins that selects the operation of the serial port/DSP interface when RESET is deasserted.
16	$\overline{\text{OFHK}}$	**Off-Hook.** An active low input control signal that provides a termination across TIP and RING for line seizing and pulse dialing,

8. Pin Descriptions: Si3018/19/10

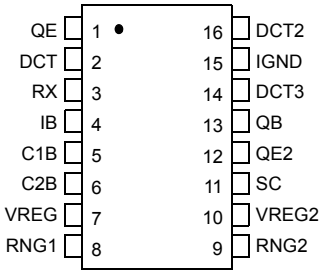


Table 25. Si3018/19/10 Pin Descriptions

Pin #	Pin Name	Description
1	QE	**Transistor Emitter.** Connects to the emitter of Q3.
2	DCT	**DC Termination.** Provides dc termination to the telephone network.
3	RX	**Receive Input.** Serves as the receive side input from the telephone network.
4	IB	**Isolation Capacitor 1B.** Connects to one side of isolation capacitor C1. Used to communicate with the system-side device.
5	C1B	**Internal Bias.** Provides internal bias.
6	C2B	**Isolation Capacitor 2B.** Connects to one side of the isolation capacitor C2. Used to communicate with the system-side device.
7	VREG	**Voltage Regulator.** Connects to an external capacitor to provide bypassing for an internal power supply.
8	RNG1	**Ring 1.** Connects through a resistor to the RING lead of the telephone line. Provides the ring and caller ID signals to the system-side device.
9	RNG2	**Ring 2.** Connects through a resistor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the system-side device.
10	VREG2	**Voltage Regulator 2.** Connects to an external capacitor to provide bypassing for an internal power supply.
11	SC	**Circuit Enable.** Enables transistor network. Should be tied through a 0 Ω resistor to I_{GND}.
12	QE2	**Transistor Emitter 2.** Connects to the emitter of transistor Q4.

Table 25. Si3018/19/10 Pin Descriptions (Continued)

Pin #	Pin Name	Description
13	QB	**Transistor Base.** Connects to the base of transistor Q4.
14	DCT3	**DC Termination 3.** Provides dc termination to the telephone network.
15	IGND	**Isolated Ground.** Connects to ground on the line-side interface.
16	DCT2	**DC Termination 2.** Provides dc termination to the telephone network.

9. Ordering Guide[1,2]

Chipset	Region	Interface	Digital (SOIC)	Line (SOIC)	Digital (TSSOP)	Line (TSSOP)	Temperature
Si3050/19	Enhanced Global	PCM/SPI or GCI		Si3019-KS	Si3050-KT	Si3019-KT	0 to 70 °C
Si3050/18	Global	PCM/SPI or GCI		Si3018-KS	Si3050-KT	Si3018-KT	0 to 70 °C
Si3056/18	Global	DSP Serial I/F	Si3056-KS	Si3018-KS		Si3018-KT	0 to 70 °C
Si3056/19	Enhanced Global	DSP Serial I/F	Si3056-KS	Si3019-KS		Si3019-KT	0 to 70 °C
Si3056/10	Low-Speed Global	DSP Serial I/F	Si3056-KS	Si3010-KS			0 to 70 °C
Si3050/19	Enhanced Global	PCM/SPI or GCI		Si3019-X-FS	Si3050-FT or Si3050-X-FT	Si3019-X-FT	0 to 70 °C
Si3050/18	Global	PCM/SPI or GCI		Si3018-X-FS		Si3018-X-FT	0 to 70 °C
Si3056/18	Global	DSP Serial I/F	Si3056-FS or Si3056-C-FS	Si3018-X-FS		Si3018-X-FT	0 to 70 °C
Si3056/19	Enhanced Global	DSP Serial I/F		Si3019-X-FS		Si3019-X-FT	0 to 70 °C
Si3056/10	Low-Speed Global	DSP Serial I/F		Si3010-X-FS			0 to 70 °C

Notes:

1. Many of the above devices are available in lead-free packages. For lead-free parts, the “K” in the part number suffix is replaced with an “F”.
2. The ordering part number for Silicon Labs devices may include the revision letter (example Si3056-D-KS, where D is the die revision letter). Refer to "12.Product Identification" on page 90 for more information on part naming conventions.

10. Evaluation Board Ordering Guide

Part Number	Line-Side Device	Platform	Intended Use	Includes Platform Board?	Includes DAA Daughter Card?
Si3056PPT-EVB	Si3018	Parallel Port	Direct Connection to a PC to use with included Windows®-based SW program.	Yes (PPT)	Yes
Si3056PPT1-EVB	Si3019	Parallel Port			
Si3056PPT2-EVB	Si3010	Parallel Port			
Si3056SSI-EVB	Si3018	Serial Interface with Buffer	Direct Connection to processor or DSP (in customer application or to another EVB).	Yes (SSI)	Yes
Si3056SSI1-EVB	Si3019	Serial Interface with Buffer			
Si3056SSI2-EVB	Si3010	Serial Interface with Buffer			
Si3056DC-EVB	Si3018	Daughtercard Only	Direct Connection to processor or DSP (in customer application).	No	Yes
Si3056DC1-EVB	Si3019	Daughtercard Only			
Si3056DC2-EVB	Si3010	Daughtercard Only			

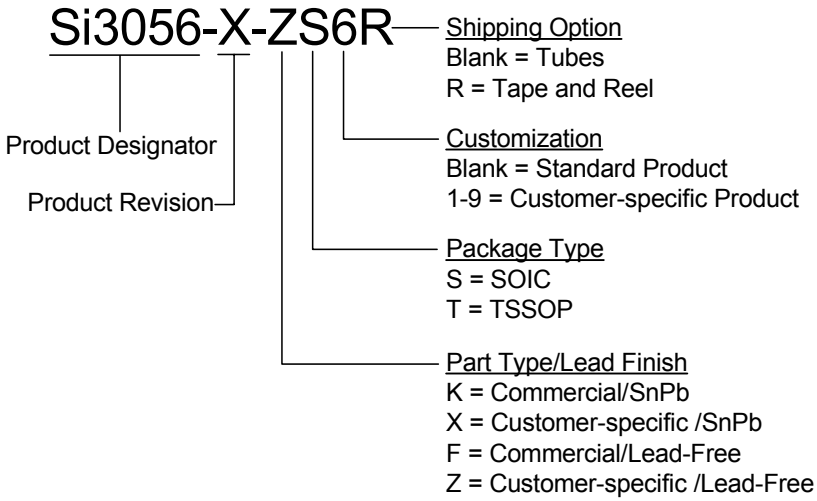
11. Product Selection and Identification Guide

Device	Finished Goods Part Number	Description	Marking
Si3056	Si3056-X-KS	Commercial part	FG Part #
Si3056	Si3056-X-FS	Commercial part, lead-free version	FG Part #
Si3056	Si3056-X-XS4	Customer-specific bond option	Custom
Si3056	Si3056-X-ZS4	Customer-specific bond option, lead-free version	Custom
Si3056	Si3056-X-XS5	Customer-specific bond option	Custom
Si3056	Si3056-X-ZS5	Customer-specific bond option, lead-free version	Custom
Si3056	Si3056-X-XS8	Customer-specific bond option	Custom
Si3056	Si3056-X-ZS4	Customer-specific bond option, lead-free version	Custom

12. Product Identification

The product identification number is a finished goods part number or is specified by a finished goods part number, such as a special customer part number.

Example:



13. Package Outline: 16-Pin SOIC

Figure 38 illustrates the package details for the Si3056/18/19/10. Table 26 lists the values for the dimensions shown in the illustration.

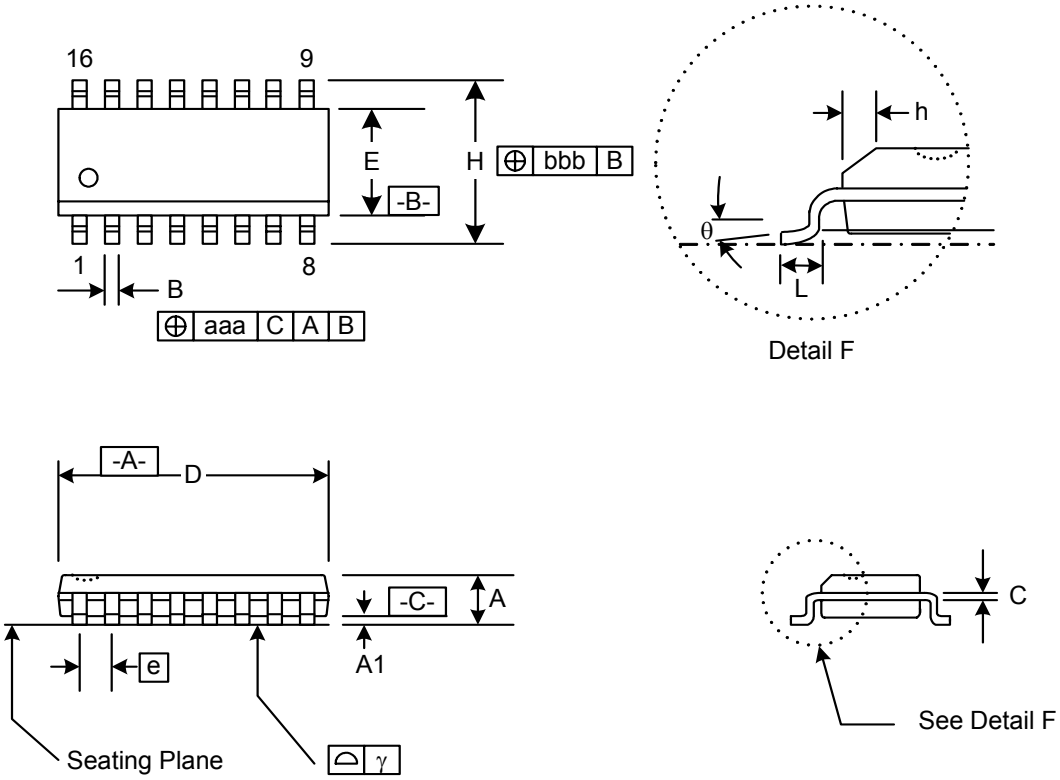


Figure 38. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 26. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	.10	.25
B	.33	.51
C	.19	.25
D	9.80	10.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	.25	.50
L	.40	1.27
γ	0.10	
θ	0º	8º
aaa	0.25	
bbb	0.25	

Document Change List

Revision 0.2 to Revision 0.71

- Updated list of applications on cover page, including ability to support V.92 modems.
- Updated Transmit Full Scale Level test condition and note in Table 4 (AC Characteristics) for description of VCID and DRCID.
- Updated specifications in Table 7, Table 8, and Table 9 (Switching Characteristics) and Figure 3, Figure 4, and Figure 5.
- Updated “3.Bill of Materials” with revised values for C3, (10% to 20% tolerance relaxation on same value cap) Q4-5 (voltage rating was misstated at 60 V, changed to correct 80 V value), R51-52 power rating relaxed from 1/10 W to 1/16 W, and updated recommended ferrite bead part numbers.
- Fixed several grammatical errors in functional descriptions, and globally replaced all instances of CTR21 with TBR21.
- Added new functional description “5.1.Upgrading from the Si3034/35/44 to Si3056” to describe new features and changes to consider when migrating to the Si3056.
- Updated “Power Supplies” functional description to reflect 5 V tolerance on Si3056 input pins.
- Updated “5.6.Transmit/Receive Full Scale Level (Si3019 Line-Side Only)” functional description.
- Updated“5.8.Line Voltage/Loop Current Sensing” functional description.
- Updated “5.15.Ring Validation” functional description.
- Updated “5.21.2.Type II Caller ID” functional description.
- Updated “5.23.Gain Control” functional description.
- Updated “5.26.Digital Interface” functional description and Figure 29.
- Updated “Power Management” functional description to qualify description to qualify wake-on-ring support in low-power sleep mode.
- Updated “5.30.In-Circuit Testing” functional description.
- Updated “5.6.Transmit/Receive Full Scale Level (Si3019 Line-Side Only)” functional description.
- Updated “5.8.1.Line Voltage Measurement” functional description.
- Updated “5.10.Interrupts” functional description.
- Updated “5.11.DC Termination” functional description.
- Updated “6.Control Registers” to reflect LVFD bit available exclusively with the Si3019 line-side.
- Updated the following bit descriptions:
  - R4.7
  - R12.4–0
  - R14.2
  - R17.4
  - R20-21
  - R28
  - R29
  - R31.0,3,7
  - R38–41
- Updated “Ordering Guide.”
- Added list of support documentation.

Revision 0.71 to Revision 1.0

- Added Si3010 to data sheet title, and to Line-Side device support functional description, and application circuit.
- Updated Tables 2, 3, & 4 based on production test results.
- Updated Table 4 with footnotes to explain expected DR and THD when using the Si3056 with the Si3010 low-speed line-side device.
- Updated BOM.
- Updated Country Specific Register Settings.
- Updated the following functional descriptions:
  - Line Voltage/Loop Current Sensing
  - Interrupts
  - DC Termination
  - Ring Detection
  - Ring Validation
  - Ringer Impedance and Threshold
  - Caller ID
  - Overload Detection
  - Gain Control (added diagram)
  - Power Management
  - Revision Identification
- Updated Register Summary
- Updated the following Register Descriptions
  - Register 1 bit 1
  - Register 3 bit 1 (added bit description)
  - Register 4 bit 1 (added bit description)
  - Register 5 bit 2
  - Register 12 bits 4:0
  - Register 13 bit 6
  - Register 16 bit 0
  - Register 18 bit 1
  - Register 19 bit 1
  - Register 24 bits 5:0
  - Register 31 bit 7
- Updated ordering guide
- Added Evaluation Board ordering guide

Revision 1.0 to Revision 1.01

- Removed “Confidential” watermark.

Revision 1.01 to Revision 1.02

- Updated Table 2, “Loop Characteristics,” on page 6.
- Updated Table 4, “AC Characteristics,” on page 8
- Updated "3.Bill of Materials" on page 19
  - Added optional caller ID circuit components in footnotes.
  - Removed R14.
- Updated Line Voltage/Loop Current Sensing functional description.
- Updated "9.Ordering Guide[1,2]" on page 88.
- Updated "13.Package Outline: 16-Pin SOIC" on page 91.
- Updated Table 26, “Package Diagram Dimensions,” on page 91.

Revision 1.02 to Revision 1.03

- Updated Table 4 on page 8.
- Updated Table 6 on page 10 to add MCLK jitter tolerance.
- Added Table 10 on page 14.
- Updated Table 13 on page 20.
- Updated Table 15 on page 23.
  - Changed recommended country settings for Australia, Austria, Bahrain, Bulgaria, China, Croatia, Cyprus, Czech Republic, Egypt, Germany, Hungary, Israel, India, Japan, Jordan, Kazakhstan, Latvia, Lebanon, Malyasia, Malta, Morocco, Nigeria, Oman, Pakistan, Philippines, Poland, Romania, Russia, Slovakia, Slovenia, South Africa, South Korea, Syria, Taiwan, Thailand.
- Updated Table 18 on page 28 (changed act for ACIM = 1010).
- Added Figure 6 on page 14.
- Updated "5.25.Clock Generation" on page 36.
- Updated Table 23, “Register Summary,” on page 48.
- Updated Table 24, “Si3056 Pin Descriptions,” on page 84.
- Updated Figure 19 on page 26.
- Updated "5.6.Transmit/Receive Full Scale Level (Si3019 Line-Side Only)" on page 25 of Functional description to include new enhanced full scale mode.
- The following bits have been added, but will only be supported with Si3018/19/10 Revision E or later line-side devices.
  - Added FULL2 bit on p. 73.
  - Added RG1 and GCE bits on p. 89.
- Updated Table 24 on page 84.
- Updated "9.Ordering Guide[1,2]" on page 88.
- Update "12.Product Identification" on page 90.
- Updated "3.Bill of Materials" on page 19.
  - Changed recommended case size of FB1, FB2.

SILICON LABORATORIES Si3056 SUPPORT DOCUMENTATION

- Application Note 13: Silicon DAA Software Guidelines
- Application Note 16: Multiple Device Support
- Application Note 17: Designing for International Safety Compliance
- Application Note 67: Layout Guidelines
- Application Note 72: Ring Detection/Validation with the Si305x DAAs
- Application Note 84: Digital Hybrid with the Si305x DAAs
- Si30xxPPT-EVB Data Sheet
- Si30xxSSI-EVB Data Sheet

Note: Refer to www.silabs.com for a current list of support documents for this chipset.

NOTES:

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