PACKAGE/ORDERING INFORMATION

MODEL	ORDER NUMBER	PACKAGE DESCRIPTION	PACKAGE OPTION	MARKING INFORMATION
SGM8625	SGM8625XN5/TR	SOT-23-5	Tape and Reel, 3000	8625

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V-.. 7.5V
Package Thermal Resistance @ T_A = +25℃
SOT-23-5, θ_{JA}... 190℃/W
Common-Mode Input Voltage.......... ($-V_S$) - 0.5 V to ($+V_S$) +0.5V
Storage Temperature Range ....-65℃ to +150℃
Junction Temperature...160℃
Operating Temperature Range..........................-40℃ to +125℃
Lead Temperature Range (Soldering 10 sec)....................260℃
ESD Susceptibility
HBM...1500V
MM...400V

NOTE:
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.
SGMICRO reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SGMICRO sales office to get the last datasheet.

ELECTRICAL CHARACTERISTICS: V_S = +5V

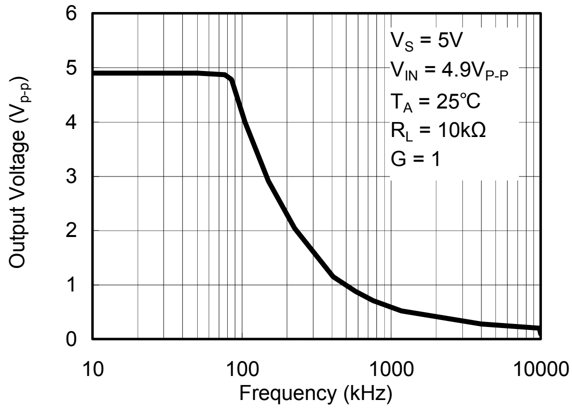
(At T_A = +25℃, V_{CM} = Vs/2, R_L = 600Ω, unless otherwise noted.)

PARAMETER	CONDITIONS	SGM8625 TYP +25℃	MIN/MAX OVER TEMPERATURE +25℃	-40℃ to 85℃	-40℃ to 125℃	UNITS	MIN/ MAX
INPUT CHARACTERISTICS							
Input Offset Voltage (V_{OS})		0.7	3	3.3	3.5	mV	MAX
Input Bias Current (I_B)		1				pA	TYP
Input Offset Current (I_{OS})		1				pA	TYP
Common-Mode Voltage Range (V_{CM})	V_S = 5.5V	-0.1 to +5.6				V	TYP
Common-Mode Rejection Ratio(CMRR)	V_S = 5.5V, V_{CM} = -0.1V to 4V	90	75	73	73	dB	MIN
	V_S = 5.5V, V_{CM} = -0.1V to 5.6V	92	66	65	64	dB	MIN
Open-Loop Voltage Gain (A_{OL})	R_L = 600Ω ,Vo = 0.15V to 4.85V	100	92	89	78	dB	MIN
	R_L = 10kΩ ,Vo = 0.05V to 4.95V	110	100	98	82	dB	MIN
Input Offset Voltage Drift ($\Delta V_{OS}/\Delta_T$)		2.7				μV/℃	TYP
OUTPUT CHARACTERISTICS							
Output Voltage Swing from Rail	R_L = 600Ω	0.1				V	TYP
	R_L = 10kΩ	0.015				V	TYP
Output Current (I_{OUT})		48	45	40	30	mA	MIN
Closed-Loop Output Impedance	F = 100kHz, G = +1	2.6				Ω	TYP
POWER-DOWN DISABLE							
Turn-On Time		6.2				ns	TYP
Turn-Off Time		1.4				ns	TYP
$\overline{\text{DISABLE}}$ Voltage-Off			0.8			V	MAX
$\overline{\text{DISABLE}}$ Voltage-On			2			V	MIN
POWER SUPPLY							
Operating Voltage Range			2.5	2.5	2.5	V	MIN
			5.5	5.5	5.5	V	MAX
Power Supply Rejection Ratio (PSRR)	V_S = +2.5V to +5.5V						
	V_{CM} = (-V_S) + 0.5V	94	79	77	76	dB	MIN
Quiescent Current (I_Q)	I_{OUT} = 0	250	300	350	380	μA	MAX
DYNAMIC PERFORMANCE							
Gain-Bandwidth Product (GBP)	R_L = 10kΩ	3				MHz	TYP
Phase Margin (φ_O)		67				degrees	TYP
Full Power Bandwidth (BW_P)	< 1% distortion, R_L = 600Ω	50				kHz	TYP
Slew Rate (SR)	G = +1, 2V Step, R_L = 10kΩ	1.7				V/μs	TYP
Settling Time to 0.1% (t_S)	G = +1, 2V Step, R_L = 600Ω	2.1				μs	TYP
Overload Recovery Time	V_{IN} ·Gain = V_S, R_L = 600Ω	1				μs	TYP
NOISE PERFORMANCE							
Voltage Noise Density (e_n)	f = 1kHz	12				nV/ $\sqrt{Hz}$	TYP
Current Noise Density (i_n)	f = 1kHz	3				fA/ $\sqrt{Hz}$	TYP

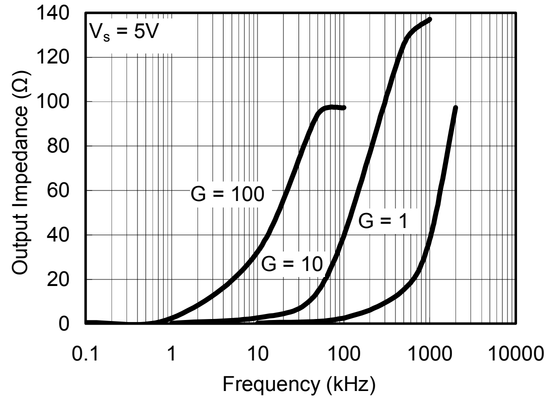
TYPICAL PERFORMANCE CHARACTERISTICS

(At T_A = +25℃, V_{CM} = V_S/2, R_L = 600Ω, unless otherwise noted.)

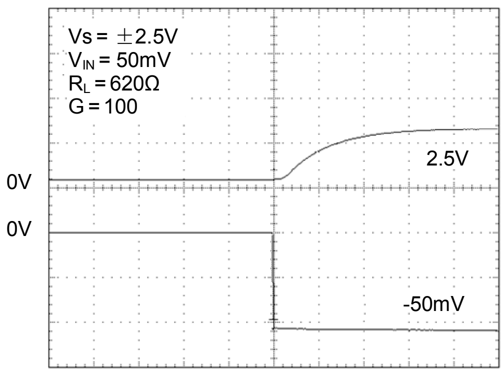
Closed-Loop Output Voltage Swing



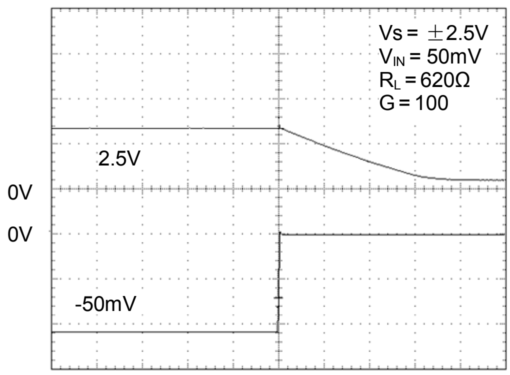
Output Impedance vs. Frequency



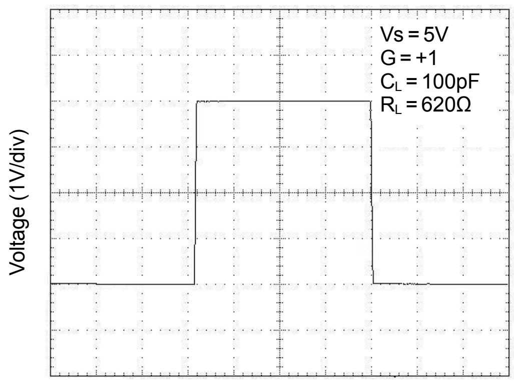
Positive Overload Recovery



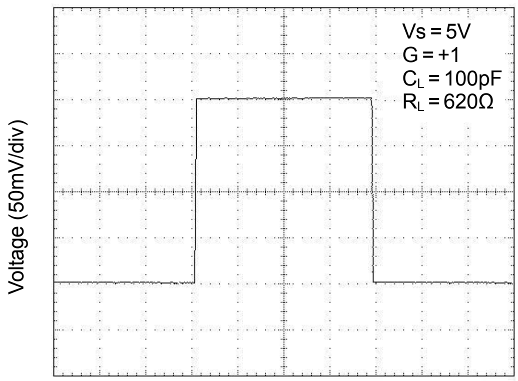
Negative Overload Recovery



Large-Signal Step Response

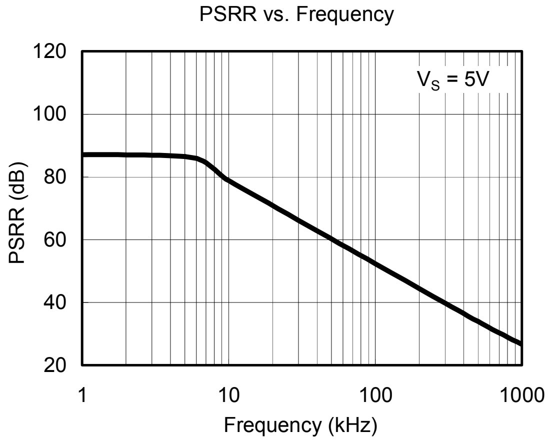


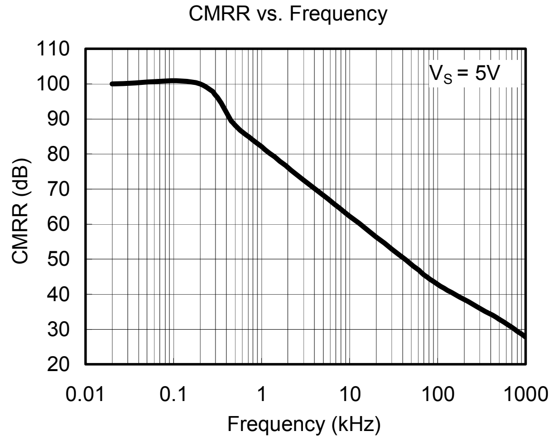
Small-Signal Step Response

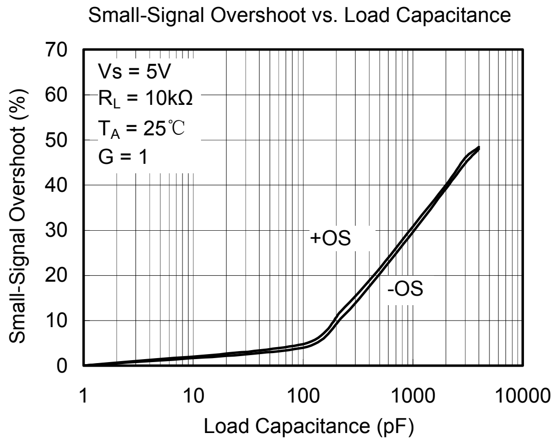


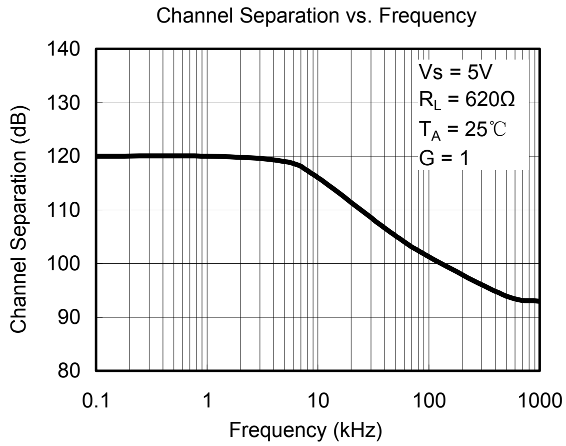
TYPICAL PERFORMANCE CHARACTERISTICS

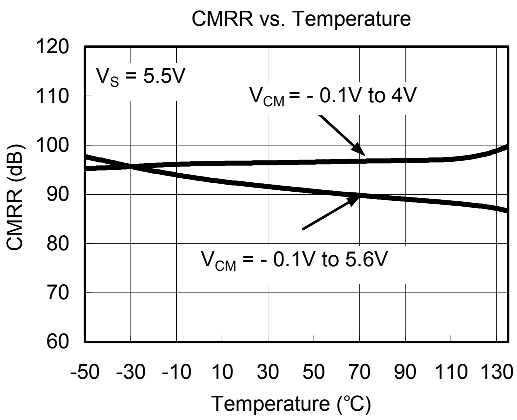
(At T_A = +25℃, V_{CM} = Vs/2, R_L = 600Ω, unless otherwise noted.)

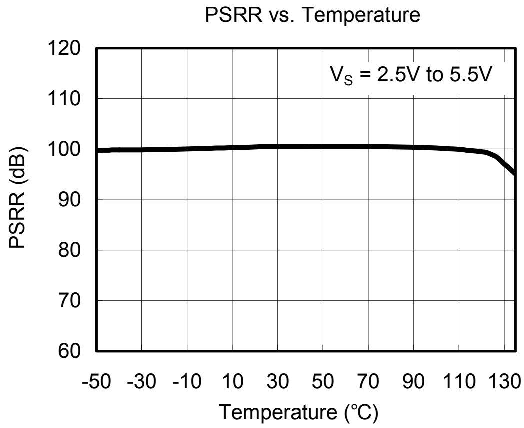






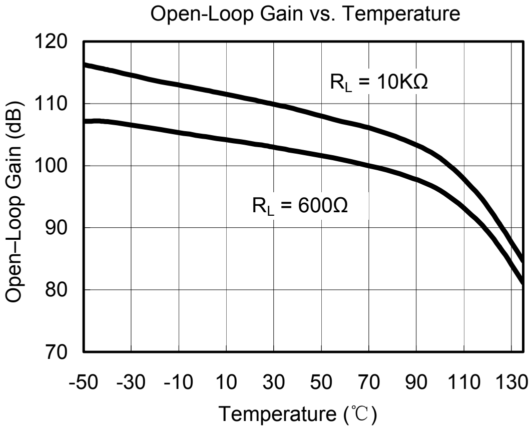


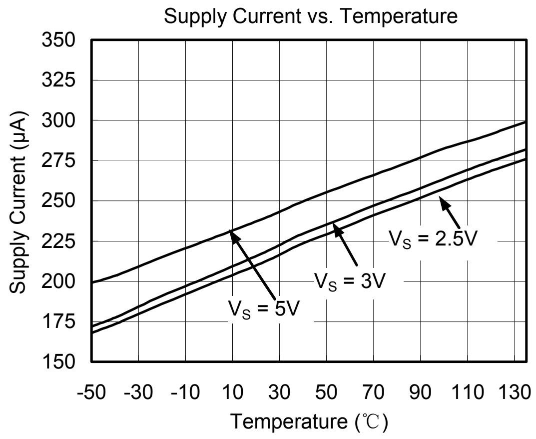


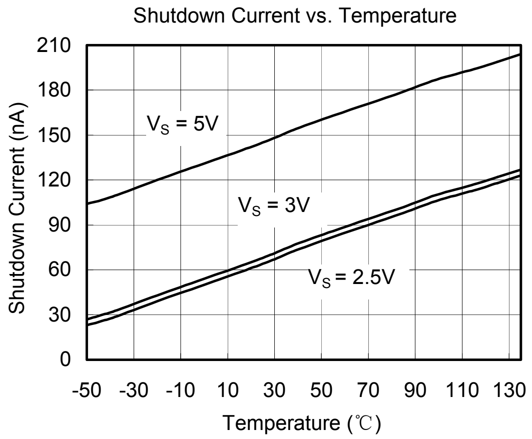


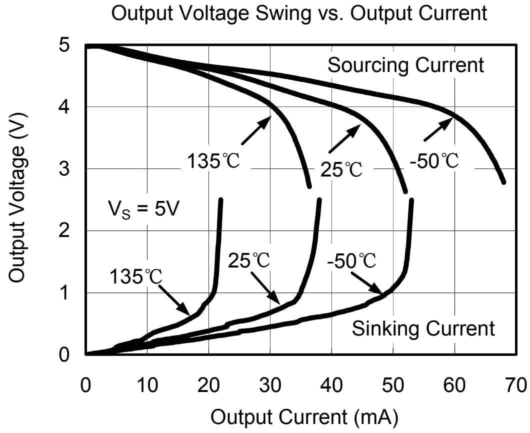
TYPICAL PERFORMANCE CHARACTERISTICS

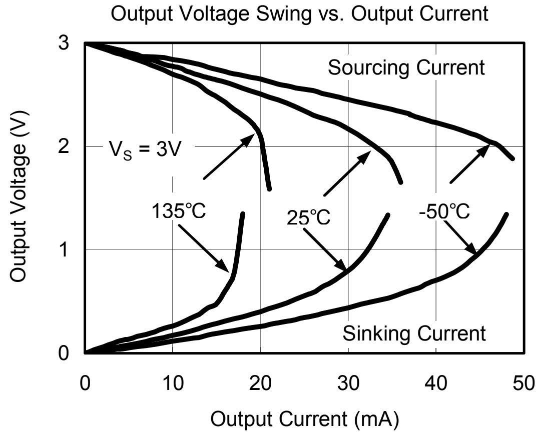
(At T_A = +25°C, V_{CM} = Vs/2, R_L = 600Ω, unless otherwise noted.)

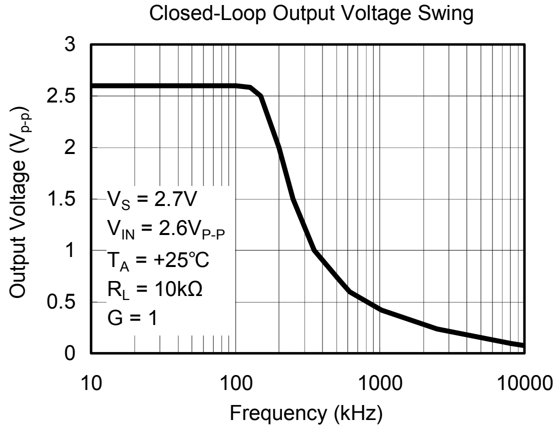






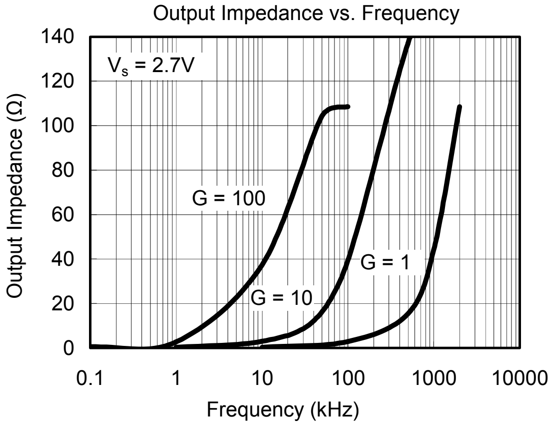


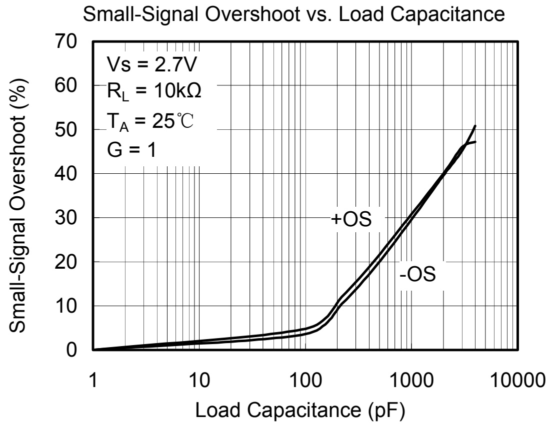


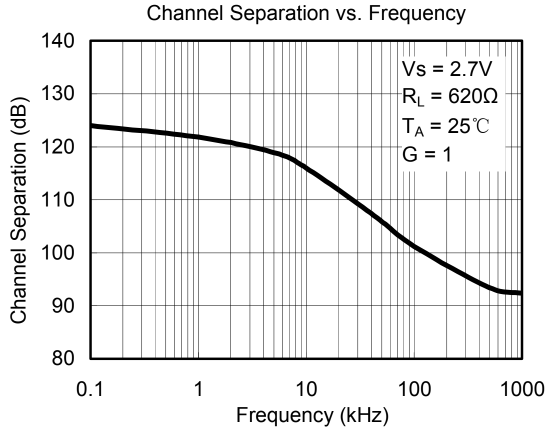


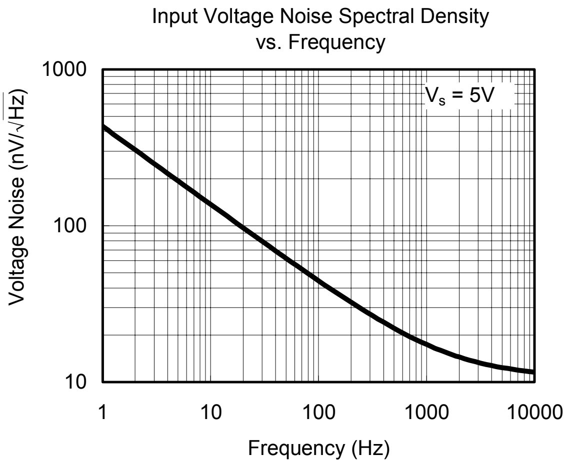
TYPICAL PERFORMANCE CHARACTERISTICS

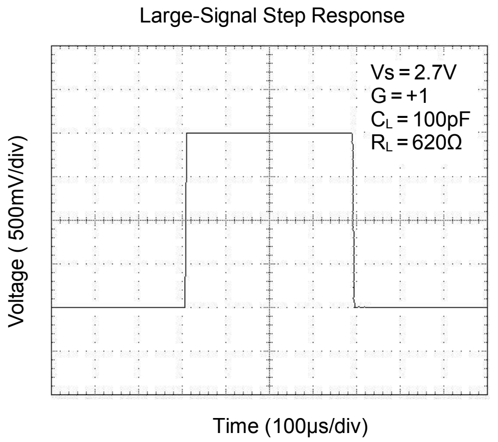
(At T_A = +25℃, V_{CM} = Vs/2, R_L = 600Ω, unless otherwise noted.)

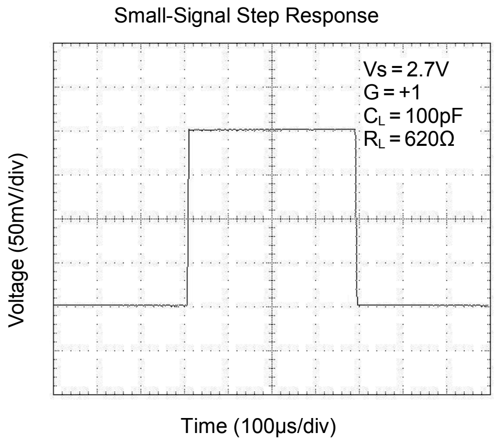












APPLICATION NOTES

Driving Capacitive Loads

The SGM8625 can directly drive 1000pF in unity-gain without oscillation. The unity-gain follower (buffer) is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers and this results in ringing or even oscillation. Applications that require greater capacitive drive capability should use an isolation resistor between the output and the capacitive load like the circuit in Figure 1. The isolation resistor R_{ISO} and the load capacitor C_L form a zero to increase stability. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_{LOAD}.

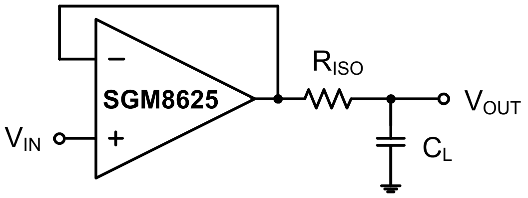


Figure 1. Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 2. It provides DC accuracy as well as AC stability. R_F provides the DC accuracy by connecting the inverting signal with the output. C_F and R_{Iso} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

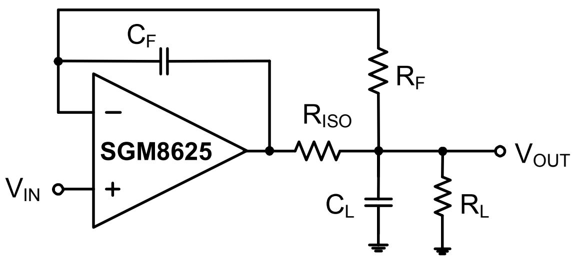


Figure 2. Indirectly Driving Heavy Capacitive Load with DC Accuracy

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

Power-Supply Bypassing and Layout

The SGM8625 operates from either a single +2.5V to +5.5V supply or dual ±1.25V to ±2.75V supplies. For single-supply operation, bypass the power supply V_{DD} with a 0.1μF ceramic capacitor which should be placed close to the V_{DD} pin. For dual-supply operation, both the V_{DD} and the V_{SS} supplies should be bypassed to ground with separate 0.1μF ceramic capacitors. 2.2μF tantalum capacitor can be added for better performance.

Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close to the device as possible. Use surface-mount components whenever possible.

For the operational amplifier, soldering the part to the board directly is strongly recommended. Try to keep the high frequency big current loop area small to minimize the EMI (electromagnetic interfacing).

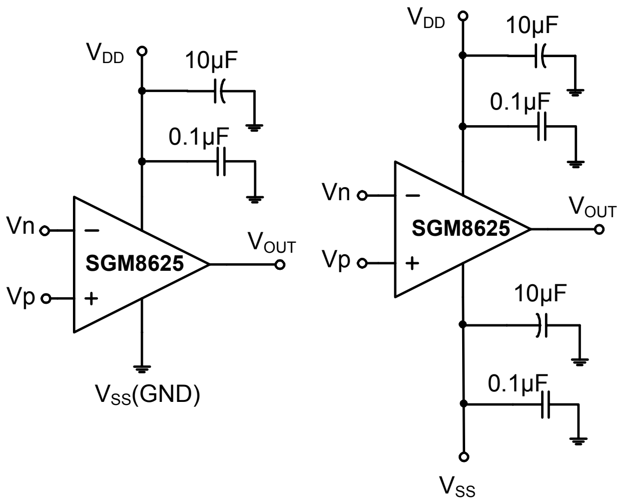


Figure 3. Amplifier with Bypass Capacitors

Grounding

A ground plane layer is important for SGM8625 circuit design. The length of the current path speed currents in an inductive ground return will create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance.

Input-to-Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

TYPICAL APPLICATION CIRCUITS

Differential Amplifier

The circuit shown in Figure 4 performs the difference function. If the resistors ratios are equal (R_4 / R_3 = R_2 / R_1), then V_{OUT} = (Vp – Vn) × R_2 / R_1 + V_{REF}.

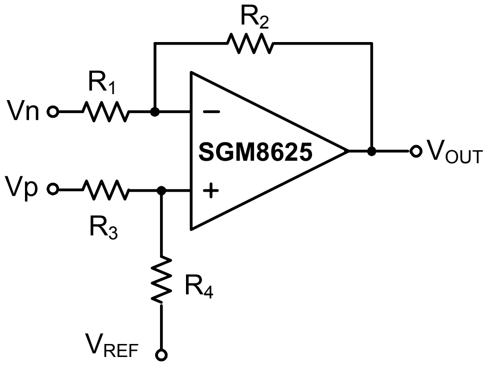


Figure 4. Differential Amplifier

Instrumentation Amplifier

The circuit in Figure 5 performs the same function as that in Figure 4 but with the high input impedance.

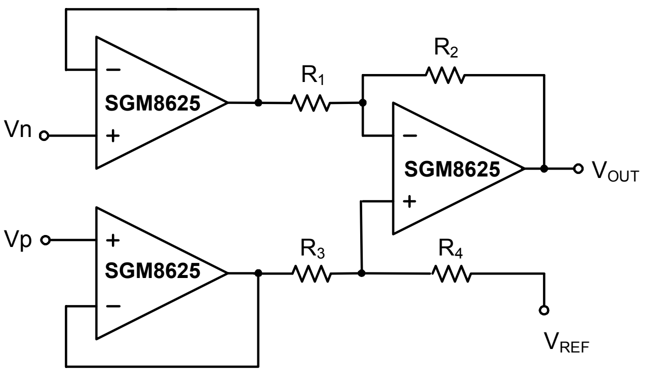


Figure 5. Instrumentation Amplifier

Low Pass Active Filter

The low pass filter shown in Figure 6 has a DC gain of ($-R_2/R_1$) and the –3dB corner frequency is $1/2\pi R_2C$. Make sure the filter is within the bandwidth of the amplifier. The Large values of feedback resistors can couple with parasitic capacitance and cause undesired effects such as ringing or oscillation in high-speed amplifiers. Keep resistors value as low as possible and consistent with output loading consideration.

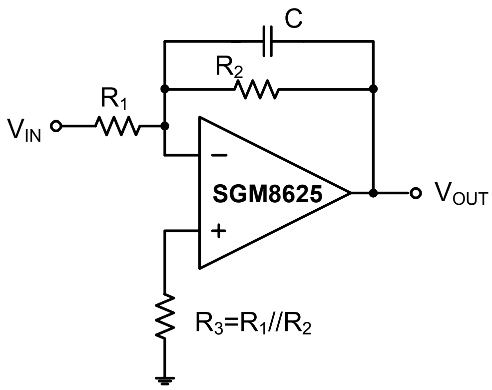
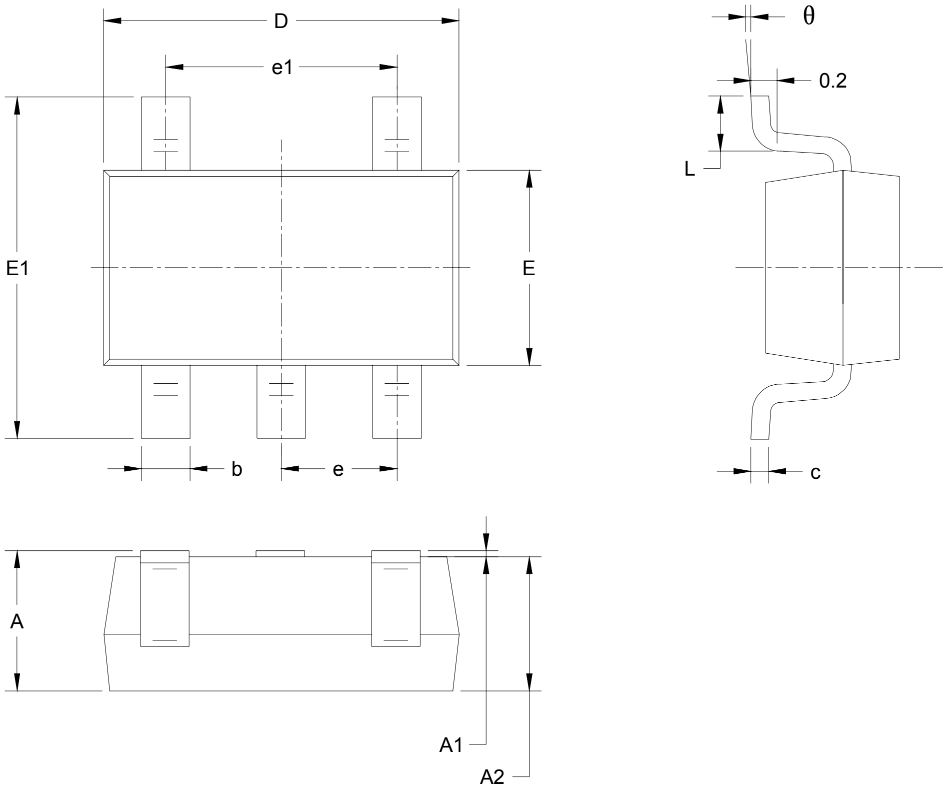


Figure 6. Low Pass Active Filter

PACKAGE OUTLINE DIMENSIONS

SOT-23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°