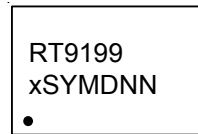


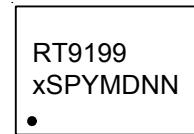
Marking Information

RT9199xS



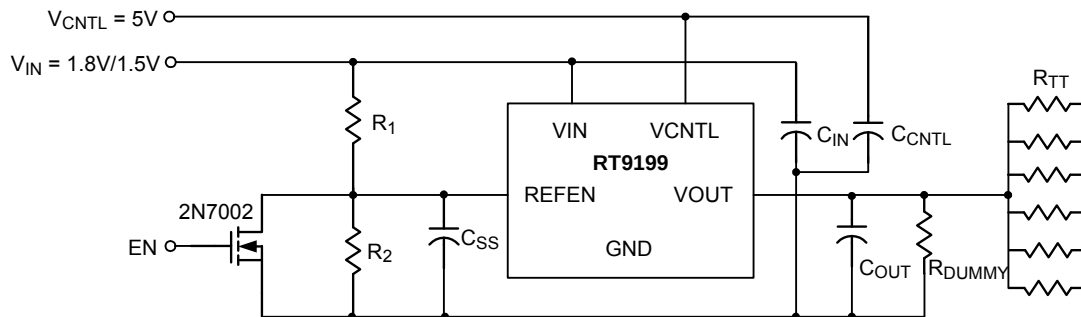
RT9199xS : Product Number
x : P or G or Z
YMDNN : Date Code

RT9199xSP



RT9199xSP : Product Number
x : P or G or Z
YMDNN : Date Code

Typical Application Circuit



$R_1 = R_2 = 100\text{k}\Omega$, $R_{TT} = 50\Omega / 33\Omega / 25\Omega$

$C_{OUT(MIN)} = 10\mu\text{F}$ (Ceramic) + $1000\mu\text{F}$ under the worst case testing condition

$R_{DUMMY} = 1\text{k}\Omega$ as for V_{OUT} discharge when V_{IN} is not presented but V_{CNTL} is presented

$C_{SS} = 1\mu\text{F}$, $C_{IN} = 470\mu\text{F}$ (Low ESR), $C_{CNTL} = 47\mu\text{F}$

Test Circuit

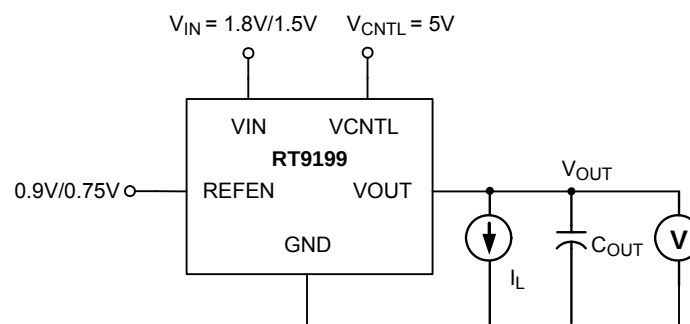


Figure 1. Output Voltage Tolerance, ΔV_{LOAD}

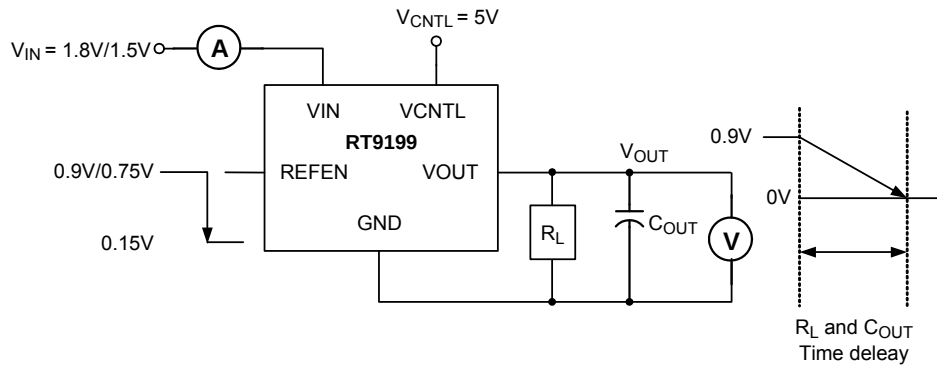


Figure 2. Current in Shutdown Mode, I_{STBY}

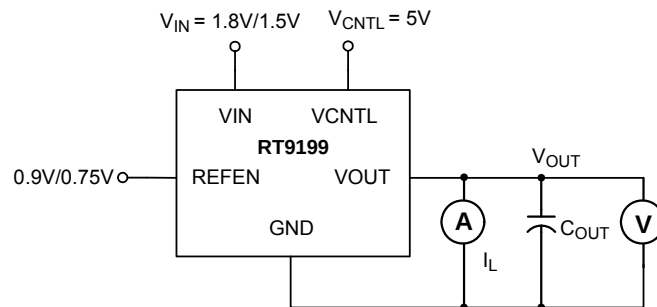


Figure 3. Current Limit for High Side, I_{LIM}

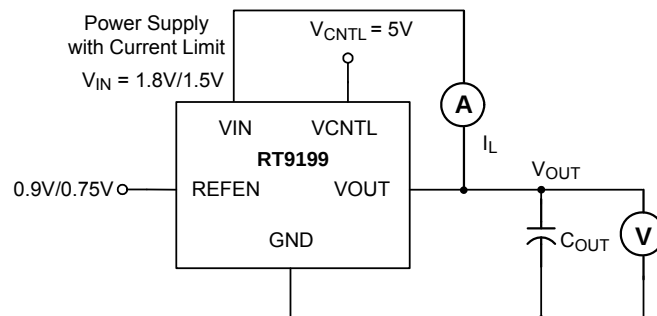


Figure 4. Current Limit for Low Side, I_{LIM}

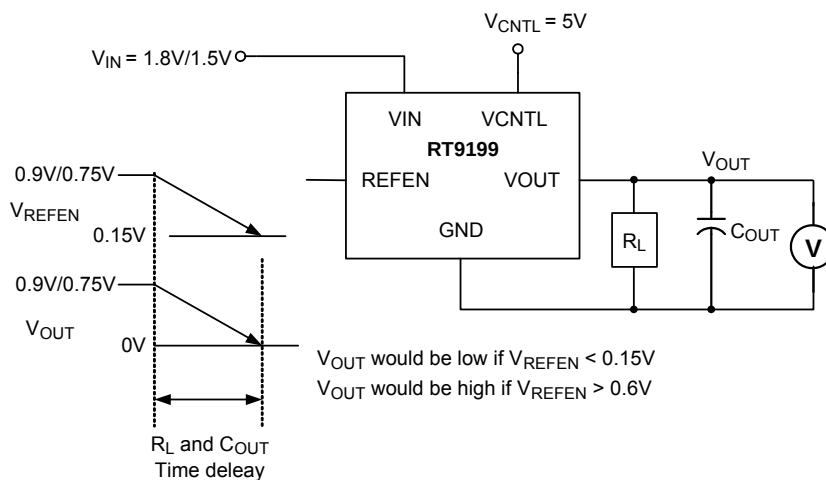


Figure 5. $REFEN$ Pin Shutdown Threshold, V_{IH} & V_{IL}

Functional Pin Description

VIN

Input voltage which supplies current to the output pin. Connect this pin to a well-decoupled supply voltage. To prevent the input rail from dropping during large load transient, a large, low ESR capacitor is recommended to use. The capacitor should be placed as close as possible to the VIN pin.

GND (Exposed Pad)

Common Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

VCNTL

VCNTL supplies the internal control circuitry and provides the drive voltage. The driving capability of output current is proportioned to the VCNTL. Connect this pin to 5V bias supply to handle large output current with at least 1 μ F capacitor from this pin to GND. An important note is that VIN should be kept lower or equal to VCNTL.

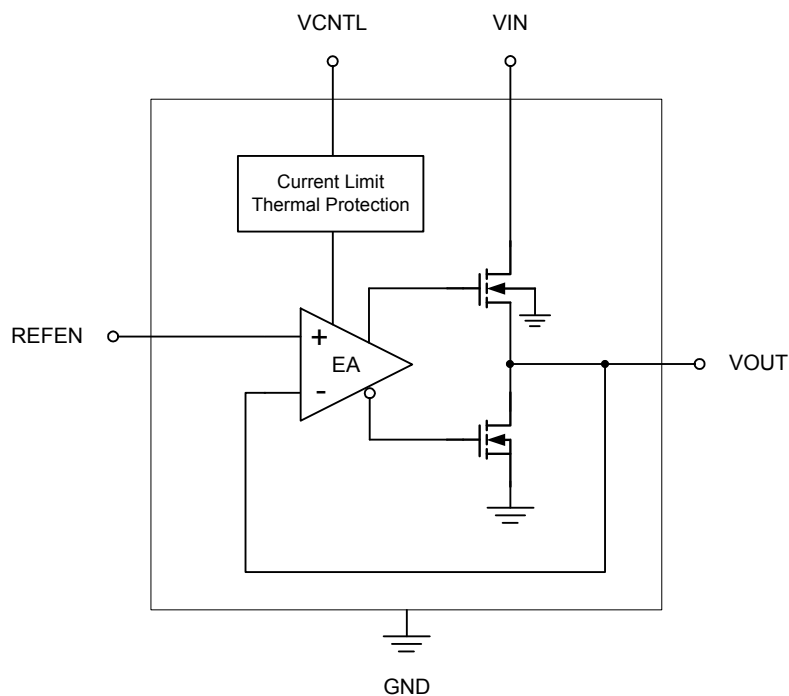
REFEN

Reference voltage input and active low shutdown control pin. Two resistors dividing down the VIN voltage on the pin to create the regulated output voltage. Pulling the pin to ground turns off the device by an open-drain, such as 2N7002, signal N-MOSFET.

VOUT

Regulator output. VOUT is regulated to REFEN voltage that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output rail. To maintain adequate large signal transient response, typical value of 1000 μ F Al electrolytic capacitor with 10 μ F ceramic capacitors are recommended to reduce the effects of current transients on VOUT.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

• Input Voltage, V_{IN}	6V
• Control Voltage, V_{CNTL}	6V
• Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$	
SOP-8	0.909W
SOP-8 (Exposed Pad)	2.33W
• Package Thermal Resistance (Note 2)	
SOP-8, θ_{JA}	110°C/W
SOP-8, θ_{JC}	60°C/W
SOP-8 (Exposed Pad), θ_{JA}	42.9°C/W
SOP-8 (Exposed Pad), θ_{JC}	12.6°C/W
• Junction Temperature	125°C
• Lead Temperature (Soldering, 10 sec.)	260°C
• Storage Temperature Range	-65°C to 150°C
• ESD Susceptibility (Note 3)	
HBM (Human Body Model)	2kV
MM (Machine Model)	200V

Recommended Operating Conditions (Note 4)

• Input Voltage, V_{IN}	1.4V to 5.5V
• Control Voltage, V_{CNTL}	5V $\pm$ 5%
• Junction Temperature Range	-40°C to 125°C

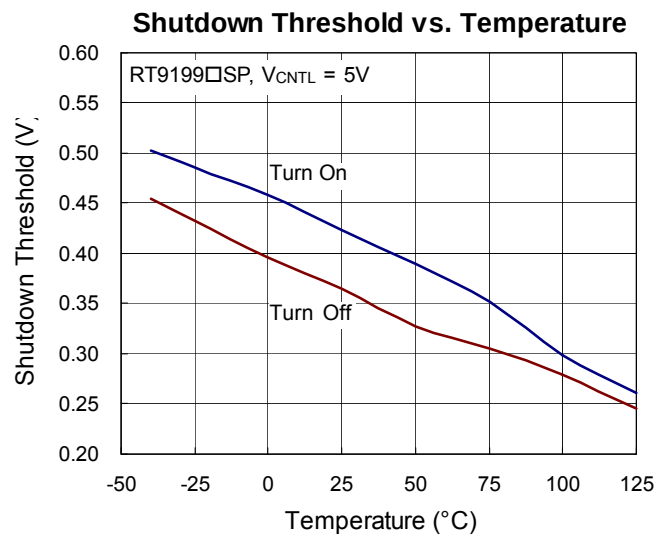
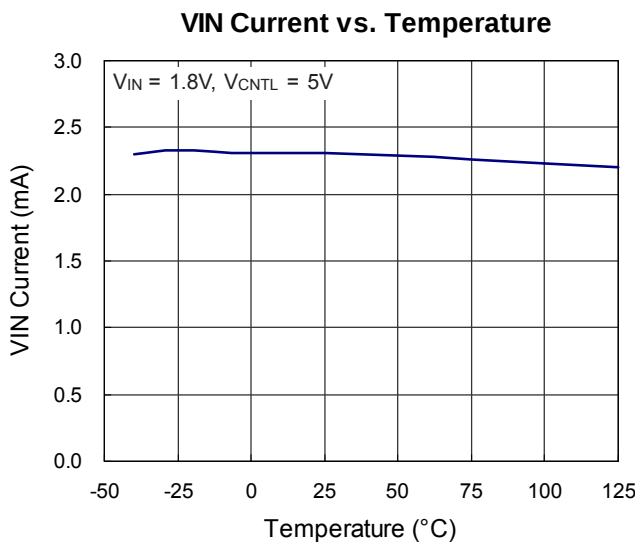
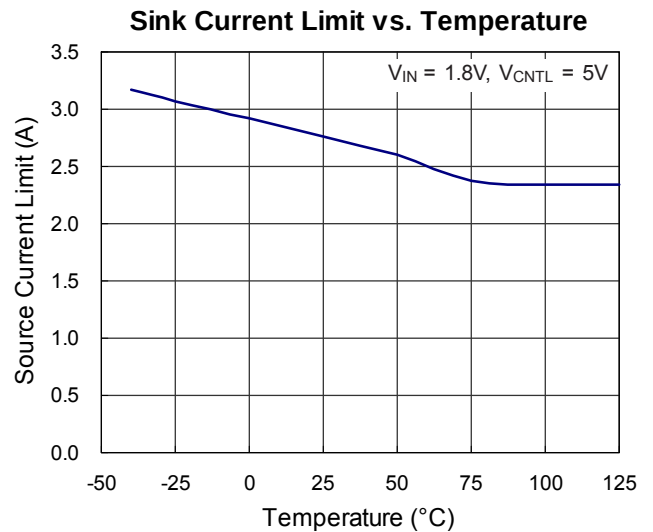
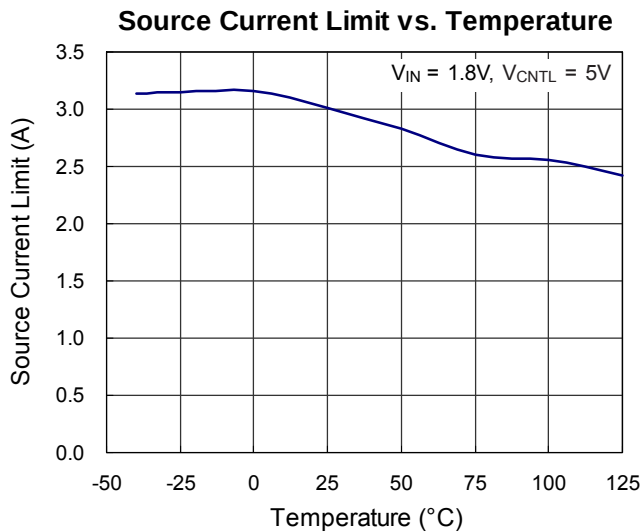
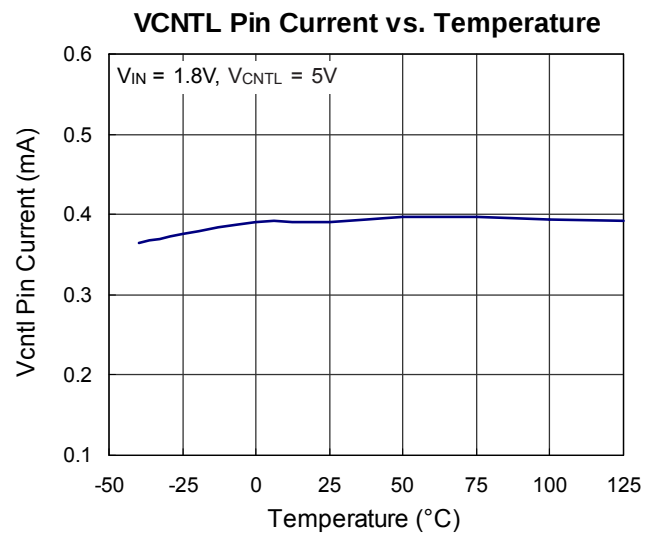
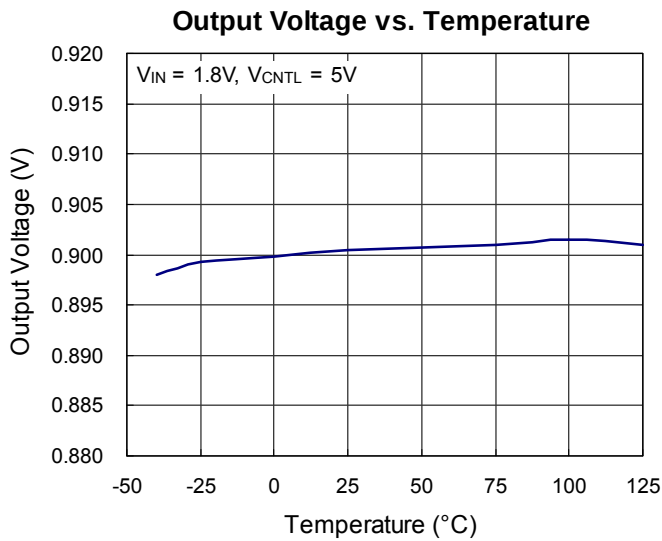
Electrical Characteristics

($V_{IN} = 1.8\text{V}/1.5\text{V}$, $V_{CNTL} = 5\text{V}$, $V_{REFEN} = 0.9\text{V}/0.75\text{V}$, $C_{OUT} = 10\mu\text{F}$ (Ceramic), $T_A = 25^\circ\text{C}$, unless otherwise specified)

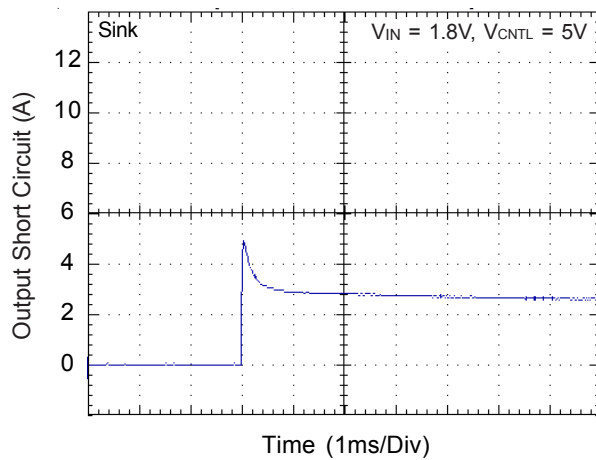
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input						
VCNTL Operation Current	I _{CNTL}	I _{OUT} = 0A	--	1	2.5	mA
Standby Current (Note 5)	I _{STBY}	V _{REFEN} < 0.2V (Shutdown), R _{LOAD} = 180Ω	--	2	90	μA
Output (DDR II)						
Output Offset Voltage (Note 6)	V _{OS}	I _{OUT} = 0A	−10	--	10	mV
Load Regulation (Note 7)	ΔV _{LOAD}	V _{IN} = 1.8V, V _{REFIN} = 0.9V, I _{OUT} = ±1.8A	−20	--	20	mV
		V _{IN} = 1.5V, V _{REFIN} = 0.75V, I _{OUT} = ±1.4A	−10	--	10	
Protection						
Current limit	I _{LIMIT}	V _{IN} = 1.8V, V _{REFIN} = 0.9V	2	--	3.5	A
		V _{IN} = 1.5V, V _{REFIN} = 0.75V	1.5	--	3.5	
Thermal Shutdown Temperature	T _{SD}	V _{CNTL} = 5V	125	170	--	°C
Thermal Shutdown Hysteresis	ΔT _{SD}	V _{CNTL} = 5V	--	35	--	°C
REFEN Shutdown						
Shutdown Threshold	V _{IH}	Enable	0.6	--	--	V
	V _{IL}	Shutdown	--	--	0.15	

- Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
- Note 2.** θ_{JA} is measured in the natural convection at $T_A = 25^{\circ}\text{C}$ on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the exposed pad for package.
- Note 3.** Devices are ESD sensitive. Handling precaution recommended.
- Note 4.** The device is not guaranteed to function outside its operating conditions.
- Note 5.** Standby current is the input current drawn by a regulator when the output voltage is disabled by a shutdown signal on REFEN pin ($V_{IL} < 0.15\text{V}$). It is measured with $V_{IN} = V_{CNTL} = 5\text{V}$.
- Note 6.** V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN} .
- Note 7.** Regulation is measured at constant junction temperature by using a 5ms current pulse. Devices are tested for load regulation in the load range from 0A to 2A peak.

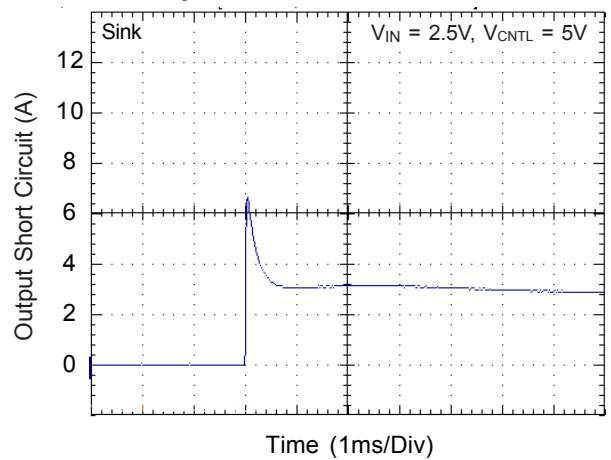
Typical Operating Characteristics



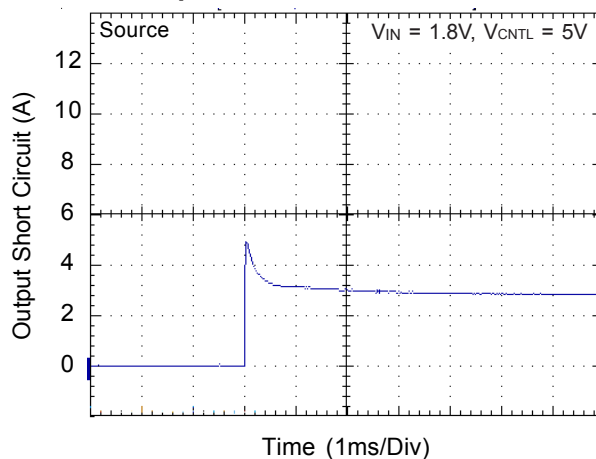
Output Short-Circuit Protection



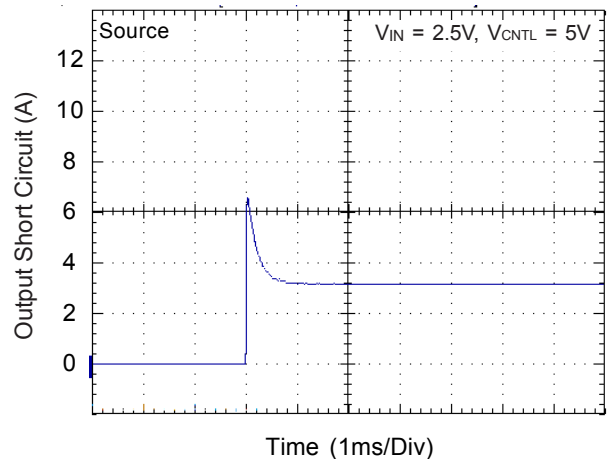
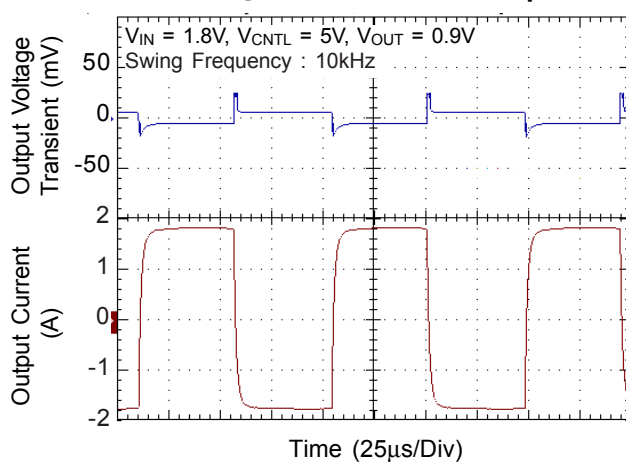
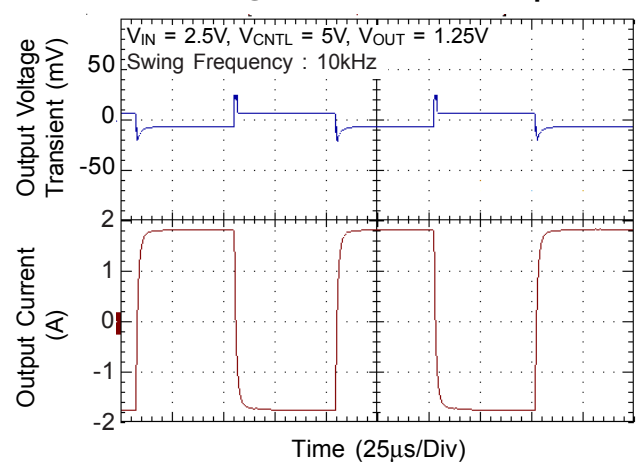
Output Short-Circuit Protection



Output Short-Circuit Protection



Output Short-Circuit Protection

0.9V_{TT} @ 1.8A Transient Response1.25V_{TT} @ 1.8A Transient Response

Application Information

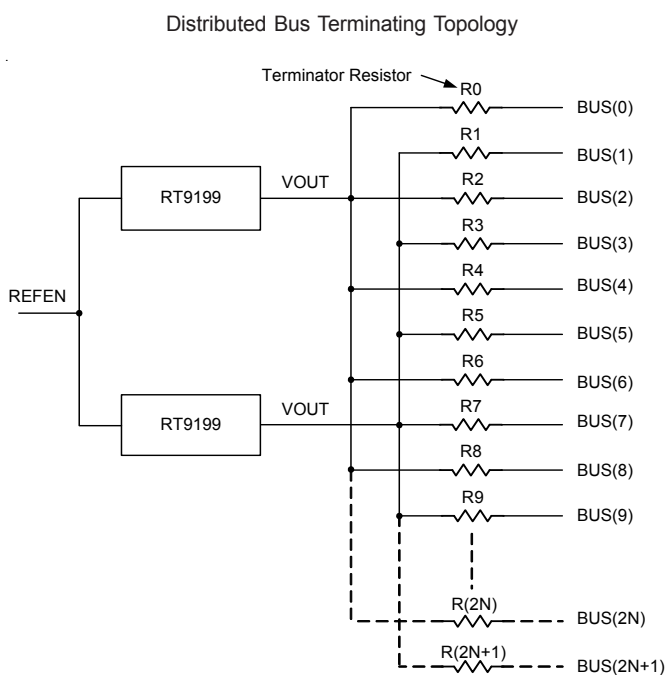
Consideration while designing the resistance of voltage divider

Refer to the “Typical Application Circuit”. Make sure the current sinking capability of pull-down NMOS is enough for the chosen voltage divider to pull-down the voltage at REFEN pin below 0.15V to shutdown the device.

In addition, the capacitor C_{SS} and voltage divider form the low-pass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.

How to reduce power dissipation on Notebook PC or the dual channel DDR SDRAM application?

In notebook application, using RichTek's Patent “Distributed Bus Terminator Topology” with choosing RichTek's product is encouraged.



General Regulator

The RT9199 could also serve as a general linear regulator. The RT9199 accepts an external reference voltage at REFEN pin and provides output voltage regulated to this reference voltage as shown in Figure 6, where

$$V_{OUT} = V_{REFEN} \times R2 / (R1 + R2)$$

As other linear regulator, dropout voltage and thermal issue should be specially considered. Figure 7 shows the $R_{DS(ON)}$ over temperature of RT9199. The minimum dropout voltage could be obtained by the product of $R_{DS(ON)}$ and output current. For thermal consideration, please refer to the relative sections.

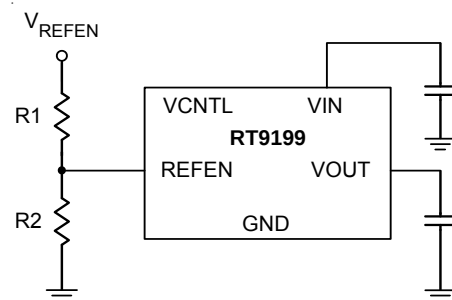


Figure 6

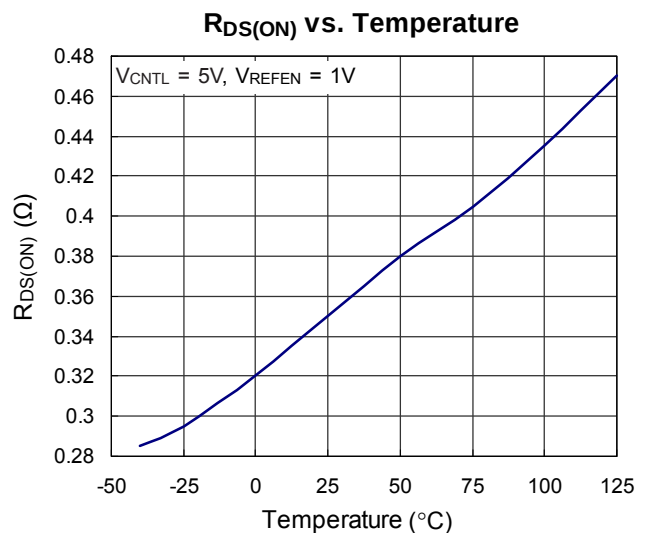


Figure 7

Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the RT9199. A low ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance. Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between RT9199 and the preceding power converter.

Thermal Consideration

RT9199 regulators have internal thermal limiting circuitry designed to protect the device during overload conditions. For continued operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. The junction to ambient thermal resistance for SOP-8 package (Exposed Pad) is 42.9°C/W, on standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / 42.9^\circ\text{C/W} = 2.33\text{W}$$

Figure 8 shows the package sectional drawing of SOP-8 (Exposed Pad). Every package has several thermal dissipation paths. As show in Figure 9, the thermal resistance equivalent circuit of SOP-8 (Exposed Pad). The path 2 is the main path due to these materials thermal conductivity. We define the exposed pad is the case point of the path 2.

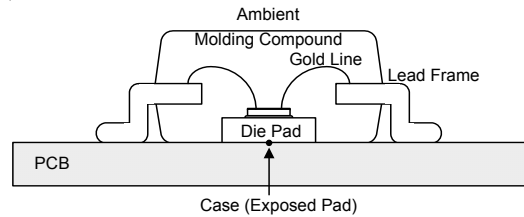


Figure 8. SOP-8 (Exposed Pad) Package Sectional Drawing

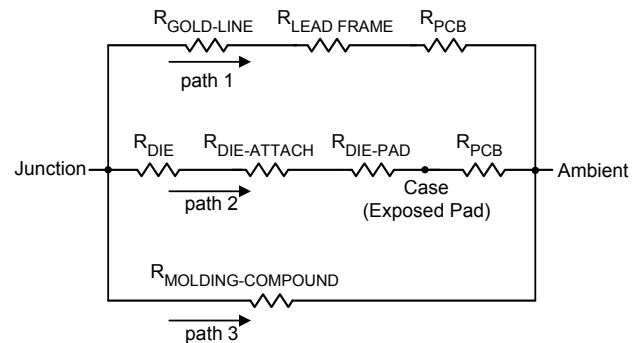
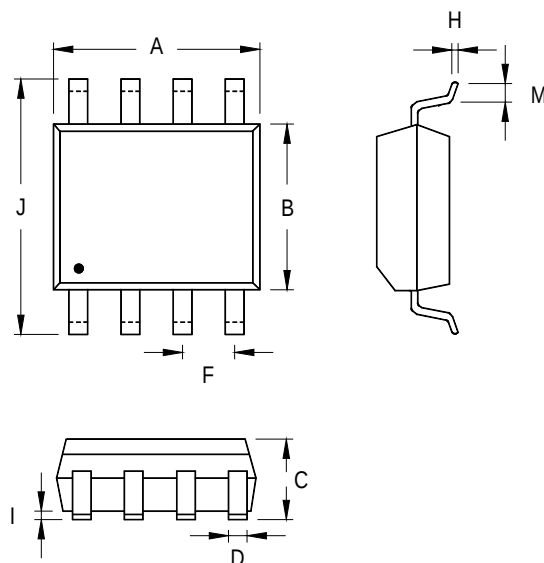


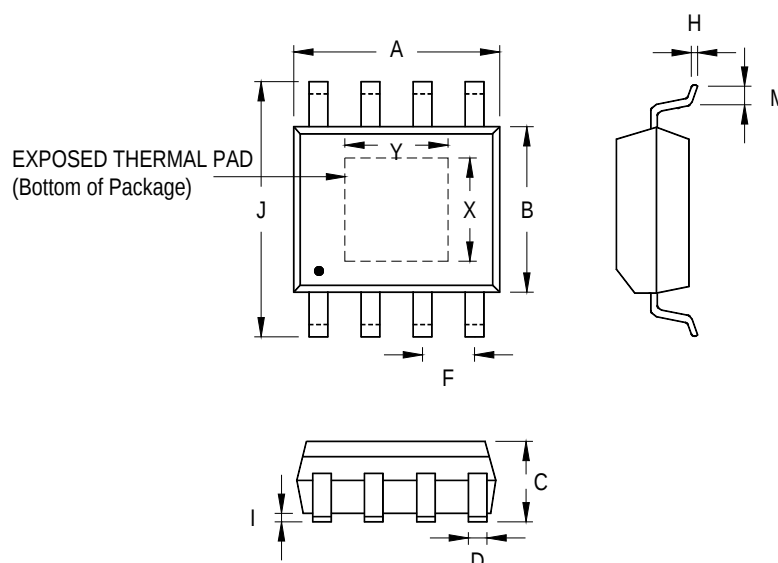
Figure 9. Thermal Resistance Equivalent Circuit

Outline Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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