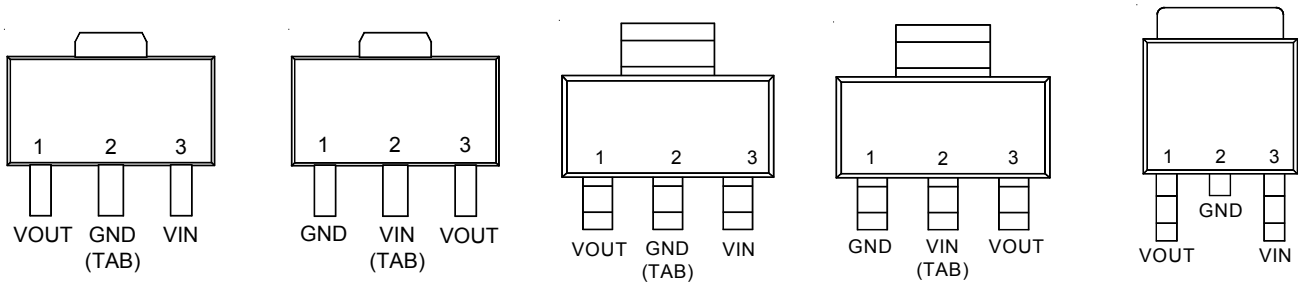
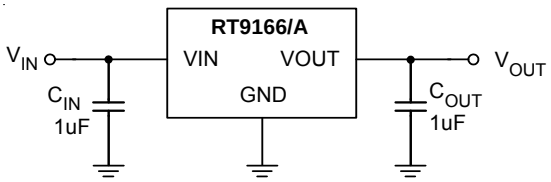


Typical Application Circuit

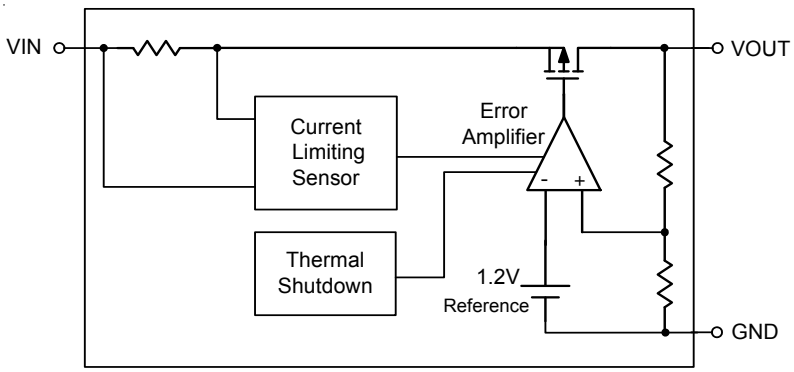


Note: To prevent oscillation, a 1μF minimum X7R or X5R dielectric is strongly recommended if ceramics are used as input/output capacitors. When using the Y5V dielectric, the minimum value of the input/output capacitance that can be used for stable over full operating temperature range is 3.3μF. (see Application Information Section for further details)

Functional Pin Description

Pin Name	Pin Function
VIN	Supply Input.
VOUT	Regulator Output.
GND	Common Ground.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  - SOT-23-3 ---------- 0.4W
  - SOT-89 ---------- 0.571W
  - SOT-223 ---------- 0.740W
  - TO-92 ---------- 0.625W
  - TO-252 ---------- 1.470W
- Package Thermal Resistance (Note 2)
  - SOT-23-3, θ_{JA} ---------- 250°C/W
  - SOT-89, θ_{JA} ---------- 175°C/W
  - SOT-89, θ_{JC} ---------- 58°C/W
  - SOT-223, θ_{JA} ---------- 135°C/W
  - SOT-223, θ_{JC} ---------- 15°C/W
  - TO-92, θ_{JA} ---------- 160°C/W
  - TO-92, θ_{JC} ---------- 40°C/W
  - TO-252, θ_{JA} ---------- 68°C/W
  - TO-252, θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.8V to 5.5V
- Junction Temperature Range ---------- – 40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = V_{OUT} + 1V or V_{IN} = 2.8V whichever is greater, C_{IN} = 1μF, C_{OUT} = 1μF, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Accuracy		ΔV_{OUT}	I_{OUT} = 1mA	–1	--	3	%
Current Limit	RT9166	I_{LIM}	R_{LOAD} = 1Ω	300	--	--	mA
	RT9166A			600	--	--	
Quiescent Current (Note 5)		I_Q	I_{OUT} = 0mA	--	220	300	μA
Dropout Voltage (Note 6)	RT9166	V_{DROP}	I_{OUT} = 300mA	--	230	--	mV
	RT9166A		I_{OUT} = 600mA	--	580	--	
Line Regulation		ΔV_{LINE}	V_{IN} = (V_{OUT} + 0.3V) to 5.5V, I_{OUT} = 1mA	--	0.2	--	%/V
Load Regulation (Note 7)	RT9166	ΔV_{LOAD}	1mA < I_{OUT} < 300mA	--	15	35	mV
	RT9166A		1mA < I_{OUT} < 600mA	--	30	55	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Rejection Rate	PSRR	f = 1kHz, C_{OUT} = 1μF	--	–55	--	dB
Thermal Shutdown Temperature	T_{SD}		--	170	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	40	--	°C

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a low effective thermal conductivity single-layer test board per JEDEC 51-3.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

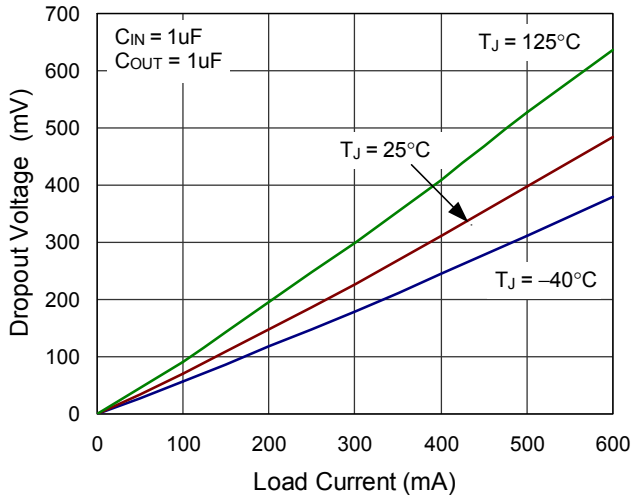
Note 5. Quiescent, or ground current, is the difference between input and output currents. It is defined by $I_Q = I_{IN} - I_{OUT}$ under no load condition (I_{OUT} = 0mA). The total current drawn from the supply is the sum of the load current plus the ground pin current.

Note 6. The dropout voltage is defined as $V_{IN} - V_{OUT}$, which is measured when V_{OUT} is $V_{OUT(NORMAL)}$ – 100mV.

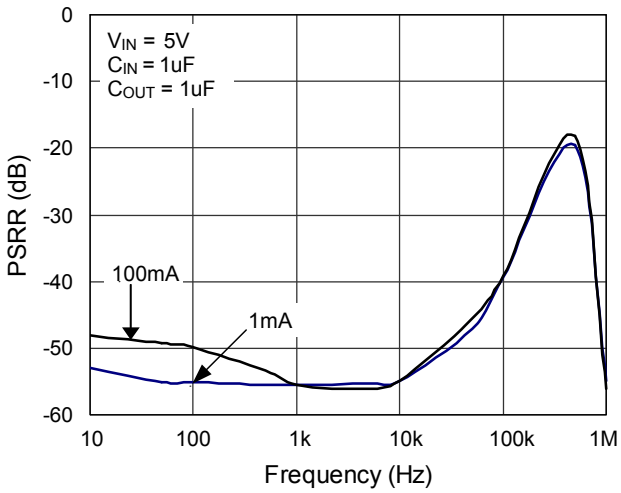
Note 7. Regulation is measured at constant junction temperature by using a 20ms current pulse. Devices are tested for load regulation in the load range from 1mA to 300mA and 600mA respectively.

Typical Operating Characteristics

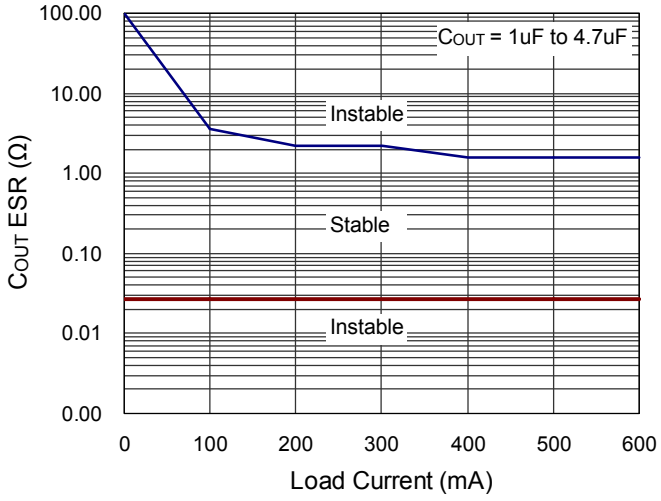
Dropout Voltage vs. Load Current



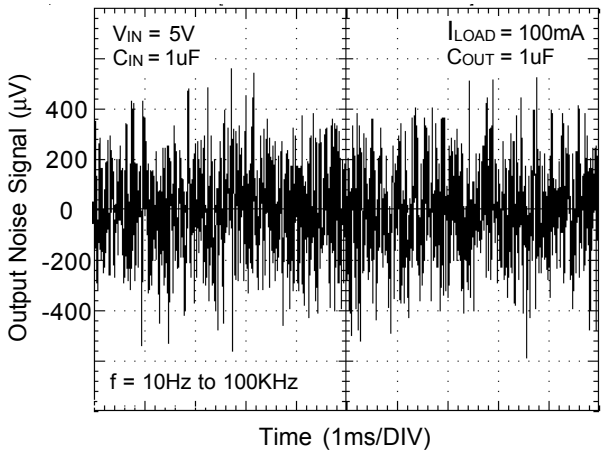
Power Supply Rejection Ratio



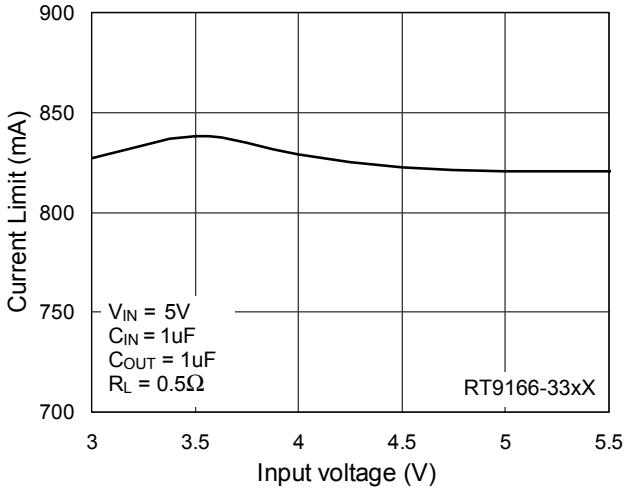
Region of Stable C_{OUT} ESR vs. Load Current



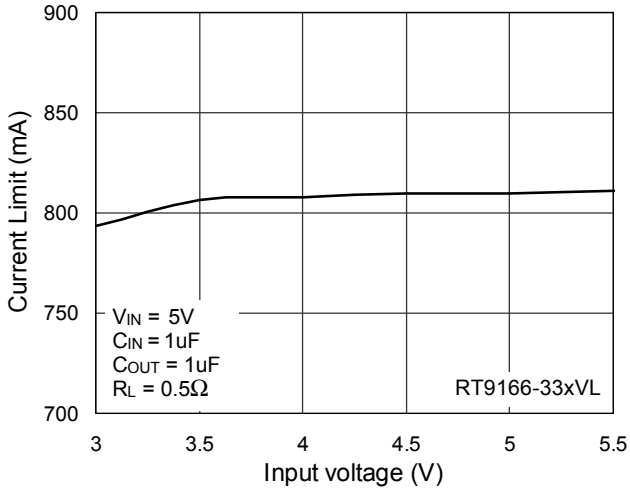
Output Noise



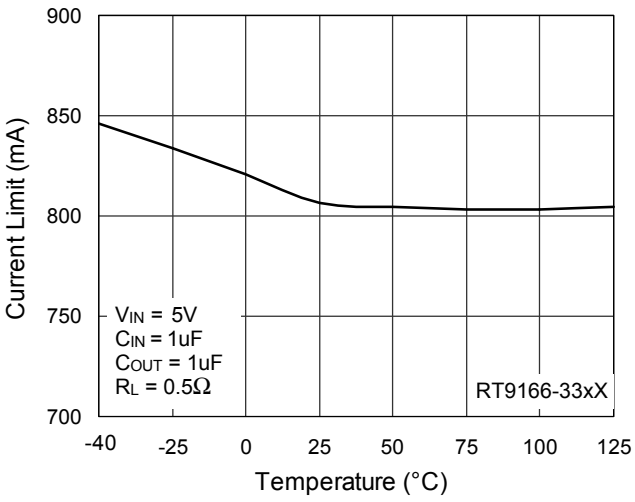
Current Limit vs. Input voltage



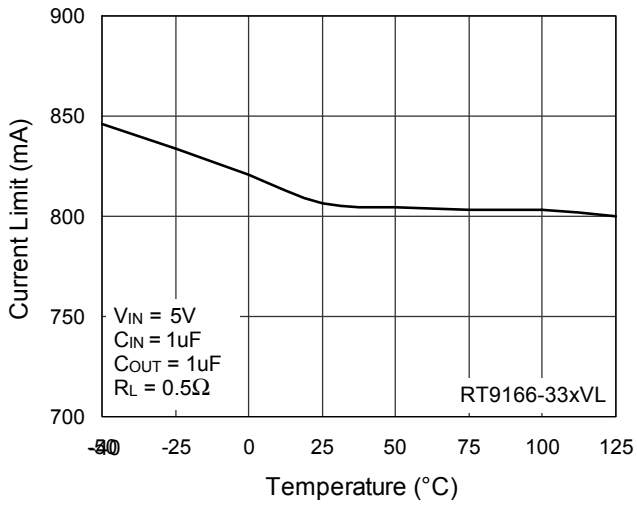
Current Limit vs. Input voltage



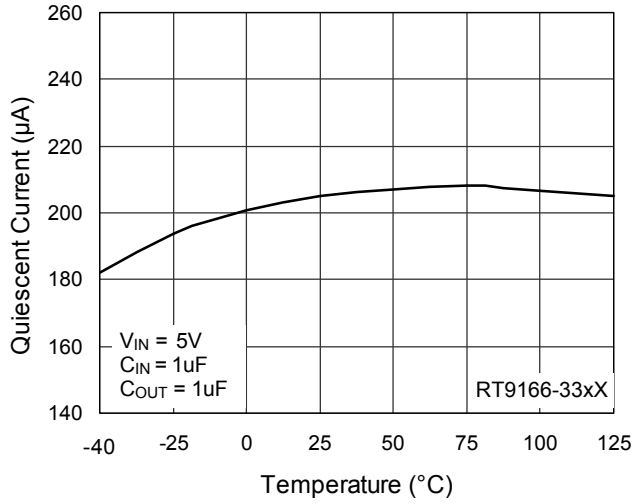
Current Limit vs. Temperature



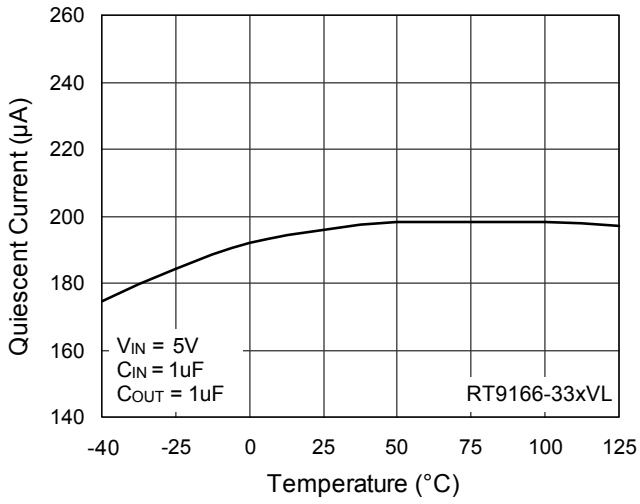
Current Limit vs. Temperature



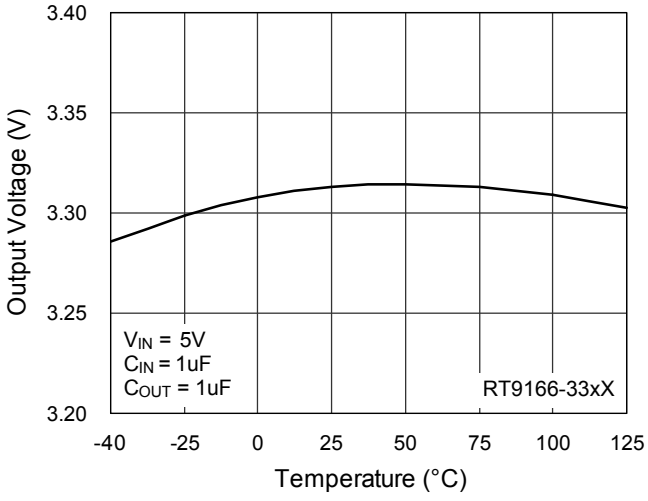
Quiescent Current vs. Temperature



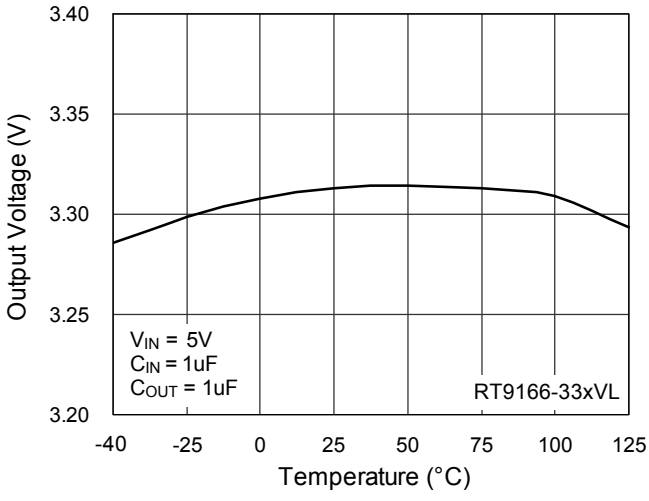
Quiescent Current vs. Temperature



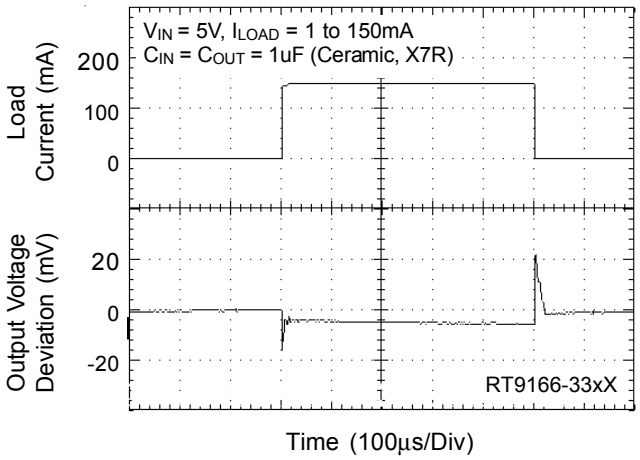
Temperature Stability



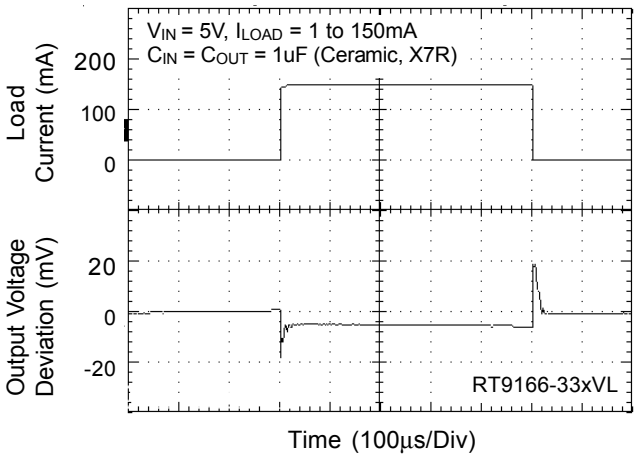
Temperature Stability



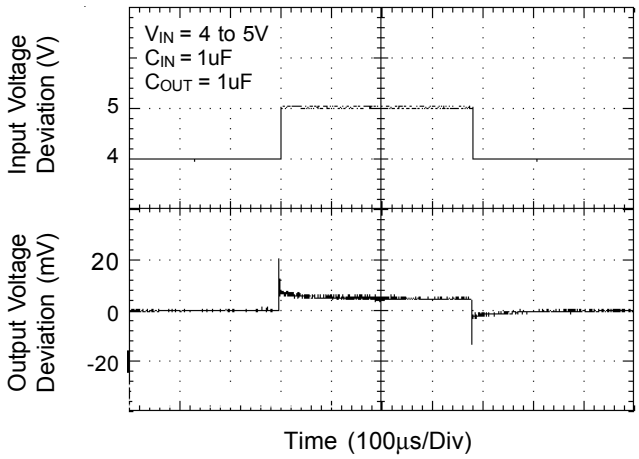
Load Transient Response



Load Transient Response



Line Transient Response



Application Information

Like any low-dropout regulator, the RT9166/A series requires input and output decoupling capacitors. These capacitors must be correctly selected for good performance (see Capacitor Characteristics Section). Please note that linear regulators with a low dropout voltage have high internal loop gains which require care in guarding against oscillation caused by insufficient decoupling capacitance.

Input Capacitor

An input capacitance of ≅ 1μF is required between the device input pin and ground directly (the amount of the capacitance may be increased without limit). The input capacitor ***MUST*** be located less than 1 cm from the device to assure input stability (see PCB Layout Section). A lower ESR capacitor allows the use of less capacitance, while higher ESR type (like aluminum electrolytic) require more capacitance.

Capacitor types (aluminum, ceramic and tantalum) can be mixed in parallel, but the total equivalent input capacitance/ESR must be defined as above to stable operation.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be ≅ 1μF over the entire operating temperature range.

Output Capacitor

The RT9166/A is designed specifically to work with very small ceramic output capacitors. The recommended minimum capacitance (temperature characteristics X7R or X5R) is 1μF to 4.7μF range with 10mΩ to 50mΩ range ceramic capacitor between LDO output and GND for transient stability, but it may be increased without limit. Higher capacitance values help to improve transient. The output capacitor's ESR is critical because it forms a zero to provide phase lead which is required for loop stability. (When using the Y5V dielectric, the minimum value of the input/output capacitance that can be used for stable over full operating temperature range is 3.3μF.)

No Load Stability

The device will remain stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

Input-Output (Dropout) Voltage

A regulator's minimum input-to-output voltage differential (dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage. Because the device uses a PMOS, its dropout voltage is a function of drain-to-source on-resistance, $R_{DS(ON)}$, multiplied by the load current :

$$V_{DROPOUT} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT}$$

Current Limit

The RT9166/A monitors and controls the PMOS' gate voltage, minimum limiting the output current to 300mA for RT9166 and 600mA for RT9166A. The output can be shorted to ground for an indefinite period of time without damaging the part.

Short-Circuit Protection

The device is short circuit protected and in the event of a peak over-current condition, the short-circuit control loop will rapidly drive the output PMOS pass element off. Once the power pass element shuts down, the control loop will rapidly cycle the output on and off until the average power dissipation causes the thermal shutdown circuit to respond to servo the on/off cycling to a lower frequency. Please refer to the section on thermal information for power dissipation calculations.

Capacitor Characteristics

It is important to note that capacitance tolerance and variation with temperature must be taken into consideration when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range. In general, a good tantalum capacitor will show very little capacitance variation with temperature, but a ceramic may not be as good (depending on dielectric type).

Aluminum electrolytics also typically have large temperature variation of capacitance value.

Equally important to consider is a capacitor's ESR change with temperature: this is not an issue with ceramics, as their ESR is extremely low. However, it is very important in Tantalum and aluminum electrolytic capacitors. Both show increasing ESR at colder temperatures, but the increase in aluminum electrolytic capacitors is so severe they may not be feasible for some applications.

Ceramic :

For values of capacitance in the 10μF to 100μF range, ceramics are usually larger and more costly than tantalums but give superior AC performance for by-passing high frequency noise because of very low ESR (typically less than 10mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature.

Z5U and Y5V dielectric ceramics have capacitance that drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

X7R and X5R dielectric ceramic capacitors are strongly recommended if ceramics are used, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

Tantalum :

Solid tantalum capacitors are recommended for use on the output because their typical ESR is very close to the ideal value required for loop compensation. They also work well as input capacitors if selected to meet the ESR requirements previously listed.

Tantalums also have good temperature stability : a good quality tantalum will typically show a capacitance value that varies less than 10 to 15% across the full temperature range of 125°C to –40°C. ESR will vary only about 2X going from the high to low temperature limits.

The increasing ESR at lower temperatures can cause oscillations when marginal quality capacitors are used (if the ESR of the capacitor is near the upper limit of the stability range at room temperature).

Aluminum :

This capacitor type offers the most capacitance for the money. The disadvantages are that they are larger in physical size, not widely available in surface mount, and have poor AC performance (especially at higher frequencies) due to higher ESR and ESL.

Compared by size, the ESR of an aluminum electrolytic is higher than either Tantalum or ceramic, and it also varies greatly with temperature. A typical aluminum electrolytic can exhibit an ESR increase of as much as 50X when going from 25°C down to –40°C.

It should also be noted that many aluminum electrolytics only specify impedance at a frequency of 120Hz, which indicates they have poor high frequency performance. Only aluminum electrolytics that have an impedance specified at a higher frequency (between 20kHz and 100kHz) should be used for the device. Derating must be applied to the manufacturer's ESR specification, since it is typically only valid at room temperature.

Any applications using aluminum electrolytics should be thoroughly tested at the lowest ambient operating temperature where ESR is maximum.

Thermal Considerations

Thermal protection limits power dissipation in RT9166/A. When the operation junction temperature exceeds 170°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turn on again after the junction temperature cools by 40°C.

For continuous operation, do not exceed absolute maximum operation junction temperature. The power dissipation definition in device is :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can

be calculated by following formula :

$P_{D\,(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For SOT-23-3 package, the thermal resistance θ_{JA} is 250°C/W on the standard JEDEC 51-3 single-layer thermal test board. For SOT-223 package, the thermal resistance θ_{JA} is 135°C/W on the standard JEDEC 51-3 single-layer thermal test board. For SOT-89 package, the thermal resistance θ_{JA} is 175°C/W on the standard JEDEC 51-3 single-layer thermal test board. For TO-92 package, the thermal resistance θ_{JA} is 160°C/W on the standard JEDEC 51-3 single-layer thermal test board. For TO-252 package, the thermal resistance θ_{JA} is 68°C/W on the standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D\,(MAX)}$ = (125°C – 25°C) / 250°C/W = 0.400W for SOT-23-3 package

$P_{D\,(MAX)}$ = (125°C – 25°C) / 175°C/W = 0.571W for SOT-89 package

$P_{D\,(MAX)}$ = (125°C – 25°C) / 135°C/W = 0.740W for SOT-223 package

$P_{D\,(MAX)}$ = (125°C – 25°C) / 160°C/W = 0.625W for TO-92 package

$P_{D\,(MAX)}$ = (125°C – 25°C) / 68°C/W = 1.470W for TO-252 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. Figure 1 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

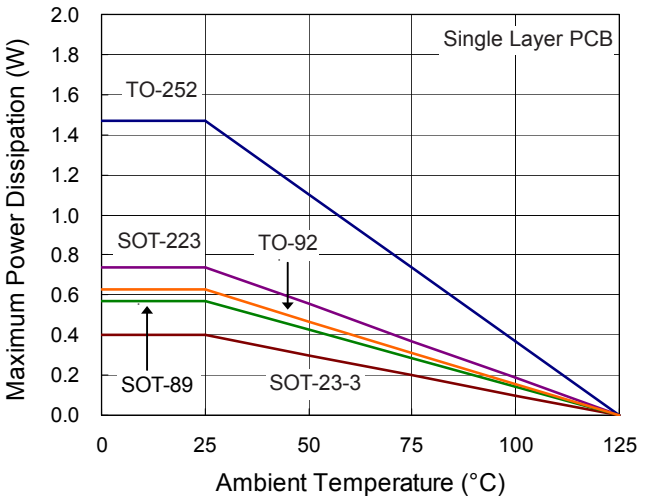


Figure 1. Derating Curve of Maximum Power Dissipation

PCB Layout

Good board layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors ***MUST*** be directly connected to the input, output, and ground pins of the device using traces which have no other currents flowing through them.

The best way to do this is to layout C_{IN} and C_{OUT} near the device with short traces to the V_{IN}, V_{OUT}, and ground pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a "single point ground".

It should be noted that stability problems have been seen in applications where "vias" to an internal ground plane were used at the ground points of the device and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single point ground technique for the regulator and it' s capacitors fixed the problem. Since high current flows through the traces going into V_{IN} and coming from V_{OUT}, Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

Optimum performance can only be achieved when the device is mounted on a PC board according to the diagram below :

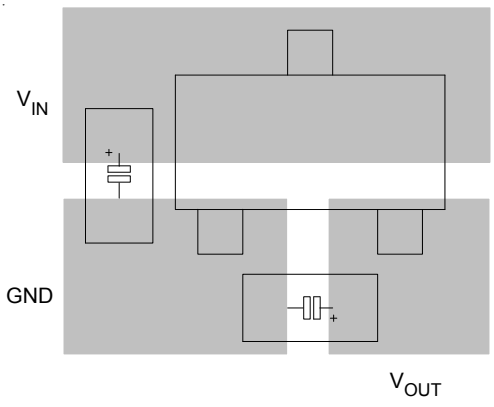
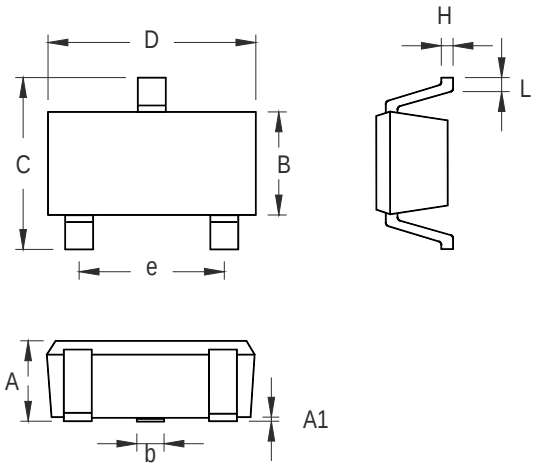


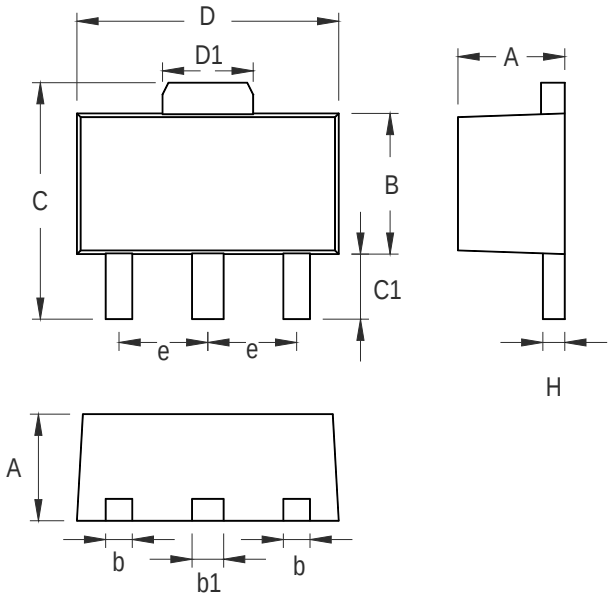
Figure 2. SOT-23-3 Board Layout

Outline Dimension



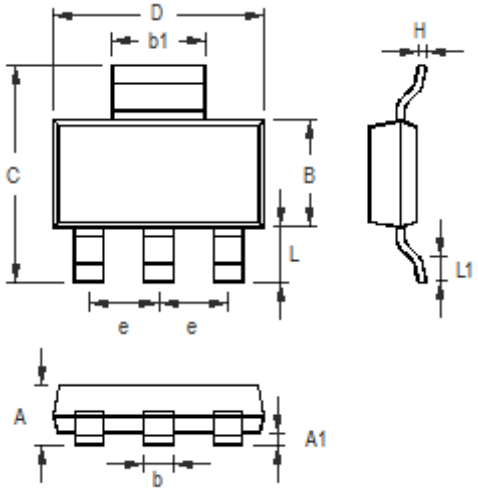
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.508	0.014	0.020
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	1.803	2.007	0.071	0.079
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-3 Surface Mount Package



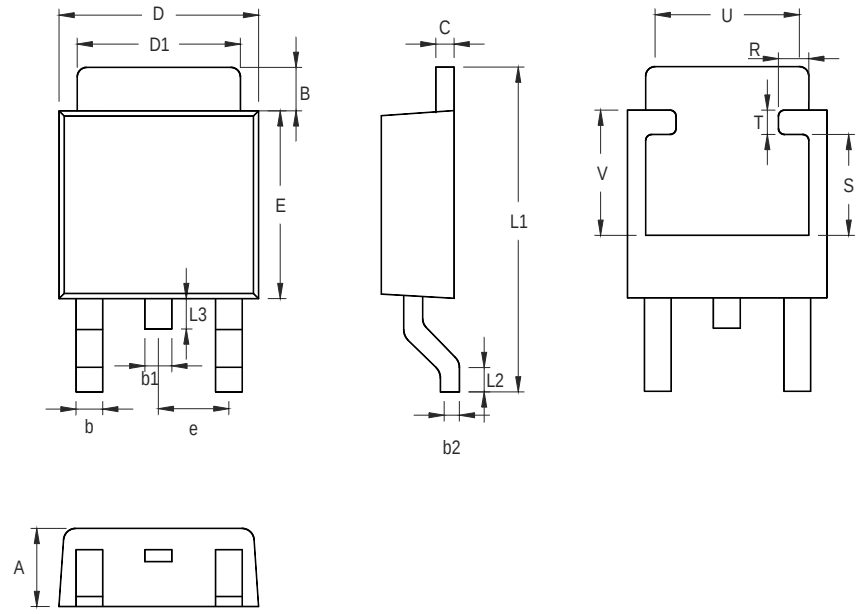
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.397	1.600	0.055	0.063
b	0.356	0.483	0.014	0.019
B	2.388	2.591	0.094	0.102
b1	0.406	0.533	0.016	0.021
C	3.937	4.242	0.155	0.167
C1	0.787	1.194	0.031	0.047
D	4.394	4.597	0.173	0.181
D1	1.397	1.753	0.055	0.069
e	1.448	1.549	0.057	0.061
H	0.356	0.432	0.014	0.017

3-Lead SOT-89 Surface Mount Package



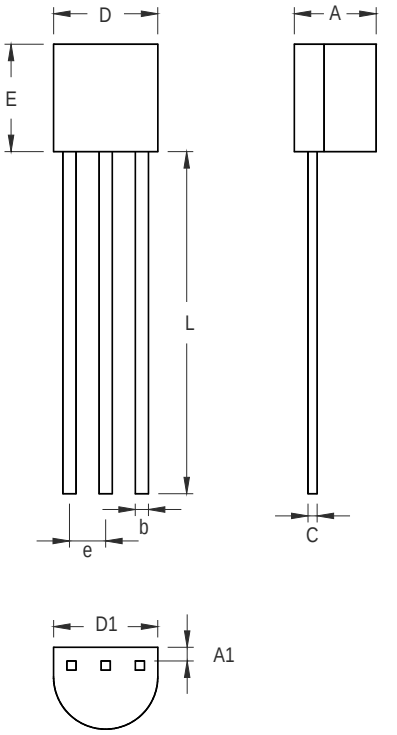
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.800	0.055	0.071
A1	0.020	0.100	0.001	0.004
b	0.600	0.840	0.024	0.033
B	3.300	3.700	0.130	0.146
C	6.700	7.300	0.264	0.287
D	6.300	6.700	0.248	0.264
b1	2.900	3.100	0.114	0.122
e	2.300		0.091	
H	0.230	0.350	0.009	0.014
L	1.500	2.000	0.059	0.079
L1	0.800	1.100	0.031	0.043

3-Lead SOT-223 Surface Mount Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.184	2.388	0.086	0.094
B	0.889	2.032	0.035	0.080
b	0.508	0.889	0.020	0.035
b1	1.016 Ref.		0.040 Ref.	
b2	0.457	0.584	0.018	0.023
C	0.457	0.584	0.018	0.023
D	6.350	6.731	0.250	0.265
D1	5.207	5.461	0.205	0.215
E	5.334	6.223	0.210	0.245
e	2.108	2.438	0.083	0.096
L1	9.398	10.414	0.370	0.410
L2	0.508 Ref.		0.020 Ref.	
L3	0.635	1.016	0.025	0.040
U	3.810 Ref.		0.150 Ref.	
V	3.048 Ref.		0.120 Ref.	
R	0.200	0.850	0.008	0.033
S	2.500	3.400	0.098	0.134
T	0.500	0.850	0.020	0.033

3-Lead TO-252 Surface Mount Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.175	4.191	0.125	0.165
A1	1.143	1.372	0.045	0.054
b	0.406	0.533	0.016	0.021
C	0.406	0.533	0.016	0.021
D	4.445	5.207	0.175	0.205
D1	3.429	5.029	0.135	0.198
E	4.318	5.334	0.170	0.210
e	1.143	1.397	0.045	0.055
L	12.700		0.500	

3-Lead TO-92 Plastic Package

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