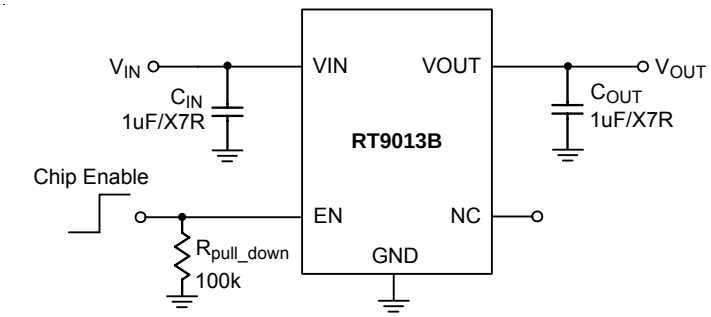
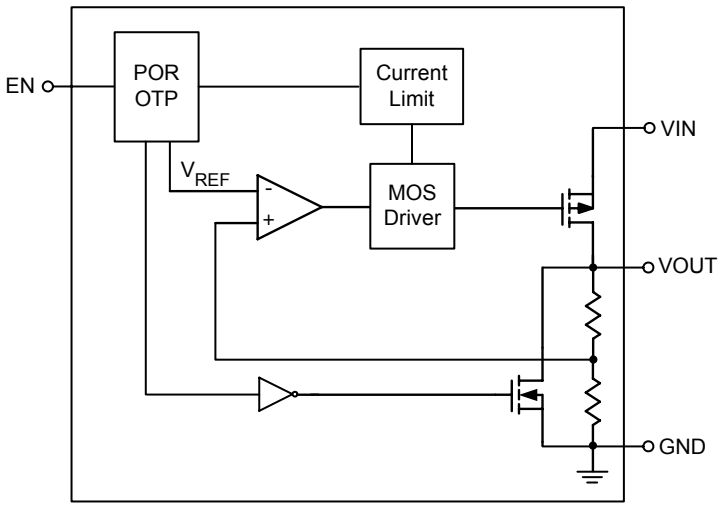
Typical Application Circuit



Functional Pin Description

Pin No.		Pin Name	Pin Function
SC-70-5	WDFN-6L 1.6x1.6		
1	3	VIN	Supply Input.
2	2, 7 (Exposed Pad)	GND	Common Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
3	1	EN	Chip Enable (Active High). It is recommended to add a 100kΩ resistor between the EN and GND.
4	5, 6	NC	No Internal Connection.
5	4	VOUT	Regulator Output.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- 6V
- EN Input Voltage ---------- 6V
- Power Dissipation, P_D @ T_A = 25°C
  - SC-70-5 ---------- 0.3W
  - WDFN-6L 1.6x1.6 ---------- 0.606W
- Package Thermal Resistance (Note 2)
  - SC-70-5, θ_{JA} ---------- 333°C/W
  - WDFN-6L 1.6x1.6, θ_{JA} ---------- 165°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM ---------- 2kV
  - MM ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.2V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = V_{OUT} + 0.5V, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 1uF/X7R (Ceramic), T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range		V_{IN}		2.2	--	5.5	V
Output Noise Voltage		V_{ON}	V_{OUT} = 1.5V	–	30	--	uV_{RMS}
Output Voltage Accuracy (Fixed Output Voltage)		ΔV_{OUT}	I_{OUT} = 10mA	–2	0	+2	%
Quiescent Current (Note 5)		I_Q	V_{EN} = 5V, I_{OUT} = 0mA	--	25	50	uA
Shutdown Current		I_{SHDN}	V_{EN} = 0V	--	0.7	1.5	uA
Current Limit		I_{LIM}	R_{LOAD} = 0Ω, 2.2V ≤ V_{IN} < 5.5V	300	400	600	mA
Dropout Voltage (Note 6)		V_{DROP}	I_{OUT} = 300mA	--	125	240	mV
Load Regulation (Note 7) (Fixed Output Voltage)		ΔV_{LOAD}	1mA < I_{OUT} < 300mA 2.2V ≤ V_{IN} < 2.7V	--	–	0.6	%
			1mA < I_{OUT} < 300mA 2.7V ≤ V_{IN} ≤ 5.5V	--	–	1	
EN Threshold	Logic-Low Voltage	V_{IL}		0	--	0.6	V
	Logic-High Voltage	V_{IH}		1.6	--	5.5	
Enable Pin Current		I_{EN}		--	0.1	1	uA
Power Supply Rejection Rate		PSRR	I_{OUT} = 100mA, f = 10kHz	–	–50	--	dB
Line Regulation		ΔV_{LINE}	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{OUT} = 1mA	–	0.01	0.2	%/V
Thermal Shutdown Temperature		T_{SD}		--	170	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	30	--	

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity single layer test board of JEDEC 51-3 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Quiescent, or ground current, is the difference between input and output currents. It is defined by $I_Q = I_{IN} - I_{OUT}$ under no load condition (I_{OUT} = 0mA). The total current drawn from the supply is the sum of the load current plus the ground pin current.

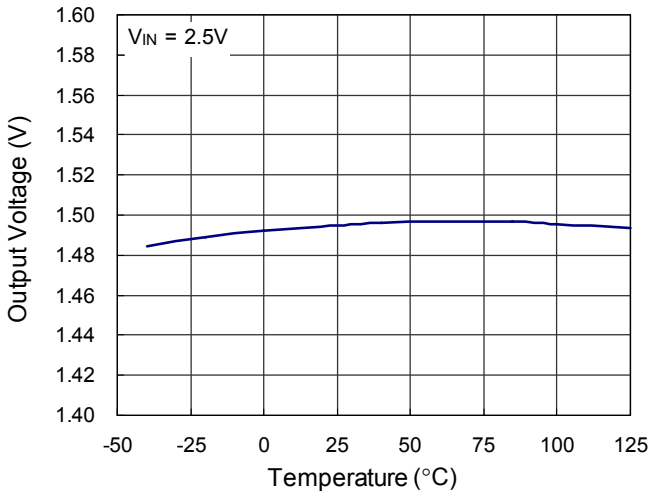
Note 6. The dropout voltage is defined as $V_{IN} - V_{OUT}$, which is measured when V_{OUT} is $V_{OUT(NORMAL)}$ - 100mV.

Note 7. Regulation is measured at constant junction temperature by using a 2ms current pulse. Devices are tested for load regulation in the load range from 10mA to 300mA.

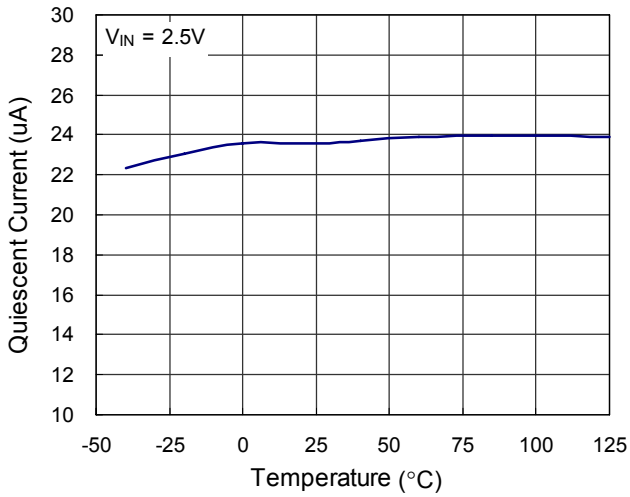
Typical Operating Characteristics

(C_{IN} = C_{OUT} = 1µ/X7R, unless otherwise specified)

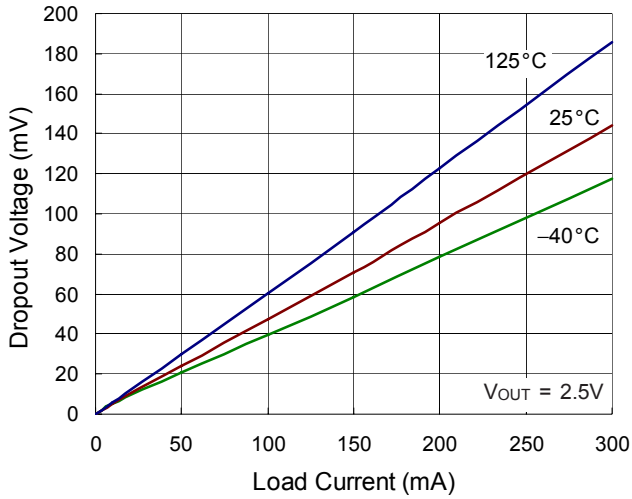
Output Voltage vs. Temperature



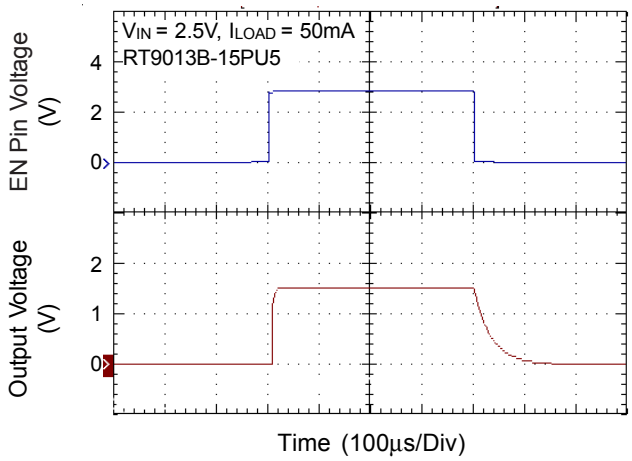
Quiescent Current vs. Temperature



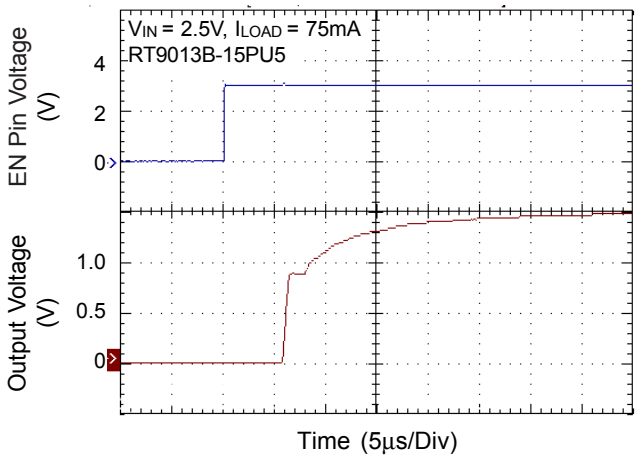
Dropout Voltage vs. Load Current



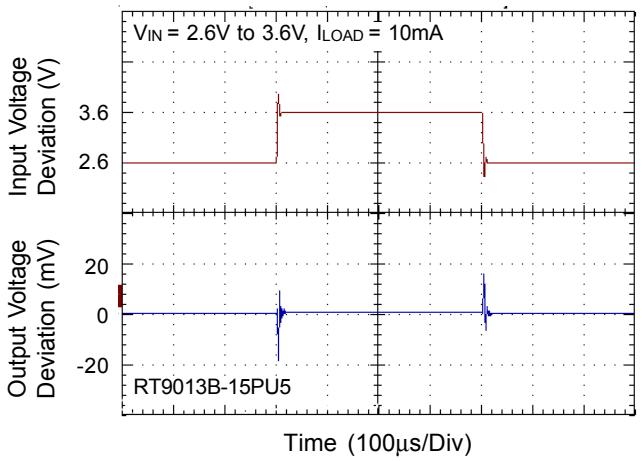
EN Pin Shutdown Response



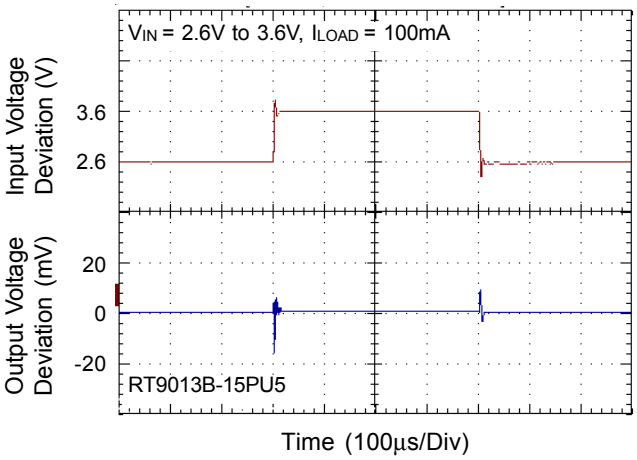
Start Up



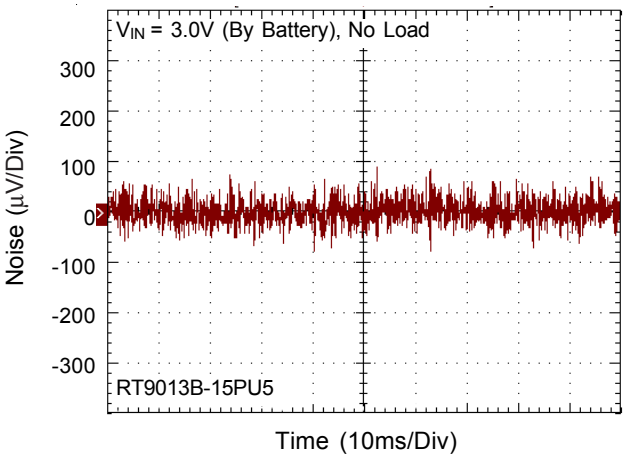
Line Transient Response



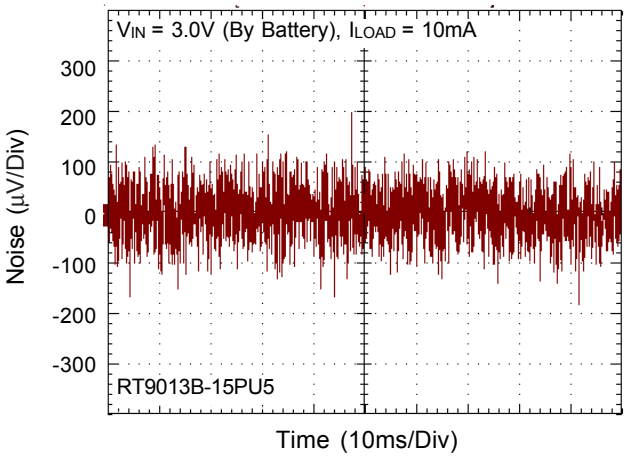
Line Transient Response



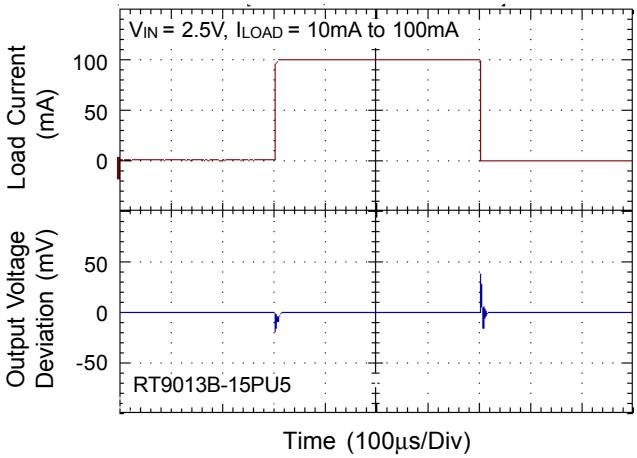
Noise



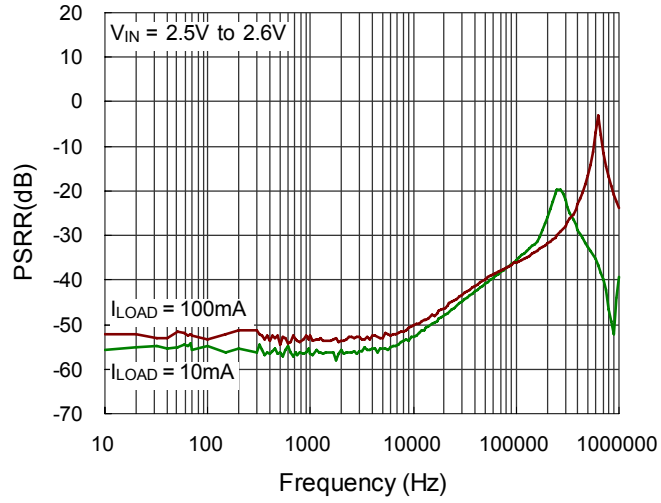
Noise



Load Transient Response



PSRR



Applications Information

Like any low-dropout regulator, the external capacitors used with the RT9013B must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 1uF / X7R on the RT9013B input and the amount of capacitance can be increased without limit. The input capacitor must be located at a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The RT9013B is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1uF with ESR is > 20mΩ on the RT9013B output ensures stability. The RT9013B still works well with output capacitor of other types due to the wide stable ESR range. Figure 1. shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the RT9013B and returned to a clean analog ground.

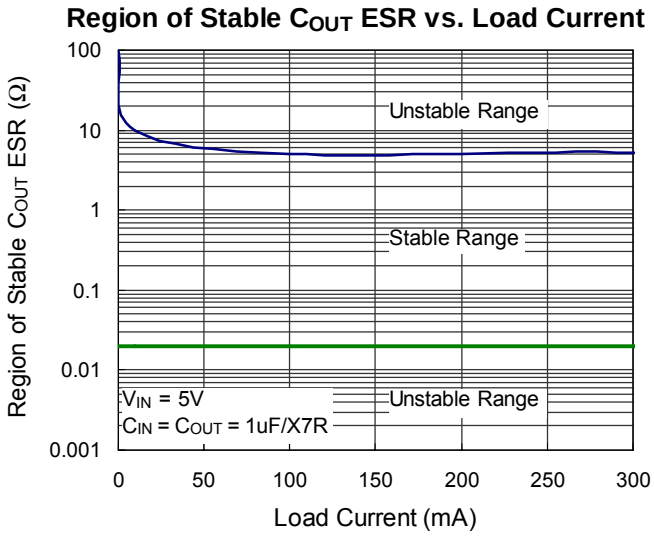


Figure 1

Enable

The RT9013B goes into sleep mode when the EN pin is in a logic low condition. During this condition, the RT9013B has an EN pin to turn on or turn off the regulator, When the EN pin is logic hight the regulator will be turned on. The supply current to 0.7uA typical. The EN pin may be directly tied to V_{IN} to keep the part on. The Enable input is CMOS logic and cannot be left floating.

PSRR

The power supply rejection ratio (PSRR) is defined as the gain from the input to output divided by the gain from the supply to the output. The PSRR is found to be

$$PSRR = 20 \times \log\left(\frac{\Delta Gain\,Error}{\Delta Supply}\right)$$

Note that in heavy load measuring, Δsupply will cause Δtemperature. And Δtemperature will cause Δoutput voltage. So the temperature effect is include in heavy load PSRR measuring.

Current Limit

The RT9013B contains an independent current limiter, which monitors and controls the pass transistor's gate voltage, limiting the output current to 0.4A (typ.). The output can be shorted to ground indefinitely without damaging the part.

Thermal Considerations

Thermal protection limits power dissipation in the RT9013B. When the operation junction temperature exceeds 170°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element will be turned on again after the junction temperature cools by 30°C.

For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in the device is calculated as follows :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between

junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of the RT9013B, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the operated ambient temperature. The junction to ambient thermal resistance for SC-70-5 package is 333°C/W and WDFN-6L 1.6x1.6 package is 165°C/W on the standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (333°C/W) = 0.3W for SC-70-5 packages

$P_{D(MAX)}$ = (125°C – 25°C) / (165°C/W) = 0.606W for WDFN-6L 1.6x1.6 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT9013B packages, the Figure 2 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

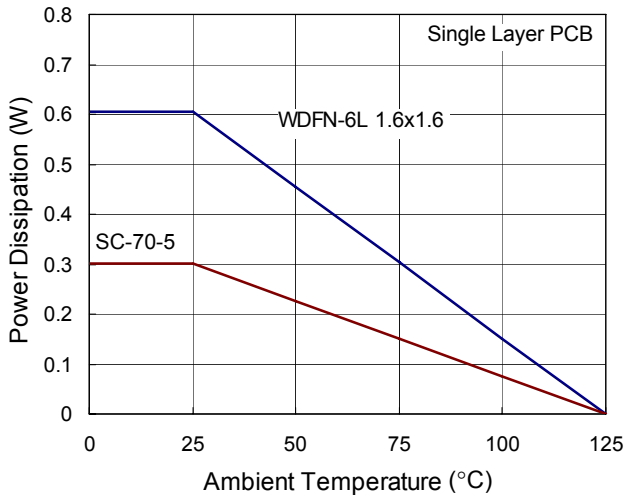
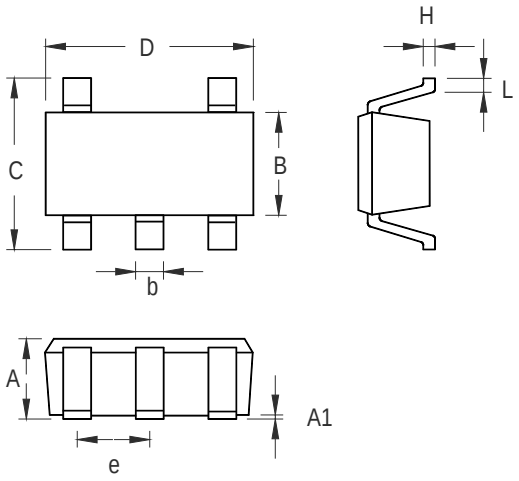


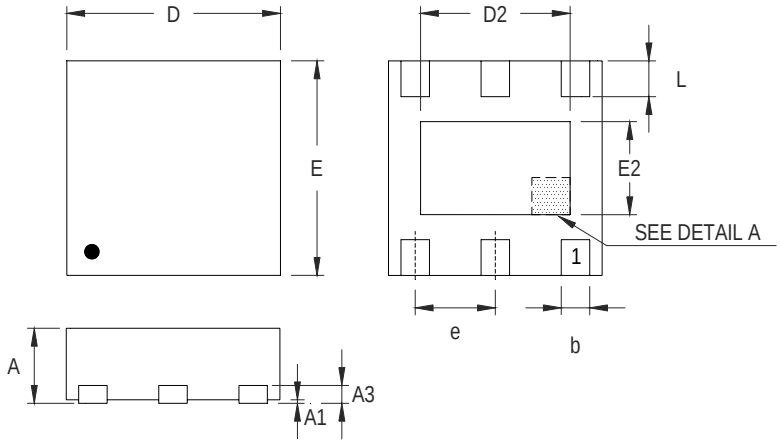
Figure 2. Derating Curves for RT9013B Packages

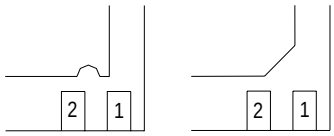
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.031	0.044
A1	0.000	0.100	0.000	0.004
B	1.150	1.350	0.045	0.054
b	0.150	0.400	0.006	0.016
C	1.800	2.450	0.071	0.096
D	1.800	2.250	0.071	0.089
e	0.650		0.026	
H	0.080	0.260	0.003	0.010
L	0.210	0.460	0.008	0.018

SC-70-5 Surface Mount Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.550	1.650	0.061	0.065
D2	0.950	1.050	0.037	0.041
E	1.550	1.650	0.061	0.065
E2	0.550	0.650	0.022	0.026
e	0.500		0.020	
L	0.190	0.290	0.007	0.011

W-Type 6L DFN 1.6x1.6 Package

Richtek Technology Corporation

Headquarter

5F, No. 20, Taiyuen Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation

Taipei Office (Marketing)

5F, No. 95, Minchiuan Road, Hsintien City

Taipei County, Taiwan, R.O.C.

Tel: (8862)86672399 Fax: (8862)86672377

Email: marketing@richtek.com