

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +4.6V
DC Input Voltage	-0.5V to $V_{CC} + 0.5V$
DC Output Current	120mA
Power Dissipation	0.5W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics for USB 2.0 Switching over Operating Range

($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 3.0 - 4.4V$)

Parameter	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed HIGH level	$V_{CC} = 4.2V$	1.8			V
			$V_{CC} = 3.3V$	1.6			
V_{IL}	Input LOW Voltage	Guaranteed HIGH level				0.8	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Max.}$, $I_{SEL} = -18\text{mA}$			-0.7	-1.2	
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$, $V_{SEL} = V_{CC}$				± 5	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}$, $V_{SEL} = \text{GND}$				± 5	
R_{ON}	Switch On-Resistance ⁽³⁾	$V_{CC} = \text{Min.}$, $-0.4V \leq V_{\text{input}} \leq 1.0V$, $I_{\text{INPUT}} = -40\text{mA}$			5.5	6.5	Ω
$R_{\text{FLAT(ON)}}$	On-Resistance Flatness ⁽³⁾	$V_{CC} = \text{Min.}$, $-0.4V \leq V_{\text{input}} \leq 1.0V$, $I_{\text{INPUT}} = -40\text{mA}$			1.5		
ΔR_{ON}	On-Resistance match from center ports to any other port ⁽³⁾	$V_{CC} = \text{Min.}$, $-0.4V \leq V_{\text{input}} \leq 1.0V$, $I_{\text{INPUT}} = -40\text{mA}$			0.9	2.0	

Notes:

- For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- $V_{CC} = 3.0 - 4.4V$, $T_A = 25^\circ\text{C}$ ambient and maximum loading.
- Measured by the voltage drop between D and D_n pin at indicated current through the Switch On-Resistance is determined by the lower of the voltages on the two (D, D_n) pins.

Power Supply Characteristics ($V_{CC} = 3.0 - 4.4V$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ.	Max.	Units
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, $V_{SEL} = \text{GND}$ or V_{CC}			1	μA

Notes:

- For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Parameters ⁽³⁾	Description	Test Conditions ⁽¹⁾	Typ. ⁽²⁾	Max.	Units
C_{IN}	Input Capacitance	$V_{SEL} = 0\text{V}$	3.6		pF
C_{OFF}	Port I Capacitance, Switch OFF		3.0		
C_{ON}	Switch Capacitance, Switch ON		5.5		

Dynamic Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	Min.	Typ. ⁽²⁾	Max.	Units
X_{TALK}	Crosstalk	$R_L = 50\Omega$, $f = 250\text{MHz}$		-40		dB
O_{IRR}	OFF Isolation			-34		
BW	-3dB Bandwidth	$R_L = 50\Omega$		1,000		MHz
BW	-0.5dB Bandwidth	$R_L = 50\Omega$		270		MHz

Notes:

- For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$ ambient and maximum loading.
- This parameter is determined by device characterization but is not production tested.

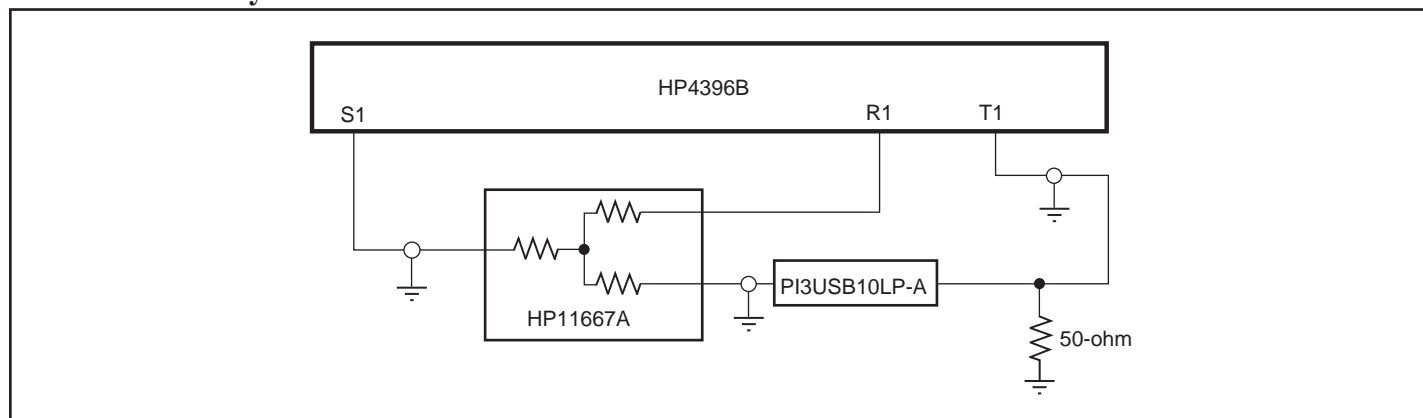
Switching Characteristics

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ.	Max.	Units
t_{PD}	Propagation Delay ^(2,3)	See Test Circuit for Electrical Characteristics		0.25		ns
t_{PZH} , t_{PZL}	Line Enable Time - SEL to D(+/-), D(+/-)n		0.5		15.0	
t_{PHZ} , t_{PLZ}	Line Disable Time - SEL to D(+/-), D(+/-)n		0.5		9.0	
t_{SKC-C}	Output skew, channel-to-channel ⁽²⁾			3.5	14	ps
t_{SKb-b}	Output skew, bit-to-bit (opposite transition of the same output (t_{PHL} - t_{PLH})) ⁽²⁾			7.5	20	

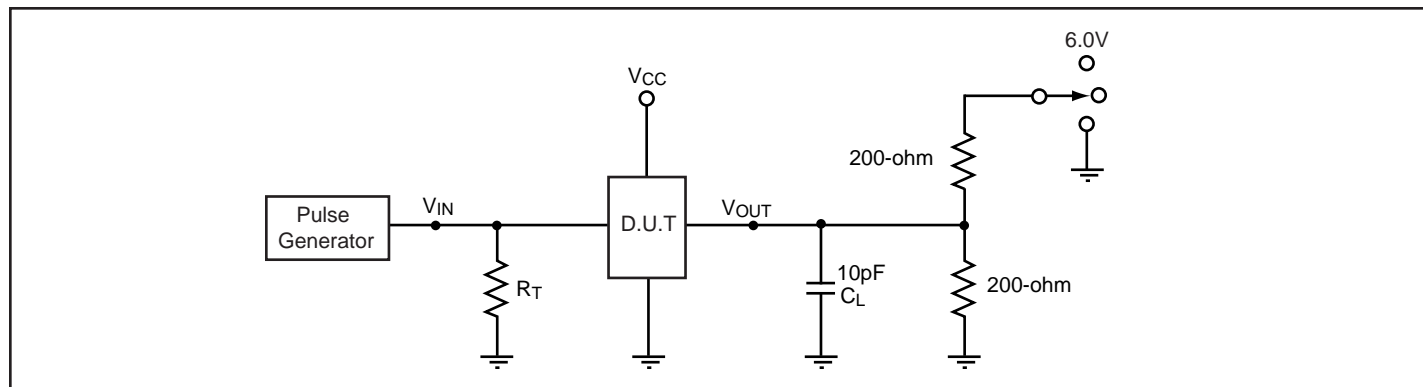
Notes:

- For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Guaranteed by design.
- The switch contributes no propagational delay other than the RC delay of the On-Resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for 10pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the switch when used in a system is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

Test Circuit for Dynamic Electrical Characteristics



Test Circuit for Electrical Characteristics



Notes:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

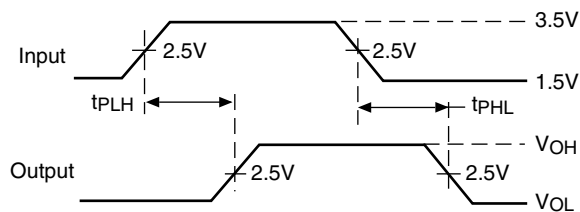
All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, Z_O = 50Ω, t_R ≤ 2.5ns, t_F ≤ 2.5ns.

The outputs are measured one at a time with on transition per measurement.

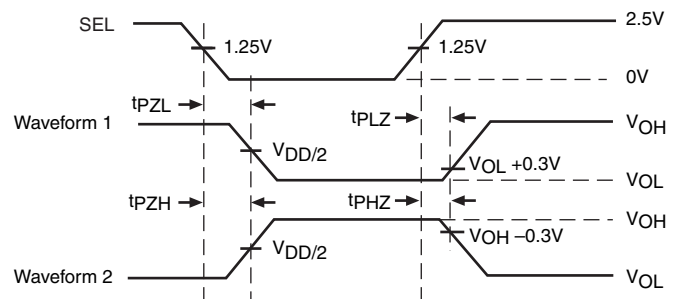
Switch Positions

Test	Switch
t _{PLZ} , t _{PZL} (output on I-side)	6.0V
t _{PHZ} , t _{PZH} (output on I-side)	GND
Prop Delay	Open

Switching Waveforms



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times

Applications Information

Logic Inputs

The logic control inputs can be driven up to +3.6V regardless of the supply voltage. For example, given a +3.3V supply, the output enables or select pins may be driven low to 0V and high to 3.6V. Driving IN Rail-to-Rail® minimizes power consumption.

Power Supply Sequencing

Proper power supply sequencing is recommended for all CMOS devices. Always apply VCC and GND before applying signals to input/output or control pins.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Eye Diagram Measurements

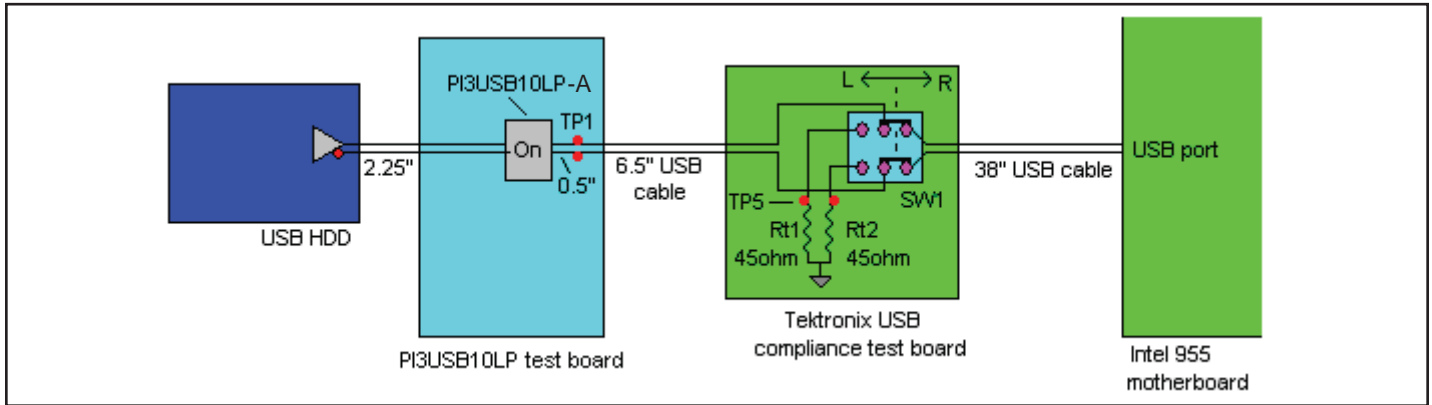


Figure 1: USB2.0 High-speed (480 Mbps) Signal Integrity Test Setup

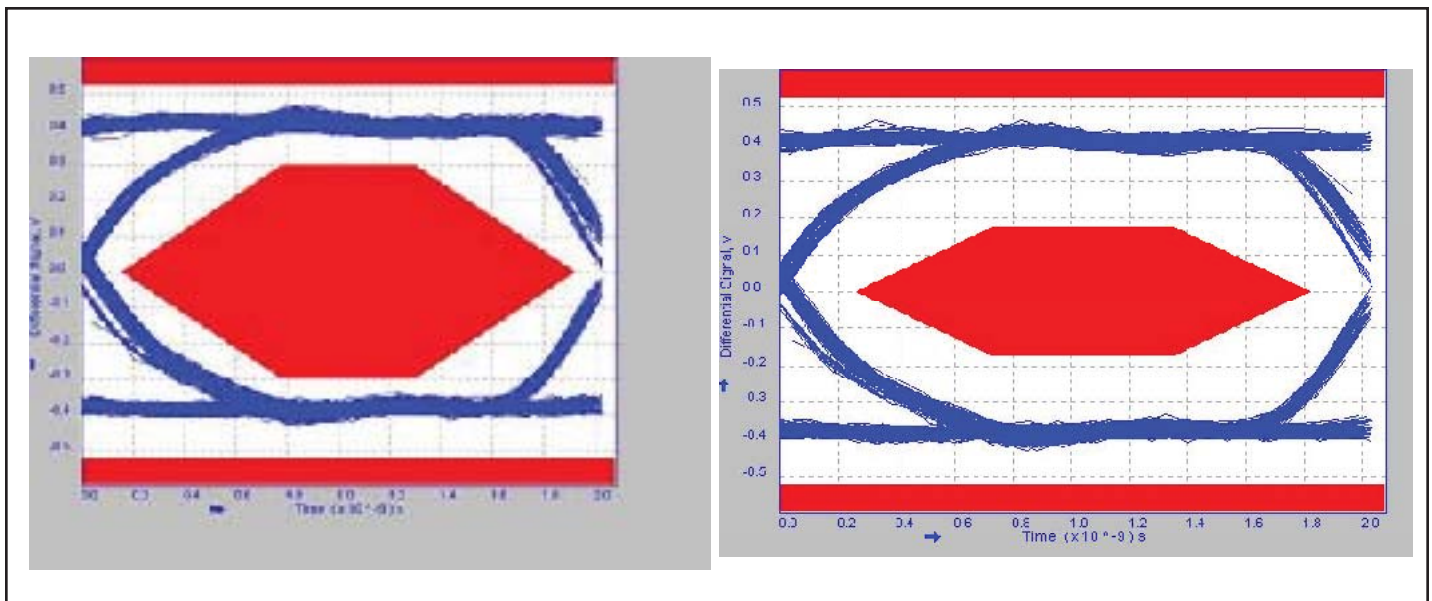
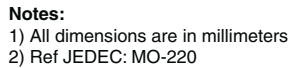
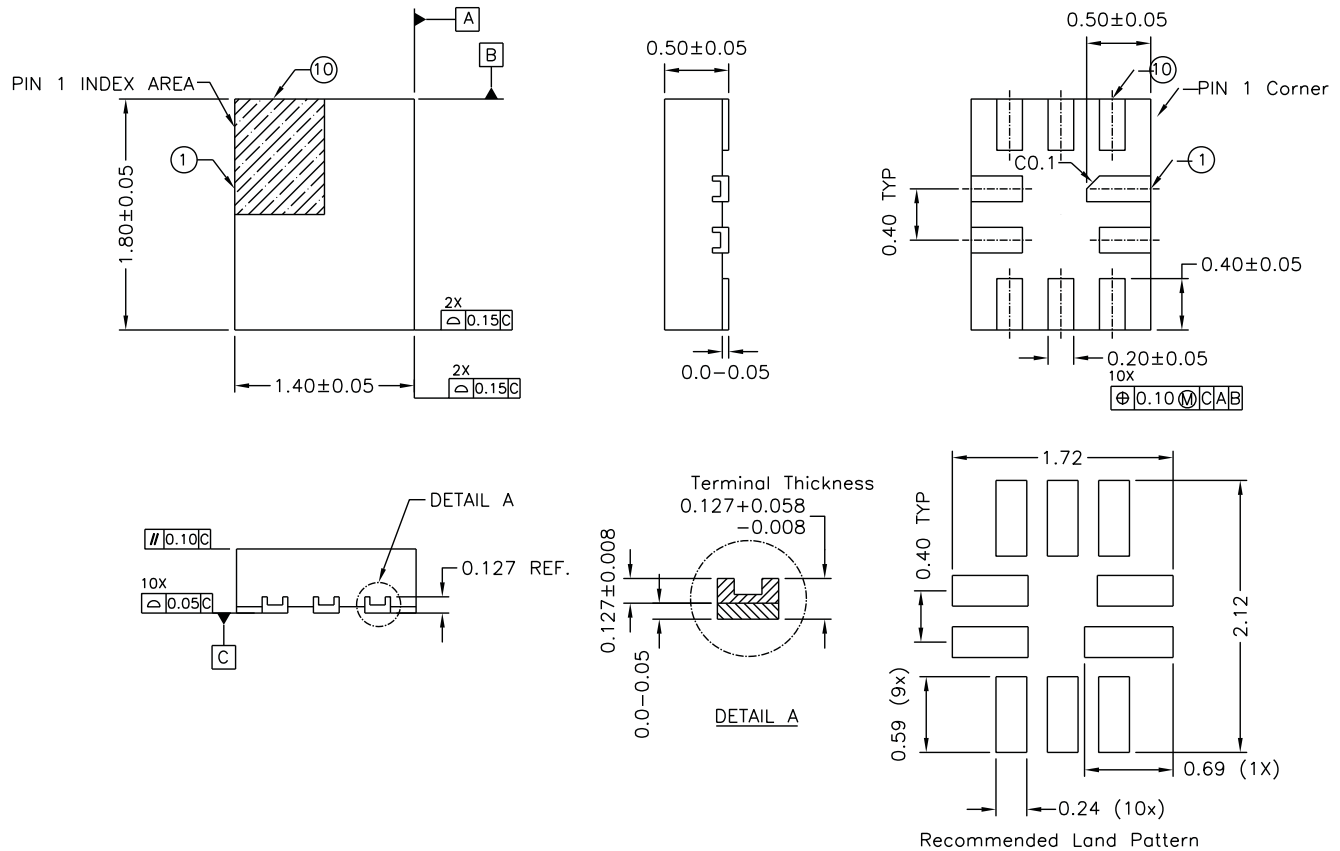


Figure 2: USB 2.0 High Speed (480Mbps) TP1, left eye, and TP5, right eye, with PI3USB10LP-A in the signal path



 PERICOM[®] Semiconductor Corporation		DATE: 03/20/06
DESCRIPTION: 10-Contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)		
PACKAGE CODE: ZL (ZL10)		
DOCUMENT CONTROL #: PD-2052		REVISION: A


NOTE :

1. All dimensions are in millimeters, angles in degrees
2. REFER JEDEC MO-220


DATE: 11/02/06
DESCRIPTION: 10-contact, Ultra Thin Quad Flat No-Lead (UQFN10L)
PACKAGE CODE: ZM10
DOCUMENT CONTROL #: PD-2066
REVISION: -
Ordering Information

Ordering Code	Package Code	Package Description	Top Mark
PI3USB10LP-AZLE	ZL	Pb-free & Green, 10-contact TQFN	AP
PI3USB10LP-AZME	ZM	Pb-free & Green, 10-contact UQFN	AP

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding X suffix = Tape/Reel