

## NDT014

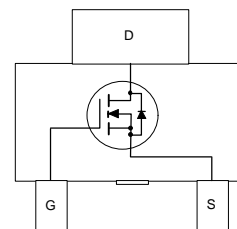
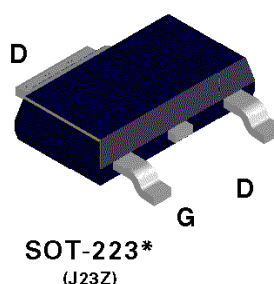
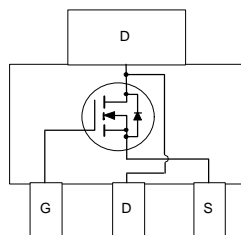
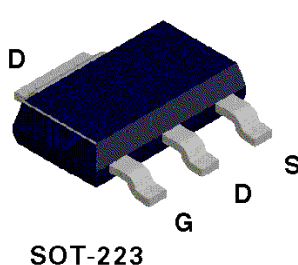
### N-Channel Enhancement Mode Field Effect Transistor

#### General Description

Power SOT N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

#### Features

- 2.7A, 60V.  $R_{DS(ON)} = 0.2\Omega$  @  $V_{GS} = 10V$ .
- High density cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability in a widely used surface mount package.



#### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDT014	Units
$V_{DS}$	Drain-Source Voltage	60	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous (Note 1a)	$\pm 2.7$	A
	- Pulsed	$\pm 10$	
$P_D$	Maximum Power Dissipation (Note 1a)	3	W
	(Note 1b)	1.3	
	(Note 1c)	1.1	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-65 to 150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	42	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	12	$^\circ\text{C/W}$

\* Order option J23Z for cropped center drain lead.

# Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			25	μA
		V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> =125°C			250	μA
I <sub>GSSF</sub>	Gate - Body Leakage, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate - Body Leakage, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	3	4	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.6 A		0.18	0.2	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 25 V, I <sub>D</sub> = 1.6 A		2		S
DYNAMIC CHARACTERISTICS						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		155		pF
C <sub>oss</sub>	Output Capacitance			60		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			15		pF
SWITCHING CHARACTERISTICS (Note 2)						
t <sub>D(on)</sub>	Turn - On Delay Time	V <sub>DD</sub> =30 V, I <sub>D</sub> = 10 A, V <sub>GEN</sub> = 10 V, R <sub>GEN</sub> = 24 Ω		10	20	ns
t <sub>r</sub>	Turn - On Rise Time			64	100	ns
t <sub>D(off)</sub>	Turn - Off Delay Time			10	20	ns
t <sub>f</sub>	Turn - Off Fall Time			10	20	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 48 V, I <sub>D</sub> = 10 A, V <sub>GS</sub> = 10 V		5	11	nC
Q <sub>gs</sub>	Gate-Source Charge			1.2	3.1	nC
Q <sub>gd</sub>	Gate-Drain Charge			2	5.8	nC

# Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				2.7	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				22	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.7A (Note 2)		0.95	1.6	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>F</sub> = 10 A, dI <sub>F</sub> /dt = 100 A/μs			140	ns

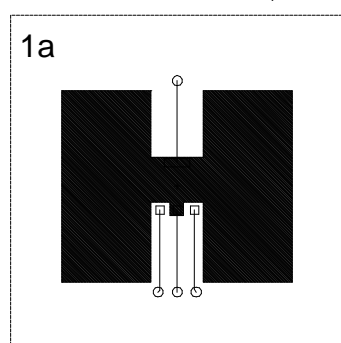
Notes:

- R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.

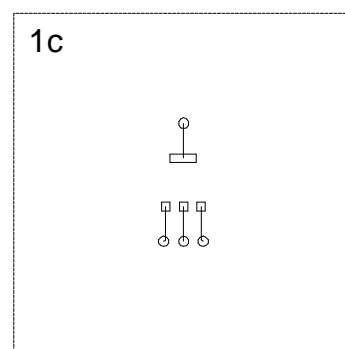
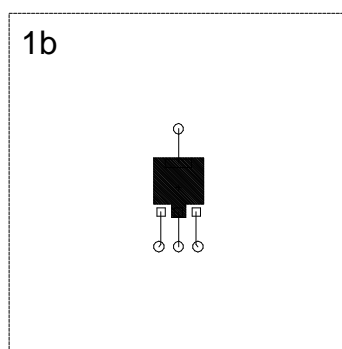
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta J} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(on)} @ T_J$$

Typical R<sub>θJA</sub> using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- 42°C/W when mounted on a 1 in<sup>2</sup> pad of 2oz copper.
- 95°C/W when mounted on a 0.066 in<sup>2</sup> pad of 2oz copper.
- 110°C/W when mounted on a 0.0123 in<sup>2</sup> pad of 2oz copper.



Scale 1 : 1 on letter size paper



- Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

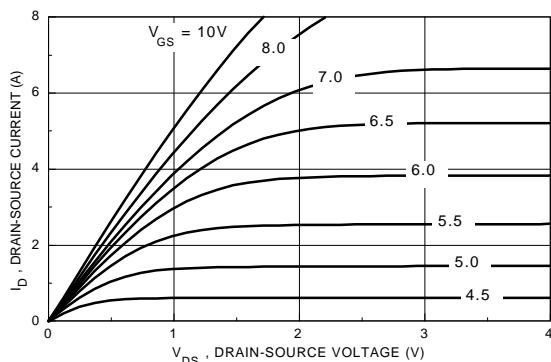


Figure 1. On-Region Characteristics.

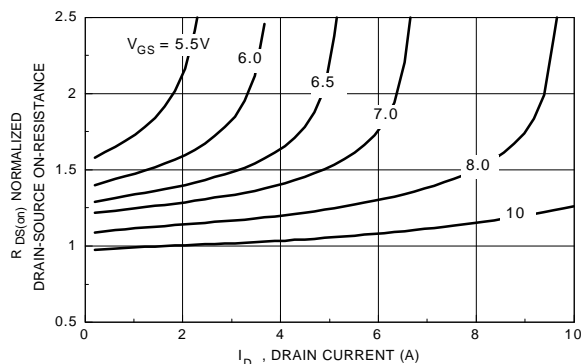


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

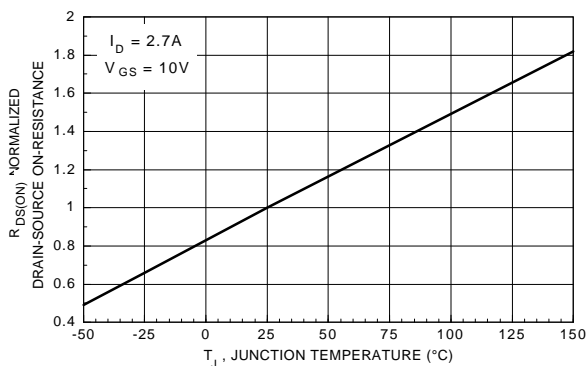


Figure 3. On-Resistance Variation with Temperature.

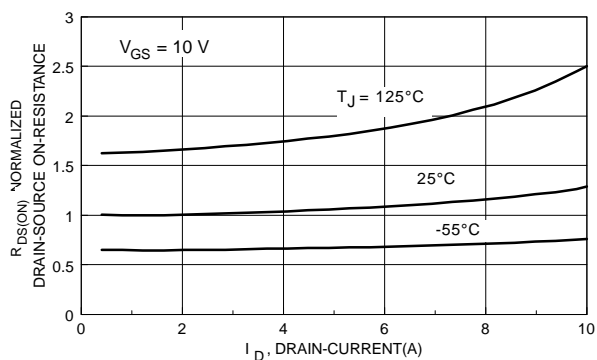


Figure 4. On-Resistance Variation with Drain Current and Temperature.

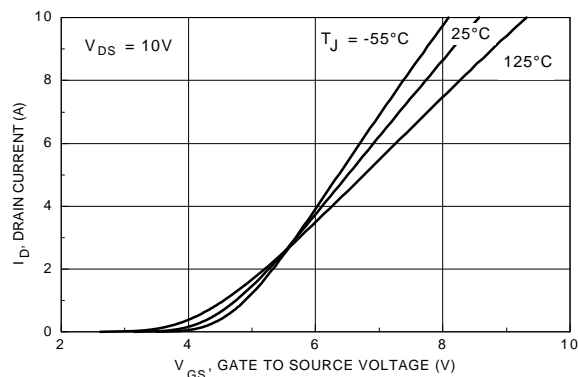


Figure 5. Transfer Characteristics.

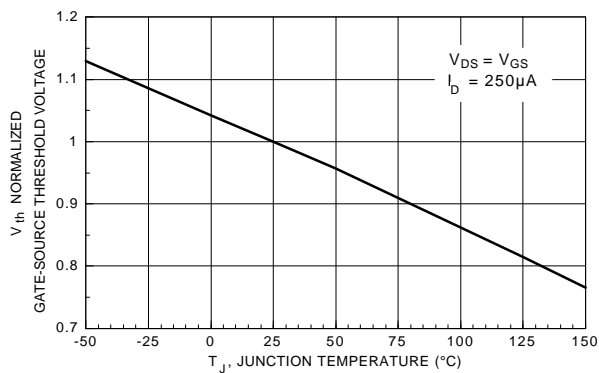


Figure 6. Gate Threshold Variation with Temperature.

## Typical Electrical Characteristics (continued)

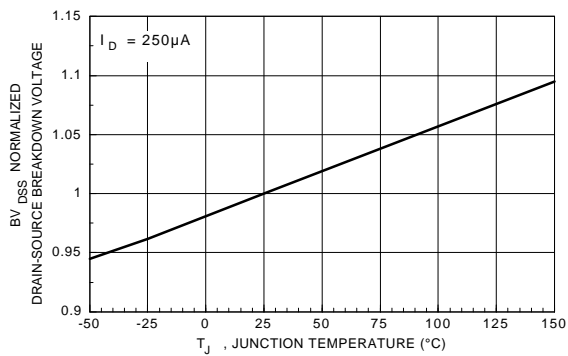


Figure 7. Breakdown Voltage Variation with Temperature.

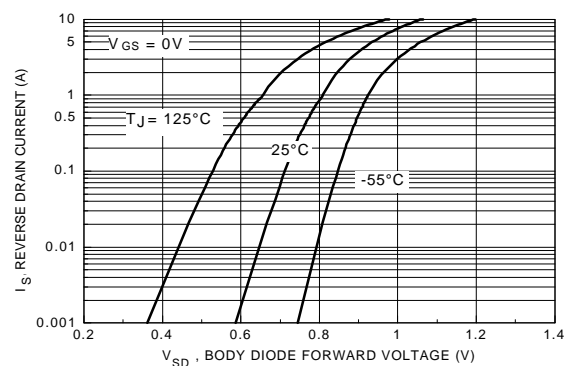


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

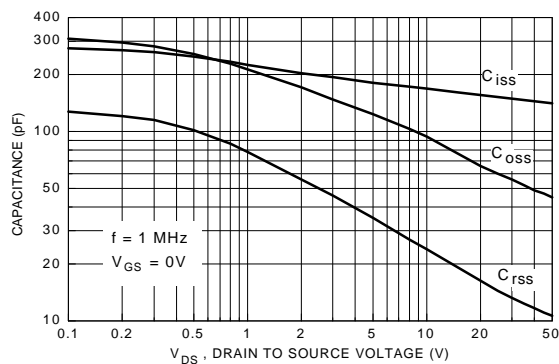


Figure 9. Capacitance Characteristics.

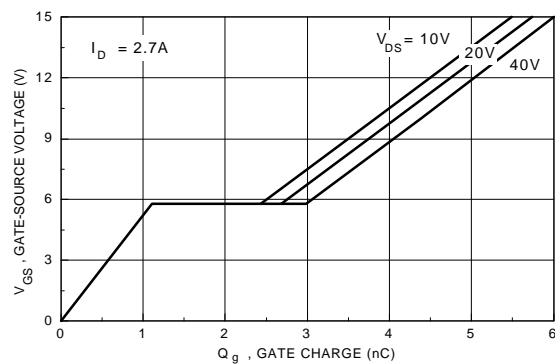


Figure 10. Gate Charge Characteristics.

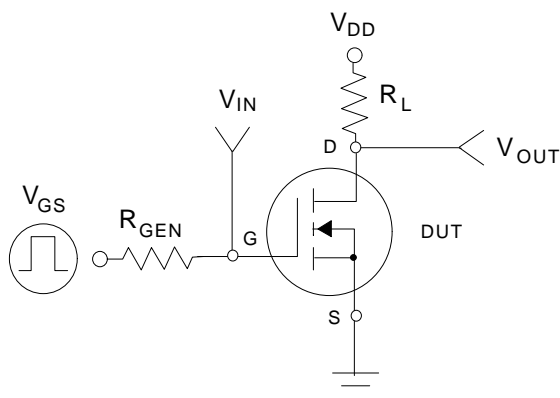


Figure 11. Switching Test Circuit.

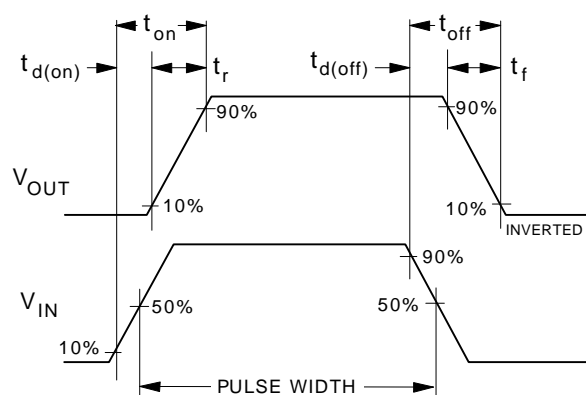
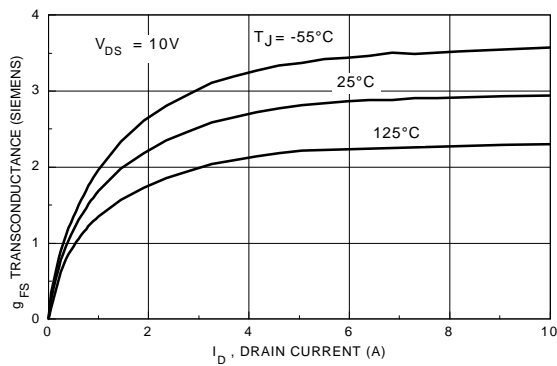
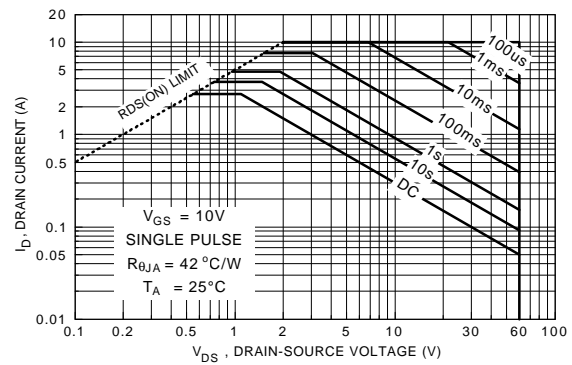


Figure 12. Switching Waveforms.

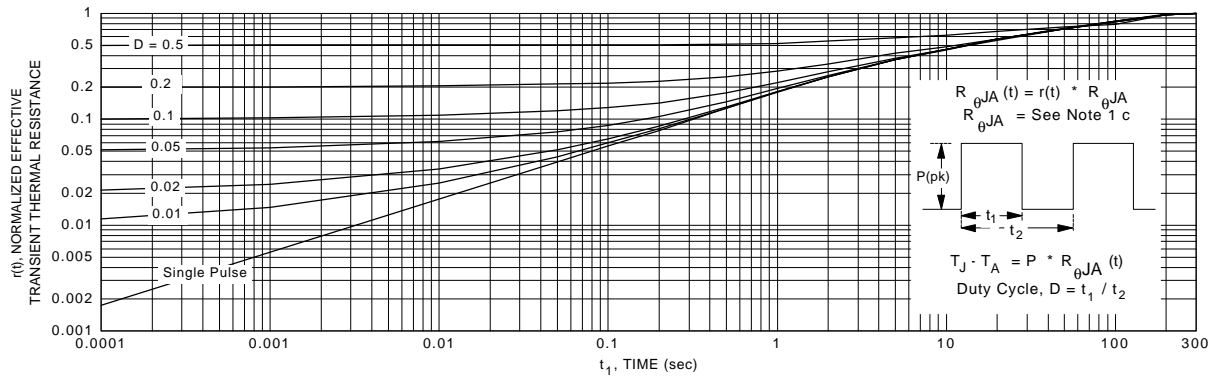
## Typical Electrical Characteristics (continued)



**Figure 13. Transconductance Variation with Drain Current and Temperature.**

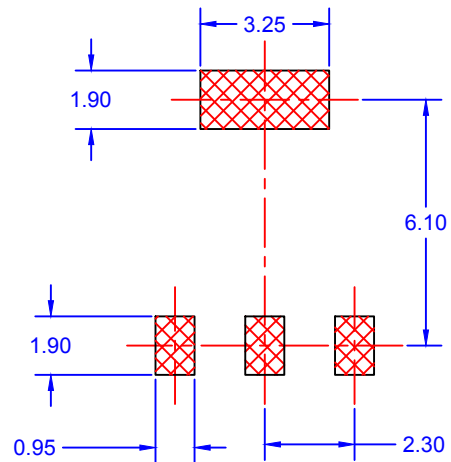
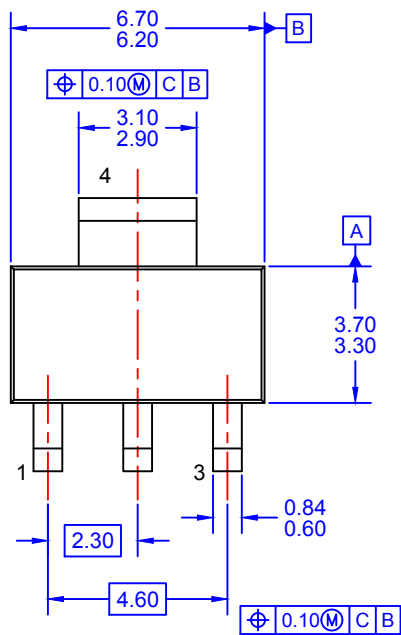


**Figure 14. Maximum Safe Operating Area.**

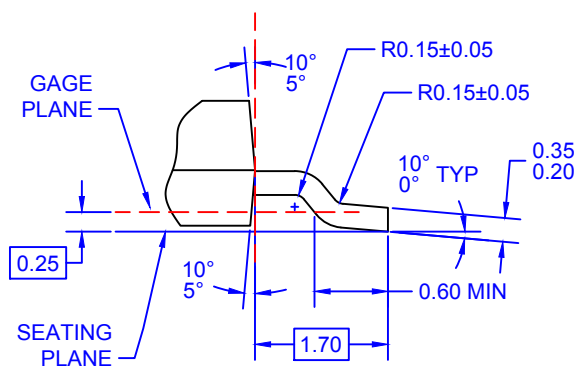
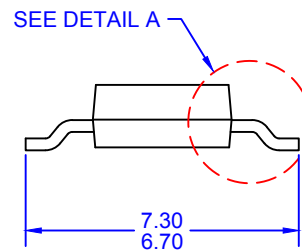
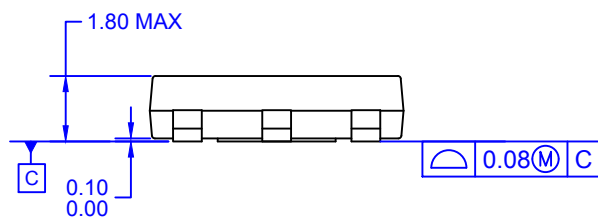


**Figure 15. Transient Thermal Response Curve.**

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.



LAND PATTERN RECOMMENDATION



**DETAIL A**  
**SCALE: 2:1**

**NOTES: UNLESS OTHERWISE SPECIFIED**

- A) DRAWING BASED ON JEDEC REGISTRATION TO-261C, VARIATION AA.**
- B) ALL DIMENSIONS ARE IN MILLIMETERS.**
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.**
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.**
- E) LANDPATTERN NAME: SOT230P700X180-4BN**
- F) DRAWING FILENAME: MKT-MA04AREV3**



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