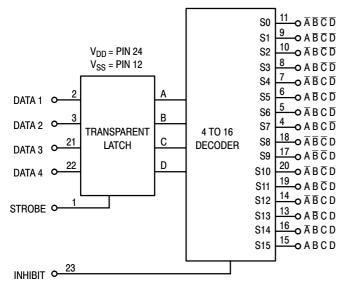
### **BLOCK DIAGRAM**



### **DECODE TRUTH TABLE** (Strobe = 1)\*

	Data Inputs				Selected Output
Inhibit	D	с	в	A	MC14514 = Logic "1" MC14515 = Logic "0"
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	Х	Х	х	х	All Outputs = 0, MC14514 All Outputs = 1, MC14515

X = Don't Care \*Strobe = 0, Data is latched

## **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>		
MC14514BCP	PDIP-24			
MC14514BCPG	PDIP-24 (Pb-Free)	15 Units / Rail		
MC14514BDW	SOIC-24	30 Units / Rail		
MC14514BDWR2	SOIC-24			
MC14514BDWR2G	SOIC-24 (Pb-Free)	1000 / Tape & Reel		
MC14515BCP	PDIP-24			
MC14515BCPG	PDIP-24 (Pb-Free)	15 Units / Rail		
MC14515BDW	SOIC-24	30 Units / Rail		
MC14515BDWR2	SOIC-24			
MC14515BDWR2G	SOIC-24 (Pb-Free)	1000 / Tape & Reel		

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS	(Voltages Referenced to V <sub>SS</sub> )
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			- 5	5°C		25°C		12	5°C	
Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Max	Min	Typ (Note 2)	Max	Min	Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V <sub>OL</sub>	5.0 10 15	- - -	0.05 0.05 0.05	_ _ _	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
"1" Level $V_{in} = 0$ or $V_{DD}$	V <sub>OH</sub>	5.0 10 15	4.95 9.95 14.95	_ _ _	4.95 9.95 14.95	5.0 10 15	_ _ _	4.95 9.95 14.95	_ _ _	Vdc
$\label{eq:VO} \begin{array}{llllllllllllllllllllllllllllllllllll$	VIL	5.0 10 15	_ _ _	1.5 3.0 4.0	 	2.25 4.50 6.75	1.5 3.0 4.0	_ _ _	1.5 3.0 4.0	Vdc
"1" Level ( $V_O = 0.5 \text{ or } 4.5 \text{ Vdc}$ ) ( $V_O = 1.0 \text{ or } 9.0 \text{ Vdc}$ ) ( $V_O = 1.5 \text{ or } 13.5 \text{ Vdc}$ )	V <sub>IH</sub>	5.0 10 15	3.5 7.0 11	_ _ _	3.5 7.0 11	2.75 5.50 8.25	_ _ _	3.5 7.0 11	_ _ _	Vdc
$\begin{array}{l} \text{Output Drive Current} \\ (V_{OH} = 2.5 \ \text{Vdc}) \\ (V_{OH} = 4.6 \ \text{Vdc}) \\ (V_{OH} = 9.5 \ \text{Vdc}) \\ (V_{OH} = 13.5 \ \text{Vdc}) \end{array}$	I <sub>ОН</sub>	5.0 5.0 10 15	- 1.2 - 0.25 - 0.62 - 1.8	- - -	- 1.0 - 0.2 - 0.5 - 1.5	- 1.7 - 0.36 - 0.9 - 3.5	- - -	- 0.7 - 0.14 - 0.35 - 1.1		mAdc
	I <sub>OL</sub>	5.0 10 15	0.64 1.6 4.2	- - -	0.51 1.3 3.4	0.88 2.25 8.8	- - -	0.36 0.9 2.4	- - -	mAdo
Input Current	l <sub>in</sub>	15	-	± 0.1	-	±0.00001	± 0.1	-	± 1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0 10 15		5.0 10 20	_ _ _	0.005 0.010 0.015	5.0 10 20	- - -	150 300 600	μAdc
Total Supply Current (Note 3, 4) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	ITL	5.0 10 15			$I_{T} = (2$	.35 μΑ/kHz) .70 μΑ/kHz) .05 μΑ/kHz)	f + I <sub>DD</sub>			μAdc

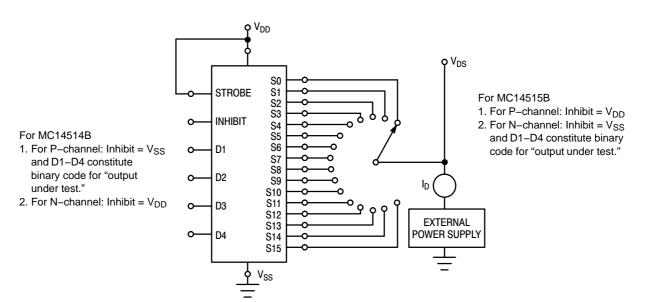
Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
The formulas given are for the typical characteristics only at 25°C.
To calculate total supply current at loads other than 50 pF: I<sub>T</sub>(C<sub>L</sub>) = I<sub>T</sub>(50 pF) + (C<sub>L</sub> - 50) Vfk where: I<sub>T</sub> is in µA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.002.

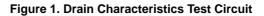
## **SWITCHING CHARACTERISTICS** (Note 5) ( $C_L = 50 \text{ pF}, T_A = 25^{\circ}C$ )

			All Types			
Characteristic	Symbol	V <sub>DD</sub>	Min	Typ (Note 6)	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	t <sub>TLH</sub>	5.0 10 15	- - -	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t <sub>THL</sub>	5.0 10 15	_ _ _	100 50 40	200 100 80	ns
Propagation Delay Time; Data, Strobe to S $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 465 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.86 \text{ ns/pF}) C_L + 192 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 125 \text{ ns}$	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0 10 15	- - -	550 225 150	1100 450 300	ns
Inhibit Propagation Delay Times $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 117 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0 10 15	- - -	400 150 100	800 300 200	ns
Setup Time Data to Strobe	t <sub>su</sub>	5.0 10 15	250 100 75	125 50 38	- - -	ns
Hold Time Strobe to Data	t <sub>h</sub>	5.0 10 15	- 20 0 10	- 100 - 40 - 30	- - -	ns
Strobe Pulse Width	twn	5.0 10 15	350 100 75	175 50 38		ns

5. The formulas given are for the typical characteristics only at  $25^{\circ}$ C.

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.





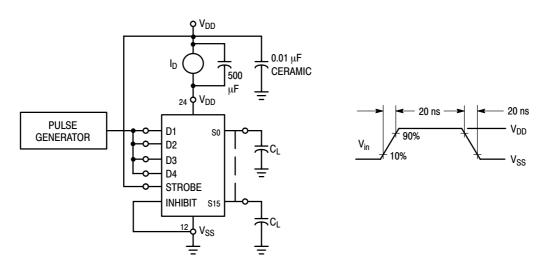


Figure 2. Dynamic Power Dissipation Test Circuit and Waveform

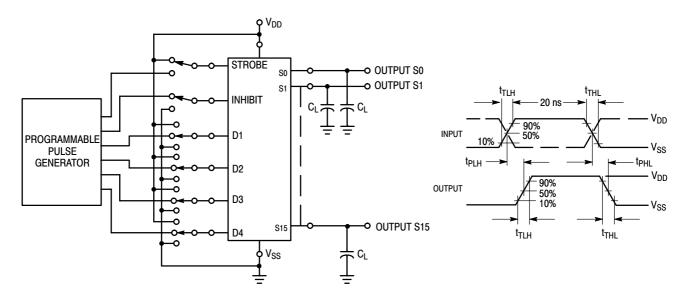
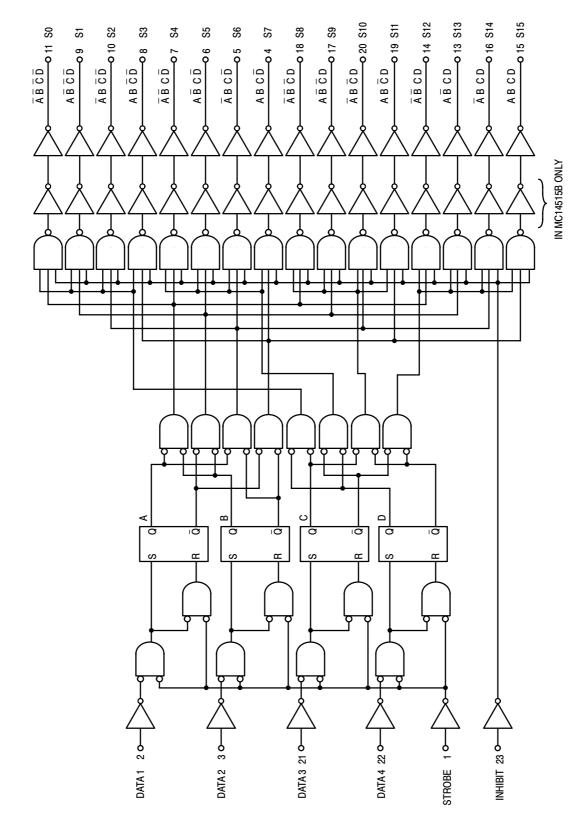


Figure 3. Switching Time Test Circuit and Waveforms



LOGIC DIAGRAM

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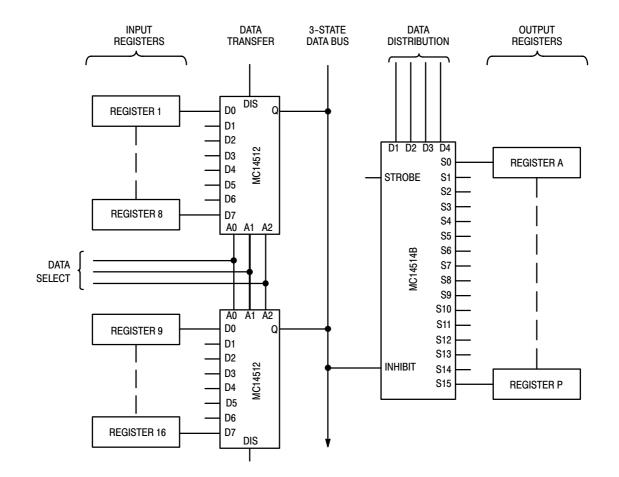
### COMPLEX DATA ROUTING

Two MC14512 eight–channel data selectors are used here with the MC14514B four–bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a 3–state data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re–routed or intermixed according to patterns determined by data select and distribution inputs.

Data is placed into the routing scheme via the eight inputs on both MC14512 data selectors. One register is assigned to each input. The signals on A0, A1, and A2 choose one of eight inputs for transfer out to the 3–state data bus. A fourth signal, labelled Dis, disables one of the MC14512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1 thru 16, the rate of transfer of the sequential information can also be varied. That is, if the MC14512 were addressed at a rate that is eight times faster then the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

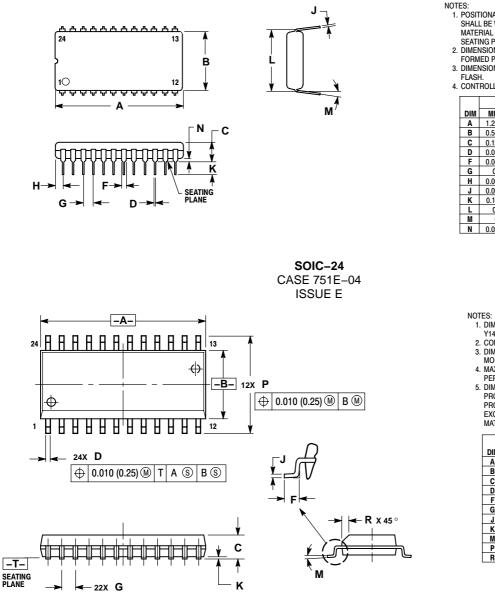
Information from the 3–state bus is redistributed by the MC14514B four–bit latch/decoder. Using the four–bit address, D1 thru D4, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A thru P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.



#### DATA ROUTING SYSTEM

### PACKAGE DIMENSIONS

PDIP-24 CASE 709-02 ISSUE D



1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO

SEATING PLANE AND EACH OTHER. 2. DIMENSION L TO CENTER OF LEADS WHEN

FORMED PARALLEL. 3. DIMENSION B DOES NOT INCLUDE MOLD

4 CONTROLLING DIMENSION: INCH

	INC	HES	MILLIMETERS		
DIM	MIN MAX		MIN	MAX	
Α	1.235	1.265	31.37	32.13	
В	0.540	0.560	13.72	14.22	
С	0.155	0.200	3.94	5.08	
D	0.014	0.022	0.36	0.56	
F	0.040	0.060	1.02	1.52	
G	0.100	BSC	2.54 BSC		
Н	0.065	0.080	1.65	2.03	
J	0.008	0.015	0.20	0.38	
Κ	0.115	0.135	2.92	3.43	
L	0.600	BSC	15.24 BSC		
Μ	0 °	15°	0 °	15°	
Ν	0.020	0.040	0.51	1.02	

1. DIMENSIONING AND TOLERANCING PER ANSI

Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER.

DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE

5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	15.25	15.54	0.601	0.612	
В	7.40	7.60	0.292	0.299	
С	2.35	2.65	0.093	0.104	
D	0.35	0.49	0.014	0.019	
F	0.41	0.90	0.016	0.035	
G	1.27	BSC	0.050 BSC		
J	0.23	0.32	0.009	0.013	
K	0.13	0.29	0.005	0.011	
Μ	0 °	8 °	0 °	8 °	
Ρ	10.05	10.55	0.395	0.415	
R	0.25	0.75	0.010	0.029	
•					

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