

One-to-Four LVCMOS-to-LVPECL Output Clock and Data Driver

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND -0.3V to +4.0V
 $\overline{Q_0}$, $\overline{Q_1}$, CLK $_0$, CLK_SEL,
 CLK_EN to GND -0.3V to (V_{CC} + 0.3V)
 Continuous Output Current 50mA
 Surge Output Current 100mA
 Continuous Power Dissipation (T_A = +70°C)
 20-Pin TSSOP (derate 11mW/°C) 879.1mW
 20-Pin 4mm x 4mm Thin QFN (derate 16.9mW/°C) ... 1349.1mW
 Junction-to-Ambient Thermal Resistance in Still Air
 20-Pin TSSOP +91°C/W
 20-Pin 4mm x 4mm Thin QFN +59.3°C/W

Junction-to-Case Thermal Resistance
 20-Pin TSSOP +20°C/W
 20-Pin 4mm x 4mm Thin QFN +2°C/W
 Operating Temperature Range -40°C to +85°C
 Junction Temperature +150°C
 Storage Temperature Range -65°C to +150°C
 Soldering Temperature (10s) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, outputs terminated with $50\Omega \pm 1\%$ to (V_{CC} - 2V), CLK_SEL = V_{CC} or GND, CLK_EN = V_{CC} , T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUTS (CLK0, CLK1, CLK_SEL, CLK_EN)							
Input High Voltage	V _{IH}	Figure 1	CLK0, CLK1	2		V _{CC}	V
			CLK_EN, CLK_SEL	2		V _{CC}	
Input Low Voltage	V _{IL}	Figure 1	CLK0, CLK1	0		1.3	V
			CLK_EN, CLK_SEL	0		0.8	
Input High Current	I _{IH}	CLK0, CLK1, CLK_SEL = V _{CC}				150	μA
		CLK_EN = V _{CC}			-5	+5	
Input Low Current	I _{IL}	CLK0, CLK1, CLK_SEL = GND			-5	+5	μA
		CLK_EN = GND			-150		
Input Capacitance	C _{IN}	CLK0, CLK1, CLK_SEL, CLK_EN (Note 4)				4	pF
OUTPUTS (Q ₀ , Q ₁)							
Single-Ended Output High Voltage	V _{OH}	Figure 1			V _{CC} - 1.4	V _{CC} - 1.0	V
Single-Ended Output Low Voltage	V _{OL}	Figure 1			V _{CC} - 2.0	V _{CC} - 1.7	V
Differential Output Voltage	V _{OD}	Figure 1, V _{OD} = V _{OH} - V _{OL}			0.6	0.85	V
SUPPLY							
Supply Current (Note 5)	I _{CC}					25	mA

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AC ELECTRICAL CHARACTERISTICS

($V_{CC} = 3.0V$ to $3.6V$, outputs terminated with $50\Omega \pm 1\%$ to $(V_{CC} - 2V)$, $f_{IN} < 266MHz$, input duty cycle = 50%, input transition time = 1.1ns (20% to 80%), $V_{IH} = V_{CC}$, $V_{IL} = GND$, $CLK_SEL = V_{CC}$ or GND , $CLK_EN = V_{CC}$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = 3.3V$, $T_A = +25^{\circ}C$.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency	f_{MAX}	$V_{OH} - V_{OL} \geq 0.6V$	266	800		MHz
		$V_{OH} - V_{OL} \geq 0.3V$	1500			
Propagation Delay	t_{PHL}, t_{PLH}	CLK0 or CLK1 to $Q_{-}, \overline{Q_{-}}$, Figure 1 (Note 6)	100	450	600	ps
Output-to-Output Skew	t_{SKOO}	(Note 7)			30	ps
Part-to-Part Skew	t_{SKPP}	(Note 8)			150	ps
Output Rise Time	t_R	20% to 80%, Figure 1	100	203	300	ps
Output Fall Time	t_F	80% to 20%, Figure 1	100	198	300	ps
Output Duty Cycle	ODC		48	50	52	%
Added Random Jitter	t_{RJ}	$f_{IN} = 266MHz$, clock pattern (Note 9)		1.7	3	ps(RMS)
Added Jitter (Note 9)	t_{AJ}	$V_{CC} = 3.3V$ with 25mV superimposed sinusoidal noise at 100kHz			10	ps(P-P)

Note 1: Measurements are made with the device in thermal equilibrium.

Note 2: Positive current flows into a pin. Negative current flows out of a pin.

Note 3: DC parameters are production tested at $T_A = +25^{\circ}C$ and guaranteed by design over the full operating temperature range.

Note 4: Guaranteed by design and characterization. Limits are set at ± 6 sigma.

Note 5: All pins open except V_{CC} and GND .

Note 6: Measured from the 50% point of the input to the crossing point of the differential output signal.

Note 7: Measured between outputs of the same part at the differential signal crosspoint for a same-edge transition.

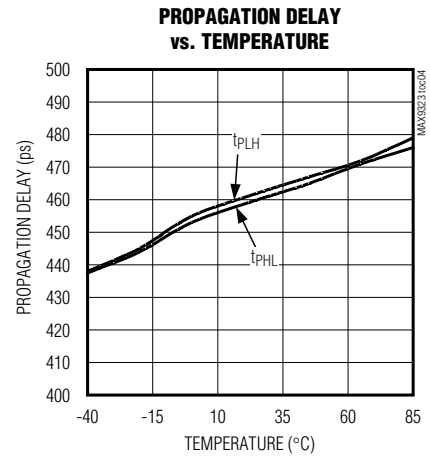
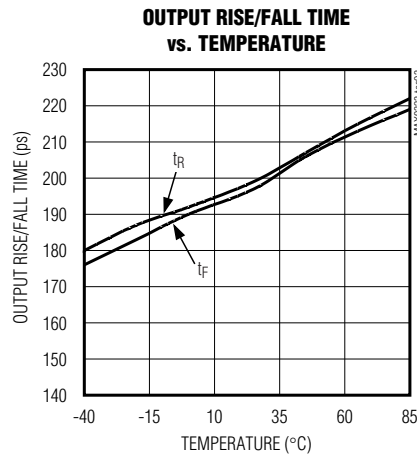
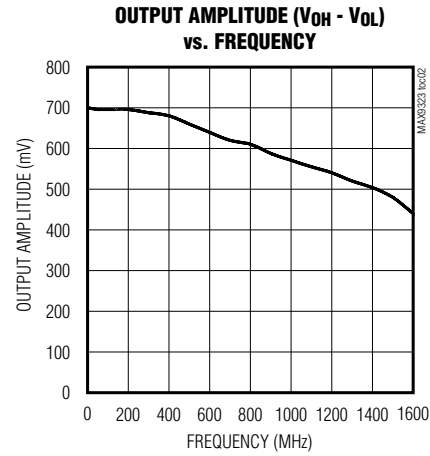
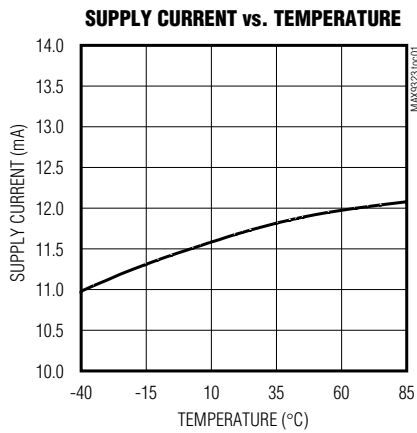
Note 8: Measured between outputs of different parts at the differential signal crosspoint under identical conditions for a same-edge transition.

Note 9: Jitter added to the input signal.

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Typical Operating Characteristics

($V_{CC} = 3.3V$, outputs terminated to ($V_{CC} - 2V$) through 50Ω , $CLK_SEL = V_{CC}$ or GND, $CLK_EN = V_{CC}$, $T_A = +25^\circ C$.)



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Pin Description

PIN		NAME	FUNCTION
TSSOP	QFN		
1	18	GND	Ground. Provide a low-impedance connection to the ground plane.
2	19	CLK_EN	Synchronous Output Enable. Connect CLK_EN to V _{CC} or leave floating to enable the differential outputs. Connect CLK_EN to GND to disable the differential outputs. When disabled, Q ₋ asserts low and $\overline{Q_-}$ asserts high. An internal 51k Ω pullup resistor to V _{CC} allows CLK_EN to be left floating.
3	20	CLK_SEL	Clock Select Input. Connect CLK_SEL to V _{CC} to select the CLK1 input. Connect CLK_SEL to GND or leave floating to select the CLK0 input. Only the selected CLK ₋ signal is reproduced at each output. An internal 51k Ω pulldown resistor to GND allows CLK_SEL to be left floating.
4	1	CLK0	LVCMOS Clock Input. When CLK_SEL = GND, each set of outputs differentially reproduces CLK0. An internal 51k Ω pulldown resistor to GND forces the outputs (Q ₋ , $\overline{Q_-}$) to differential low when CLK0 is left open or at GND, CLK_SEL = GND, and the outputs are enabled.
5, 7, 8, 9	2, 4, 5, 6	N.C.	No Connect. Not internally connected.
6	3	CLK1	LVCMOS Clock Input. When CLK_SEL = V _{CC} , each set of outputs differentially reproduces CLK1. An internal 51k Ω pulldown resistor to GND forces the outputs (Q ₋ , $\overline{Q_-}$) to differential low when CLK1 is left open or at GND, CLK_SEL = V _{CC} , and the outputs are enabled.
10, 13, 18	7, 10, 15	V _{CC}	Positive Supply Voltage. Bypass V _{CC} to GND with three 0.01 μ F and one 0.1 μ F ceramic capacitors. Place the 0.01 μ F capacitors as close to each V _{CC} input as possible (one per V _{CC} input). Connect all V _{CC} inputs together, and bypass to GND with a 0.1 μ F ceramic capacitor.
11	8	$\overline{Q3}$	Inverting Differential LVPECL Output. Terminate Q3 to (V _{CC} - 2V) with a 50 Ω $\pm$ 1% resistor.
12	9	Q3	Noninverting Differential LVPECL Output. Terminate Q3 to (V _{CC} - 2V) with a 50 Ω $\pm$ 1% resistor.
14	11	$\overline{Q2}$	Inverting Differential LVPECL Output. Terminate $\overline{Q2}$ to (V _{CC} - 2V) with a 50 Ω $\pm$ 1% resistor.
15	12	Q2	Noninverting Differential LVPECL Output. Terminate Q2 to (V _{CC} - 2V) with a 50 Ω $\pm$ 1% resistor.
16	13	$\overline{Q1}$	Inverting Differential LVPECL Output. Terminate $\overline{Q1}$ to (V _{CC} - 2V) with a 50 Ω $\pm$ 1% resistor.
17	14	Q1	Noninverting Differential LVPECL Output. Terminate Q1 to (V _{CC} - 2V) with a 50 Ω $\pm$ 1% resistor.
19	16	$\overline{Q0}$	Inverting Differential LVPECL Output. Terminate $\overline{Q0}$ to (V _{CC} - 2V) with a 50 Ω $\pm$ 1% resistor.
20	17	Q0	Noninverting Differential LVPECL Output. Terminate Q0 to (V _{CC} - 2V) with a 50 Ω $\pm$ 1% resistor.

Detailed Description

The MAX9323 low-skew, low-jitter, clock and data driver distributes one of two single-ended LVCMOS input signals to four differential LVPECL outputs. An input multiplexer allows selection of one of the two input signals. The output drivers operate at frequencies up to 1.5GHz. The MAX9323 operates from 3.0V to 3.6V, making it ideal for 3.3V systems.

Data Inputs

Single-Ended LVCMOS Inputs

The MAX9323 accepts two single-ended LVCMOS inputs (CLK0 and CLK1, Figure 1). An internal reference (V_{CC}/2) provides the input threshold voltage for CLK0 and CLK1. CLK_SEL selects the CLK0 input or CLK1 input to be converted to four differential LVPECL signals (see Table 1). Connect CLK_SEL to GND to

select CLK0. Connect CLK_SEL to V_{CC} to select CLK1. CLK0 and CLK1 are pulled to GND through internal 51k Ω resistors, when not connected.

CLK_EN Input

CLK_EN enables/disables the differential outputs of the MAX9323. Connect CLK_EN to V_{CC} to enable the differential outputs. The (Q₋, $\overline{Q_-}$) outputs are driven to a differential low condition when CLK_EN = GND. Each differential output pair disables following successive rising and falling edges on CLK₋, after CLK_EN connects to GND. Both a rising and falling edge on CLK₋ are required to complete the enable/disable function (Figure 2).

CLK_SEL Input

CLK_SEL selects which single-ended LVCMOS input signal is output differentially as four LVPECL signals. Connect CLK_SEL to GND to select the CLK0 input.

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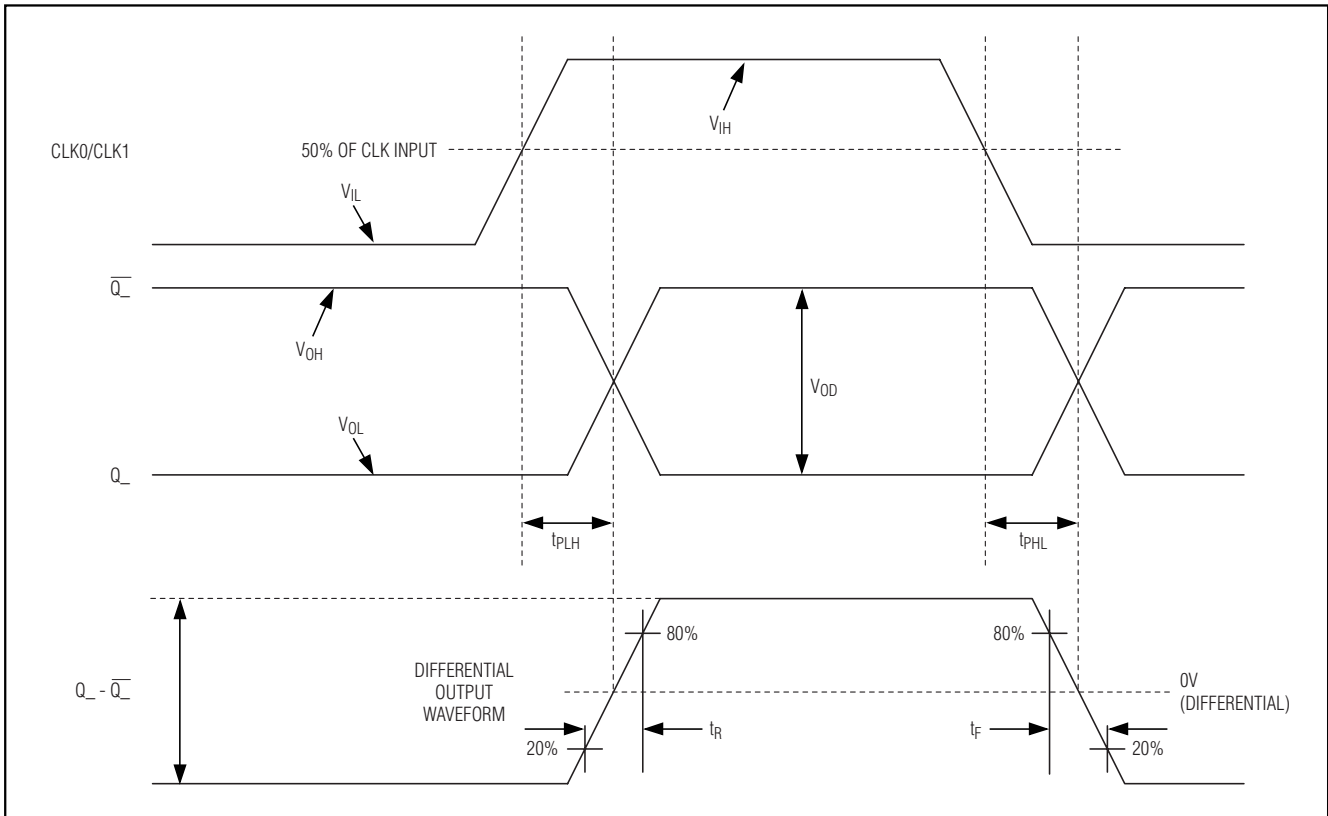


Figure 1. MAX9323 Clock Input-to-Output Delay and Rise/Fall Time

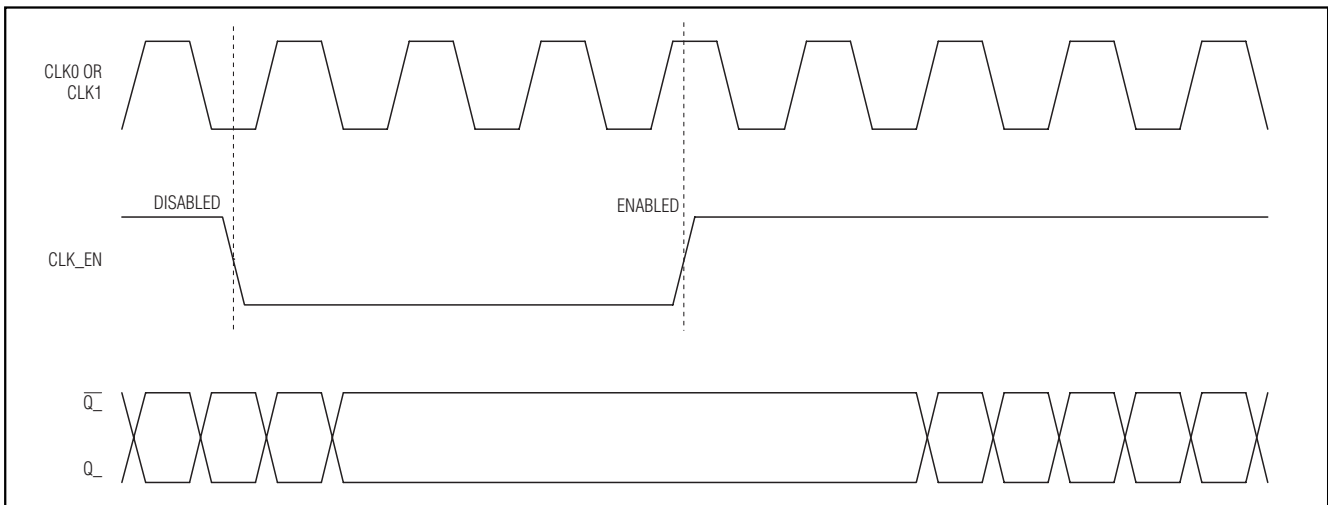


Figure 2. MAX9323 CLK_EN Timing Diagram

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Table 1. Control Input Table

INPUTS			OUTPUTS	
CLK_EN	CLK_SEL	SELECTED SOURCE	Q0–Q3	$\overline{Q0}–\overline{Q3}$
0	0	CLK0	Disabled, pulled to logic low	Disabled, pulled to logic high
0	1	CLK1	Disabled, pulled to logic low	Disabled, pulled to logic high
1	0	CLK0	Enabled	Enabled
1	1	CLK1	Enabled	Enabled

Connect CLK_SEL to V_{CC} to select the CLK1 input. An internal 51k Ω pulldown resistor to GND allows CLK_SEL to be left floating.

Applications Information

Output Termination

Terminate both outputs of each differential pair through 50 Ω to (V_{CC} - 2V) or use an equivalent Thevenin termination. Use identical termination on each output for the lowest output-to-output skew. Terminate both outputs when deriving a single-ended signal from a differential output. For example, using Q0 as a single-ended output requires termination for both Q0 and $\overline{Q0}$.

Ensure that the output currents do not violate the current limits as specified in the *Absolute Maximum Ratings* table. Observe the device's total thermal limits under all operating conditions.

Power-Supply Bypassing

Bypass V_{CC} to GND using three 0.01 μ F ceramic capacitors and one 0.1 μ F ceramic capacitor. Place the 0.01 μ F capacitors (one per V_{CC} input) as close to V_{CC} as possible (see the *Typical Operating Circuit*). Use multiple bypass vias to minimize parasitic inductance.

Circuit Board Traces

Input and output trace characteristics affect the performance of the MAX9323. Connect each input and output to a 50 Ω characteristic impedance trace to minimize reflections. Avoid discontinuities in differential imped-

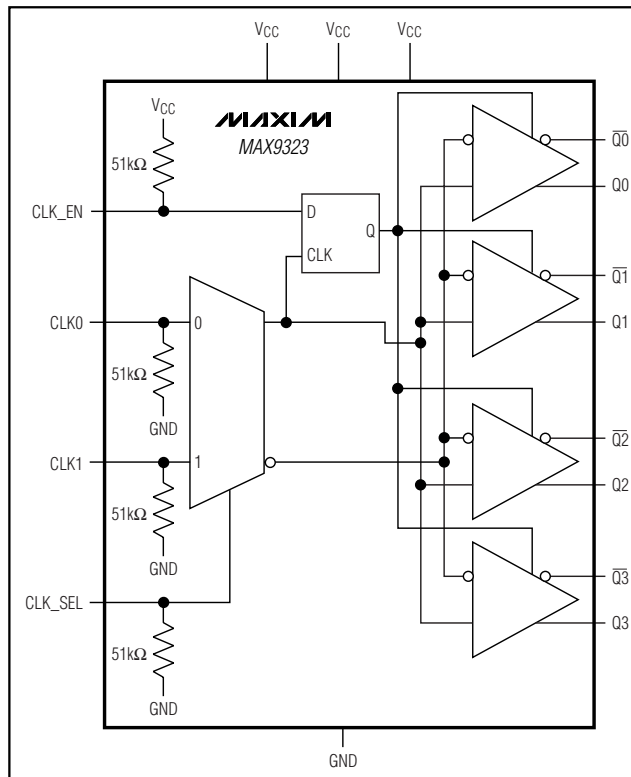
ance and maximize common-mode noise immunity by maintaining the distance between differential traces and avoiding sharp corners. Minimize the number of vias to prevent impedance discontinuities. Minimize skew by matching the electrical length of the traces.

Chip Information

TRANSISTOR COUNT: 4430

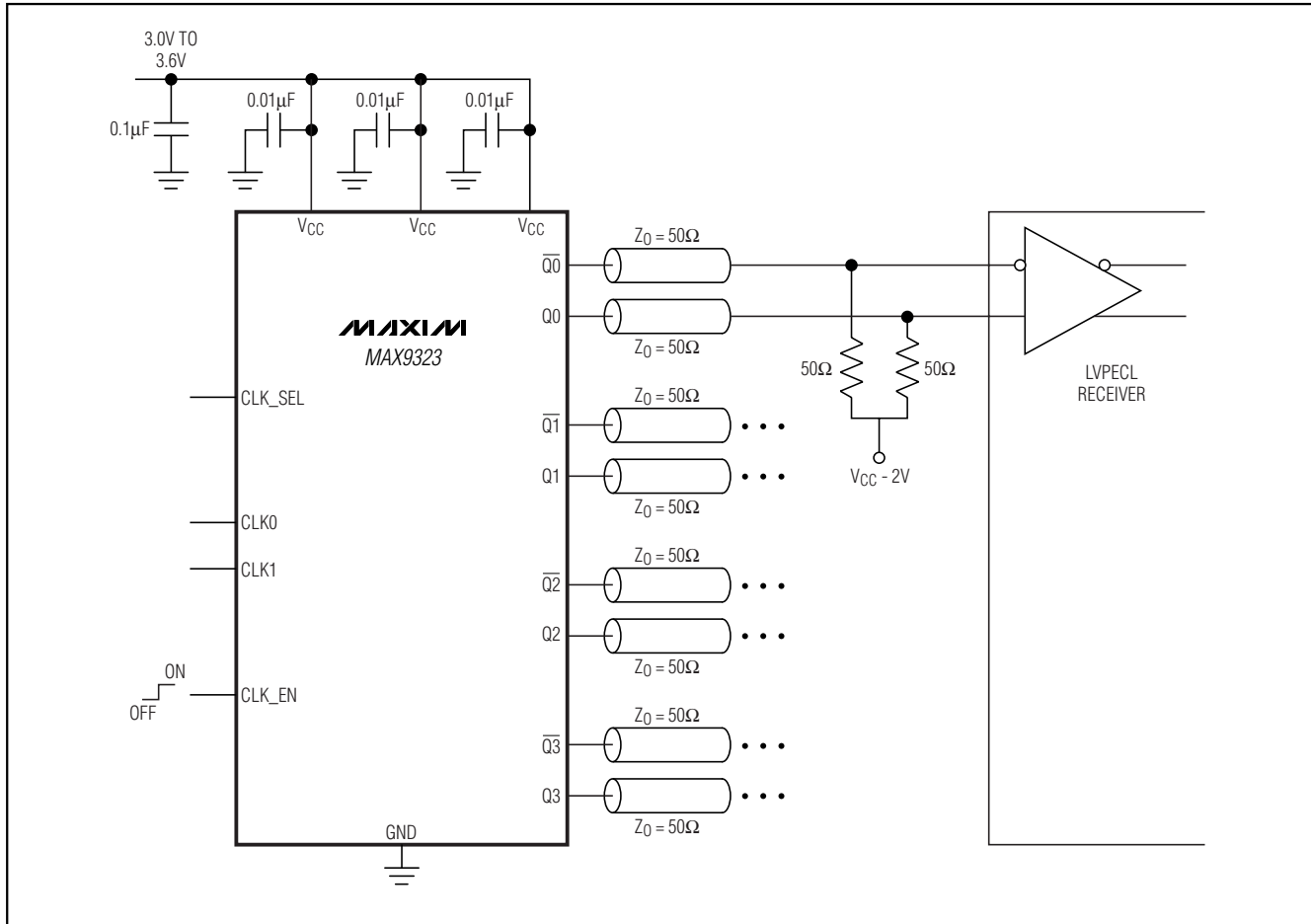
PROCESS: BiCMOS

Functional Diagram



One-to-Four LVCMOS-to-LVPECL Output Clock and Data Driver

Typical Operating Circuit

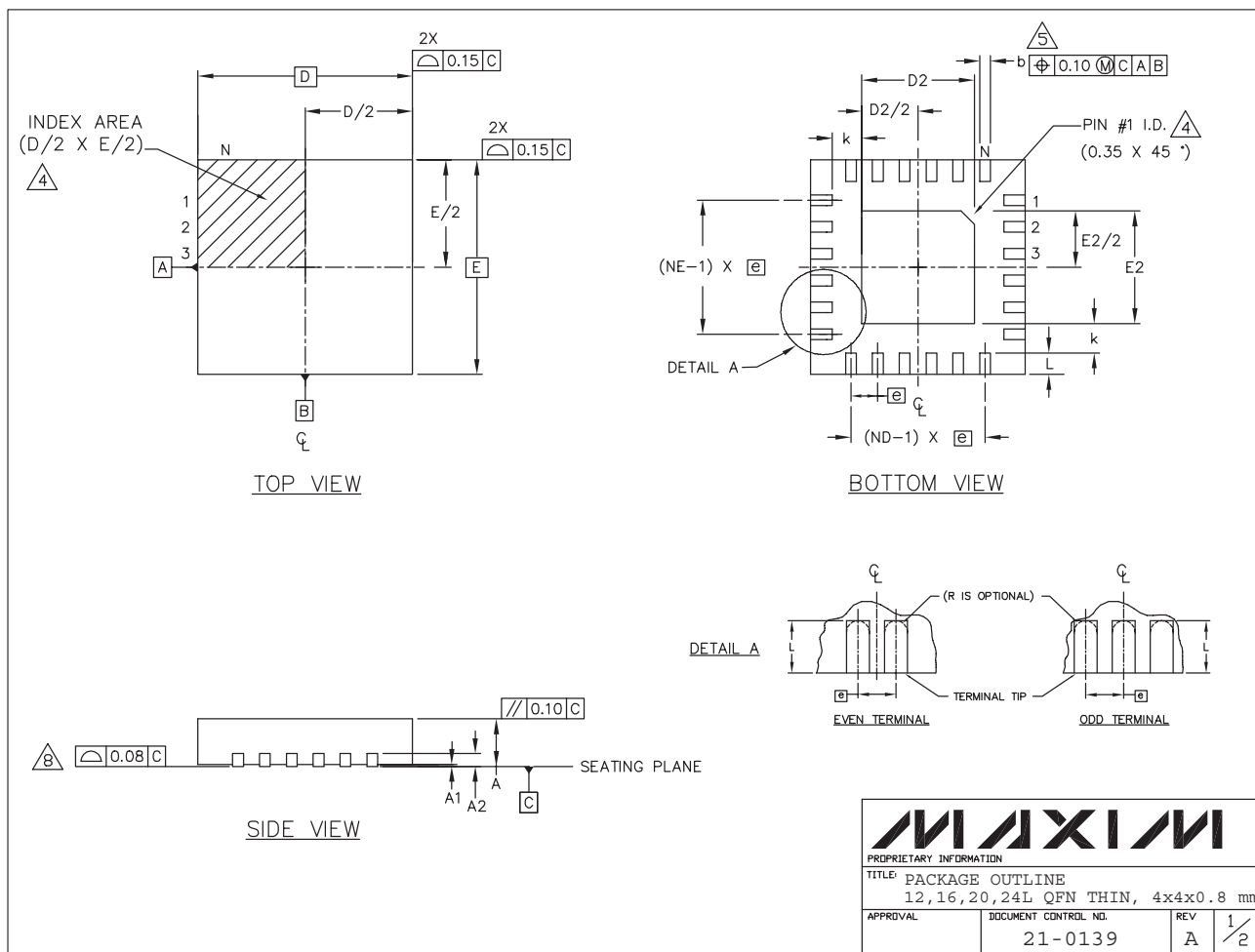


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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

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Package Information (continued)

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COMMON DIMENSIONS												
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
JeDEC	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63

NOTES:

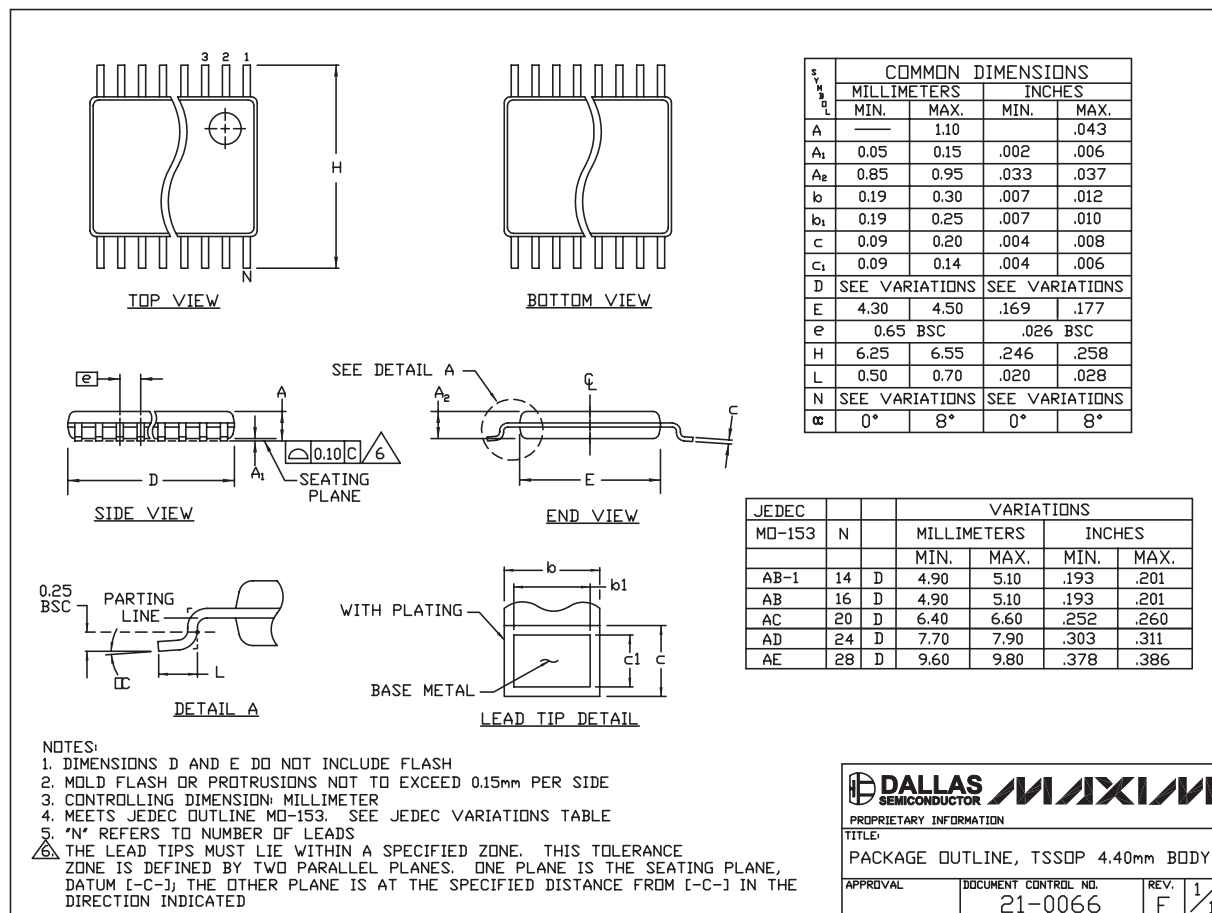
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.

MAXIM			
PROPRIETARY INFORMATION			
TITLE: PACKAGE OUTLINE			
12, 16, 20, 24L QFN THIN, 4x4x0.8 mm			
APPROVAL	DOCUMENT CONTROL NO.	REV	2/2
	21-0139	A	

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Package Information (continued)

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TSSOP4.40mm, EPS

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