# 1:2 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$ to $V_{EE}$ .....+4.1V
D or $\overline{D}$ ..... $V_{EE}$ - 0.3V to $V_{CC}$ + 0.3V
D to $\overline{D}$ .....±3.0V
Continuous Output Current .....50mA
Surge Output Current.....100mA
Junction-to-Ambient Thermal Resistance in Still Air
8-Pin SOT23.....+112°C/W
8-Pin µMAX .....+221°C/W
8-Pin SO.....+170°C/W
Junction-to-Ambient Thermal Resistance with 500 LFPM Airflow
8-Pin SOT23.....+78°C/W
8-Pin µMAX .....+155°C/W
8-Pin SO.....+99°C/W
Junction-to-Case Thermal Resistance
8-Pin SOT23.....+80°C/W
8-Pin µMAX .....+39°C/W
8-Pin SO.....+40°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection
Human Body Model (D, $\overline{D}$, Q_, $\overline{Q\_}$) .....>2kV
Soldering Temperature (10s).....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## DC ELECTRICAL CHARACTERISTICS

($V_{CC}$ - $V_{EE}$ = +2.25V to +3.8V, outputs loaded with 50Ω ±1% to $V_{CC}$ - 2V. Typical values are at $V_{CC}$ - $V_{EE}$ = +3.3V, $V_{IHD}$ = $V_{CC}$ - 1.0V, $V_{ILD}$ = $V_{CC}$ - 1.5V, unless otherwise noted.) (Notes 1, 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | -40°C | | | +25°C | | | +85°C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **DIFFERENTIAL INPUT (D, $\overline{D}$)** | | | | | | | | | | | | |
| High Voltage of Differential Input | $V_{IHD}$ | | $V_{EE}$ + 1.2 | | $V_{CC}$ | $V_{EE}$ + 1.2 | | $V_{CC}$ | $V_{EE}$ + 1.2 | | $V_{CC}$ | V |
| Low Voltage of Differential Input | $V_{ILD}$ | | $V_{EE}$ | | $V_{CC}$ - 0.1 | $V_{EE}$ | | $V_{CC}$ - 0.1 | $V_{EE}$ | | $V_{CC}$ - 0.1 | V |
| Differential Input Voltage | $V_{IHD}$ - $V_{ILD}$ | For $V_{CC}$ - $V_{EE}$ < +3.0V | 0.1 | | $V_{CC}$ - $V_{EE}$ | 0.1 | | $V_{CC}$ - $V_{EE}$ | 0.1 | | $V_{CC}$ - $V_{EE}$ | V |
| | | For $V_{CC}$ - $V_{EE}$ ≥ +3.0V | 0.1 | | 3.0 | 0.1 | | 3.0 | 0.1 | | 3.0 | |
| Input High Current | $I_{IH}$ | | | | 150 | | | 150 | | | 150 | µA |
| D Input Low Current | $I_{ILD}$ | | -10 | | 100 | -10 | | 100 | -10 | | 100 | µA |
| $\overline{D}$ Input Low Current | $I_{IL\overline{D}}$ | | -150 | | +150 | -150 | | +150 | -150 | | +150 | µA |
| **DIFFERENTIAL OUTPUTS (Q_, $\overline{Q\_}$)** | | | | | | | | | | | | |
| Single-Ended Output High Voltage | $V_{OH}$ | Figure 1 | $V_{CC}$ - 1.135 | | $V_{CC}$ - 0.885 | $V_{CC}$ - 1.07 | | $V_{CC}$ - 0.82 | $V_{CC}$ - 1.01 | | $V_{CC}$ - 0.76 | V |

## DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ - $V_{EE}$ = +2.25V to +3.8V, outputs loaded with 50Ω ±1% to $V_{CC}$ - 2V. Typical values are at $V_{CC}$ - $V_{EE}$ = +3.3V, $V_{IHD}$ = $V_{CC}$ - 1.0V, $V_{ILD}$ = $V_{CC}$ - 1.5V, unless otherwise noted.) (Notes 1, 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | -40°C | | | +25°C | | | +85°C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| Single-Ended Output Low Voltage | $V_{OL}$ | Figure 1 | $V_{CC}$ - 1.935 | | $V_{CC}$ - 1.685 | $V_{CC}$ - 1.87 | | $V_{CC}$ - 1.62 | $V_{CC}$ - 1.81 | | $V_{CC}$ - 1.56 | V |
| Differential Output Voltage | $V_{OH}$ - $V_{OL}$ | Figure 1 | 550 | | | 550 | | | 550 | | | mV |
| **POWER SUPPLY** | | | | | | | | | | | | |
| Supply Current | $I_{EE}$ | (Note 4) | | 20 | 28 | | 22 | 28 | | 23 | 30 | mA |

## AC ELECTRICAL CHARACTERISTICS

($V_{CC}$ - $V_{EE}$ = +2.25V to +3.8V, outputs loaded with 50Ω ±1% to $V_{CC}$ - 2V, input frequency = 1.5GHz, input transition time = 125ps (20% to 80%), $V_{IHD}$ = $V_{EE}$ + 1.2V to $V_{CC}$, $V_{ILD}$ = $V_{EE}$ to $V_{CC}$ - 0.15V, $V_{IHD}$ - $V_{ILD}$ = 0.15V to the smaller of 3V or $V_{CC}$ - $V_{EE}$. Typical values are at $V_{CC}$ - $V_{EE}$ = +3.3V, $V_{IHD}$ = $V_{CC}$ - 1V, $V_{ILD}$ = $V_{CC}$ - 1.5V, unless otherwise noted.) (Note 5)

| PARAMETER | SYMBOL | CONDITIONS | -40°C | | | +25°C | | | +85°C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| Differential Input-to-Output Delay | $t_{PLHD}$, $t_{PHLD}$ | Figure 1 | 145 | 203 | 265 | 155 | 208 | 265 | 160 | 220 | 270 | ps |
| Output-to-Output Skew | $t_{SKOO}$ | (Note 6) | | 6 | 30 | | 6 | 30 | | 6 | 30 | ps |
| Part-to-Part Skew | $t_{SKPP}$ | (Note 7) | | 20 | 120 | | 20 | 110 | | 20 | 110 | ps |
| Added Random Jitter (Note 8) | $t_{RJ}$ | $f_{IN}$ = 1.5GHz, clock pattern | | 1.7 | 2.8 | | 1.7 | 2.8 | | 1.7 | 2.8 | ps (RMS) |
| | | $f_{IN}$ = 3.0GHz, clock pattern | | 0.6 | 1.5 | | 0.6 | 1.5 | | 0.6 | 1.5 | |
| Added Deterministic Jitter | $t_{DJ}$ | 3.0Gbps $2^{23}$-1 PRBS pattern (Note 8) | | 57 | 80 | | 57 | 80 | | 57 | 80 | ps (p-p) |

# 1:2 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

## AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ - $V_{EE}$ = +2.25V to +3.8V, outputs loaded with 50Ω ±1% to $V_{CC}$ - 2V, input frequency = 1.5GHz, input transition time = 125ps (20% to 80%), $V_{IHD}$ = $V_{EE}$ + 1.2V to $V_{CC}$, $V_{ILD}$ = $V_{EE}$ to $V_{CC}$ - 0.15V, $V_{IHD}$ - $V_{ILD}$ = 0.15V to the smaller of 3V or $V_{CC}$ - $V_{EE}$. Typical values are at $V_{CC}$ - $V_{EE}$ = +3.3V, $V_{IHD}$ = $V_{CC}$ - 1V, $V_{ILD}$ = $V_{CC}$ - 1.5V, unless otherwise noted.) (Note 5)

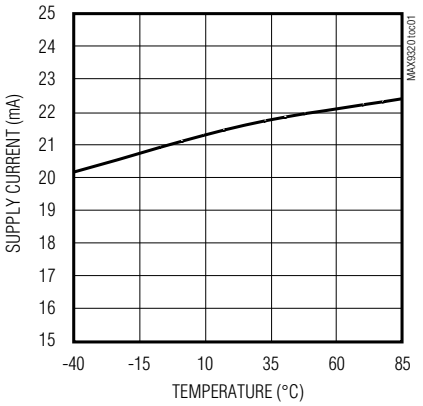
| PARAMETER | SYMBOL | CONDITIONS | -40°C | | | +25°C | | | +85°C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| Switching Frequency | $f_{MAX}$ | $V_{OH}$ - $V_{OL}$ ≥ 300mV, clock pattern, Figure 1 | 3.0 | | | 3.0 | | | 3.0 | | | GHz |
| | | $V_{OH}$ - $V_{OL}$ ≥ 550mV, clock pattern, Figure 1 | 2.0 | | | 2.0 | | | 2.0 | | | |
| Output Rise/Fall Time (20% to 80%) | $t_R$, $t_F$ | Figure 1 | 50 | 88 | 120 | 50 | 89 | 120 | 50 | 90 | 120 | ps |

**Note 1:** Measurements are made with the device in thermal equilibrium.
**Note 2:** Current into a pin is defined as positive. Current out of a pin is defined as negative.
**Note 3:** DC parameters production tested at $T_A$ = +25°C. Guaranteed by design and characterization over the full operating temperature range.
**Note 4:** All pins open except $V_{CC}$ and $V_{EE}$.
**Note 5:** Guaranteed by design and characterization. Limits are set at ±6 sigma.
**Note 6:** Measured between outputs of the same part at the signal crossing points for a same-edge transition.
**Note 7:** Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.
**Note 8:** Device jitter added to the input signal.

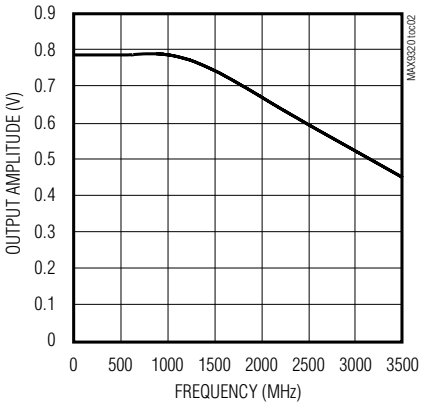
## Typical Operating Characteristics

($V_{CC}$ = +3.3V, $V_{EE}$ = 0, input transition time = 125ps (20% to 80%), $V_{IHD}$ = $V_{CC}$ - 1V, $V_{ILD}$ = $V_{CC}$ - 1.5V, $f_{IN}$ = 1.5GHz, outputs loaded with 50Ω to $V_{CC}$ - 2V, $T_A$ = +25°C, unless otherwise noted.)

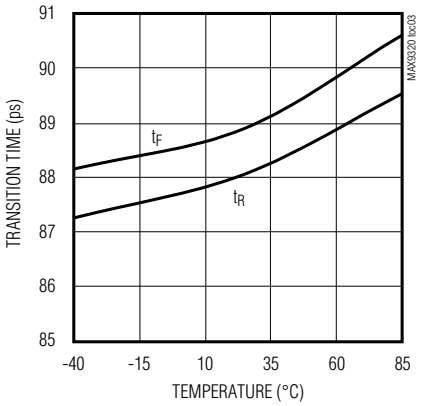
**SUPPLY CURRENT, $I_{EE}$ vs. TEMPERATURE**



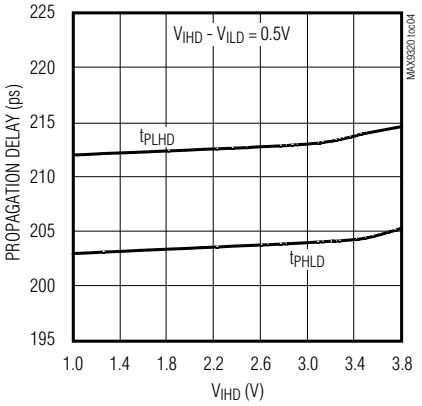

**OUTPUT AMPLITUDE, $V_{OH}$ - $V_{OL}$ vs. FREQUENCY**



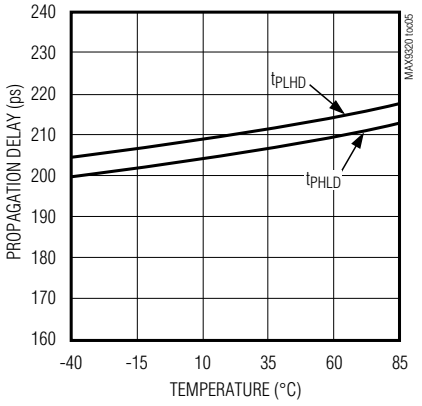

**TRANSITION TIME vs. TEMPERATURE**




**PROPAGATION DELAY vs. HIGH VOLTAGE OF DIFFERENTIAL INPUT, $V_{IHD}$**




**PROPAGATION DELAY vs. TEMPERATURE**



# 1:2 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

## Pin Description (MAX9320)

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| µMAX/SO | SOT23 | | |
| 1 | 8 | Q0 | Noninverting Q0 Output. Typically terminate with 50Ω resistor to $V_{CC}$ - 2V. |
| 2 | 7 | $\overline{Q0}$ | Inverting Q0 Output. Typically terminate with 50Ω resistor to $V_{CC}$ - 2V. |
| 3 | 6 | Q1 | Noninverting Q1 Output. Typically terminate with 50Ω resistor to $V_{CC}$ - 2V. |
| 4 | 5 | $\overline{Q1}$ | Inverting Q1 Output. Typically terminate with 50Ω resistor to $V_{CC}$ - 2V. |
| 5 | 2 | $V_{EE}$ | Negative Supply Voltage |
| 6 | 4 | $\overline{D}$ | Inverting Differential Input. 60kΩ pullup to $V_{CC}$ and 100kΩ pulldown to $V_{EE}$. |
| 7 | 3 | D | Noninverting Differential Input. 100kΩ pulldown to $V_{EE}$. |
| 8 | 1 | $V_{CC}$ | Positive Supply Voltage. Bypass from $V_{CC}$ to $V_{EE}$ with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device. |

## Pin Description (MAX9320A)

| PIN | NAME | FUNCTION |
|---|---|---|
| SOT23 | | |
| 1 | $V_{CC}$ | Positive Supply Voltage. Bypass from $V_{CC}$ to $V_{EE}$ with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device. |
| 2 | $V_{EE}$ | Negative Supply Voltage |
| 3 | $\overline{D}$ | Inverting Differential Input. 60kΩ pullup to $V_{CC}$ and 100kΩ pulldown to $V_{EE}$. |
| 4 | D | Noninverting Differential Input. 100kΩ pulldown to $V_{EE}$. |
| 5 | $\overline{Q1}$ | Inverting Q1 Output. Typically terminate with 50Ω resistor to $V_{CC}$ - 2V. |
| 6 | Q1 | Noninverting Q1 Output. Typically terminate with 50Ω resistor to $V_{CC}$ - 2V. |
| 7 | $\overline{Q0}$ | Inverting Q0 Output. Typically terminate with 50Ω resistor to $V_{CC}$ - 2V. |
| 8 | Q0 | Noninverting Q0 Output. Typically terminate with 50Ω resistor to $V_{CC}$ - 2V. |

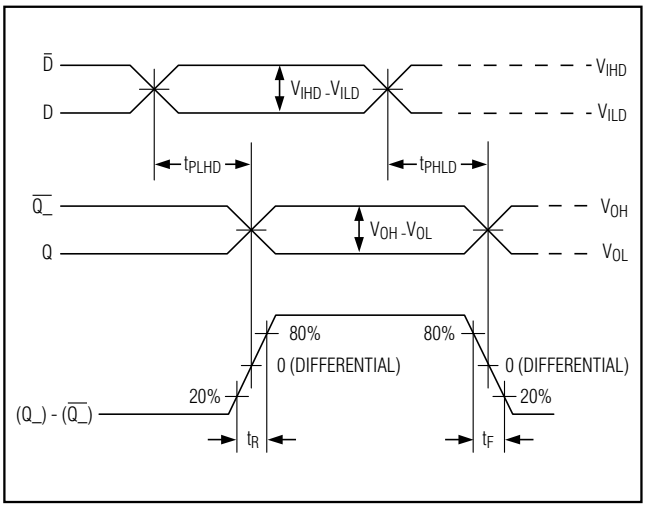



*Figure 1. Differential Transition Time and Propagation Delay Timing Diagram*

## Detailed Description

The MAX9320/MAX9320A low-skew, 1-to-2 differential drivers are designed for clock and data distribution. For interfacing to differential HSTL and LVPECL signals, these devices operate over a +2.25V to +3.8V supply range, allowing high-performance clock and data distribution in systems with a nominal +2.5V or +3.3V supply. For differential LVECL operation, these devices operate from a -2.25V to -3.8V supply.

### Inputs

The maximum magnitude of the differential input from D to $\overline{D}$ is $V_{CC}$ - $V_{EE}$ or 3.0V, whichever is less. This limit also applies to the difference between any reference voltage input and a single-ended input.

The differential inputs have bias resistors that drive the outputs to a differential low when the inputs are open. The inverting input, $\overline{D}$, is biased with a 60kΩ pullup to $V_{CC}$ and a 100kΩ pulldown to $V_{EE}$. The noninverting input, D, is biased with a 100kΩ pulldown to $V_{EE}$.

Specifications for the high and low voltages of the differential input ($V_{IHD}$ and $V_{ILD}$) and the differential input voltage ($V_{IHD}$ - $V_{ILD}$) apply simultaneously ($V_{ILD}$ cannot be higher than $V_{IHD}$).

### Outputs

Output levels are referenced to $V_{CC}$ and are considered LVPECL or LVECL, depending on the level of the $V_{CC}$ supply. With $V_{CC}$ connected to a positive supply and $V_{EE}$ connected to GND, the outputs are LVPECL. The outputs are LVECL when $V_{CC}$ is connected to GND and $V_{EE}$ is connected to a negative supply.

A single-ended input of ±100mV around a reference voltage or a differential input of at least ±100mV switches the outputs to the $V_{OH}$ and $V_{OL}$ levels specified in the *DC Electrical Characteristics* table.

## Applications Information

### Supply Bypassing

Bypass $V_{CC}$ to $V_{EE}$ with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors in parallel as close to the device as possible, with the 0.01µF value capacitor closest to the device. Use multiple parallel vias for low inductance.

### Traces

Input and output trace characteristics affect the performance of the MAX9320/MAX9320A. Connect each signal of a differential input or output to a 50Ω characteristic impedance trace. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through connectors and across cables. Reduce skew within a differential pair by matching the electrical length of the traces.

The exposed-pad (EP) SO package can be soldered to the PC board for enhanced thermal performance. If the EP is not soldered to the PC board, the thermal resistance is the same as the regular SO package. The EP is connected to the chip $V_{EE}$ supply. Be sure that the pad does not touch signal lines or other supplies.

Contact the Maxim Packaging department for guidelines on the use of EP packages.

### Output Termination

Terminate outputs through 50Ω to $V_{CC}$ - 2V or use an equivalent Thevenin termination. Terminate both outputs and use the same termination on each for the lowest output-to-output skew. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if Q0 is used as a single-ended output, terminate both Q0 and $\overline{Q0}$.

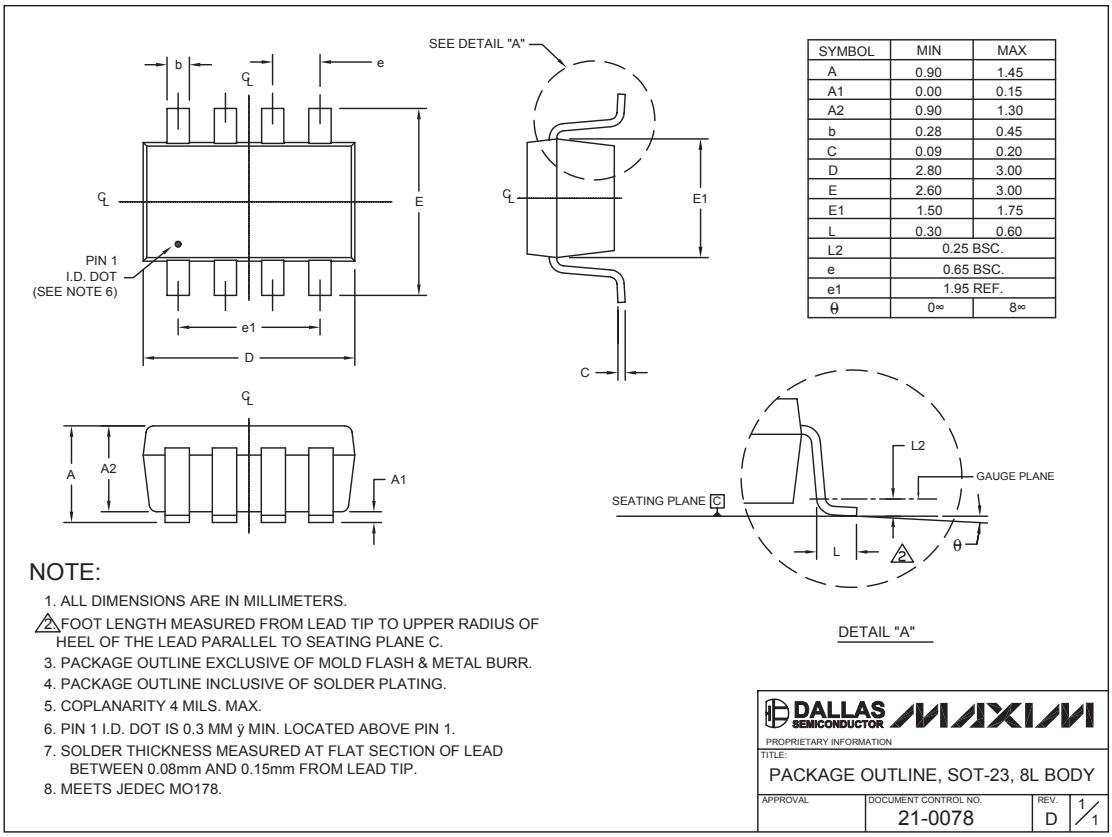
## Chip Information

TRANSISTOR COUNT: 182

# 1:2 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)




| SYMBOL | MIN | MAX |
|---|---|---|
| A | 0.90 | 1.45 |
| A1 | 0.00 | 0.15 |
| A2 | 0.90 | 1.30 |
| b | 0.28 | 0.45 |
| C | 0.09 | 0.20 |
| D | 2.80 | 3.00 |
| E | 2.60 | 3.00 |
| E1 | 1.50 | 1.75 |
| L | 0.30 | 0.60 |
| L2 | 0.25 BSC. | |
| e | 0.65 BSC. | |
| e1 | 1.95 REF. | |
| θ | 0∞ | 8∞ |

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. PIN 1 I.D. DOT IS 0.3 MM ÿ MIN. LOCATED ABOVE PIN 1.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

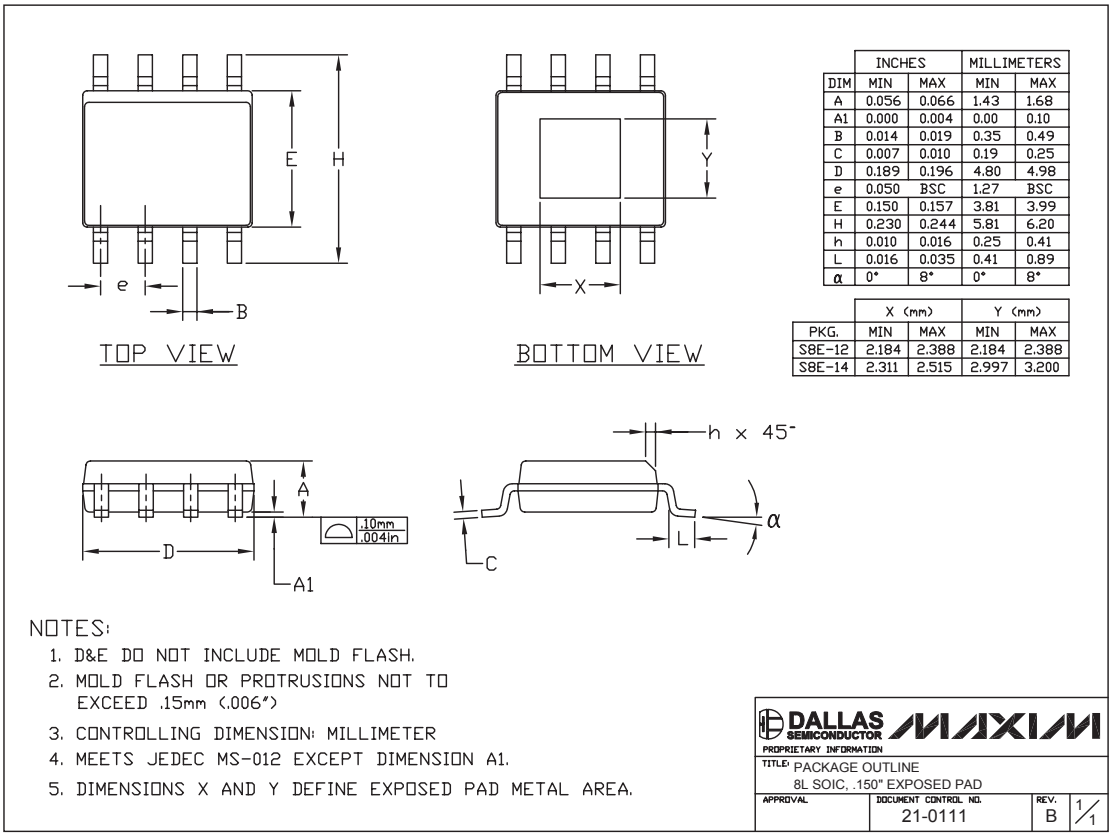
TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0078 | D | 1/1 |

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

8L, SOIC EXP. PAD.EPS




| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.056 | 0.066 | 1.43 | 1.68 |
| A1 | 0.000 | 0.004 | 0.00 | 0.10 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| D | 0.189 | 0.196 | 4.80 | 4.98 |
| e | 0.050 | BSC | 1.27 | BSC |
| E | 0.150 | 0.157 | 3.81 | 3.99 |
| H | 0.230 | 0.244 | 5.81 | 6.20 |
| h | 0.010 | 0.016 | 0.25 | 0.41 |
| L | 0.016 | 0.035 | 0.41 | 0.89 |
| α | 0° | 8° | 0° | 8° |

| | X (mm) | | Y (mm) | |
|---|---|---|---|---|
| PKG. | MIN | MAX | MIN | MAX |
| S8E-12 | 2.184 | 2.388 | 2.184 | 2.388 |
| S8E-14 | 2.311 | 2.515 | 2.997 | 3.200 |

NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-012 EXCEPT DIMENSION A1.
5. DIMENSIONS X AND Y DEFINE EXPOSED PAD METAL AREA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
8L SOIC, .150" EXPOSED PAD

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0111 | B | 1/1 |

# 1:2 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

## Package Information (continued)

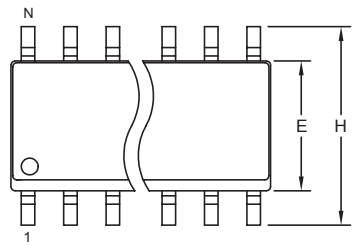
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICN .EPS

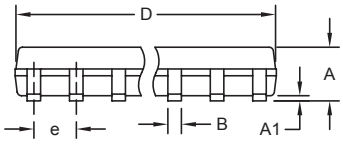
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| e | 0.050 BSC | | 1.27 BSC | |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

VARIATIONS:

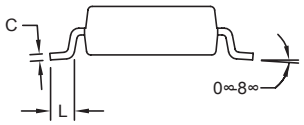
| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX | N | MS012 |
| D | 0.189 | 0.197 | 4.80 | 5.00 | 8 | AA |
| D | 0.337 | 0.344 | 8.55 | 8.75 | 14 | AB |
| D | 0.386 | 0.394 | 9.80 | 10.00 | 16 | AC |




TOP VIEW




FRONT VIEW




SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0041 | B | 1/1 |