

Micropower, Ultra-Small, Single/Dual/Quad, Single-Supply Comparators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to V_{SS}) -0.3V to +6V
 Voltage Inputs ($IN+$, $IN-$ to V_{SS}) -0.3V to ($V_{DD} + 0.3V$)
 Differential Input Voltage ($IN+$ to $IN-$) 6.6V
 Current into Input Pins $\pm 20mA$
 Output Short-Circuit Duration 2s to Either V_{DD} or V_{SS}
 Current into Any Pin 20mA
 Continuous Power Dissipation ($T_A = +70^\circ C$)
 5-Pin SC70 (derate 3.1mW/ $^\circ C$ above $+70^\circ C$) 247mW
 5-Pin SOT23 (derate 7.1mW/ $^\circ C$ above $+70^\circ C$) 571mW
 8-Pin SOT23 (derate 9.1mW/ $^\circ C$ above $+70^\circ C$) 727mW

8-Pin μMAX (derate 4.5mW/ $^\circ C$ above $+70^\circ C$) 362mW
 8-Pin SO (derate 5.88mW/ $^\circ C$ above $+70^\circ C$) 471mW
 14-Pin TSSOP (derate 9.1mW/ $^\circ C$ above $+70^\circ C$) 727mW
 14-Pin SO (derate 8.3mW/ $^\circ C$ above $+70^\circ C$) 667mW
 Operating Temperature Range
 Automotive Application $-40^\circ C$ to $+125^\circ C$
 Junction Temperature $+150^\circ C$
 Storage Temperature Range $-65^\circ C$ to $+150^\circ C$
 Lead Temperature (soldering, 10s) $+300^\circ C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{DD} = 5V$, $V_{SS} = 0$, $V_{CM} = 0$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{DD}	Guaranteed by PSRR test	2.5		5.5	V
Supply Current Per Comparator	I_{DD}			2.8	5	μA
Input Offset Voltage	V_{OS}	(Note 2)		± 1	± 8	mV
Input Offset Voltage Temperature Coefficient	TCV_{OS}			± 1		$\mu V/^\circ C$
Hysteresis		(Note 3)		4		mV
Input Bias Current	I_{BIAS}			3	80	nA
Input Offset Current	I_{OS}			± 2	± 60	nA
Common-Mode Voltage Range	V_{CM}	Guaranteed by CMRR test	V_{SS}		$V_{DD} - 1.1$	V
Common-Mode Rejection Ratio	CMRR	$V_{SS} \leq V_{CM} \leq (V_{DD} - 1.1V)$, $V_{DD} = 5.5V$	70	100		dB
Power-Supply Rejection Ratio	PSRR	$V_{DD} = 2.5V$ to $5.5V$	60	80		dB
Output-Voltage Swing	V_{OL} , V_{OH}	$V_{OH} = V_{DD} - V_{OUT}$, $(V_{IN+} - V_{IN-}) \geq 20mV$	$I_{SOURCE} = 10\mu A$		2	mV
			$I_{SOURCE} = 4mA$		160	
		$V_{OL} = V_{OUT} - V_{SS}$, $(V_{IN-} - V_{IN+}) \geq 20mV$	$I_{SINK} = 10\mu A$		2	
			$I_{SINK} = 4mA$		180	
Output Short-Circuit Current	I_{SC}			50		mA
Propagation Delay	t_{pd+} , t_{pd-}	$R_L = 10k\Omega$, $C_L = 15pF$ (Note 4)	$V_{OD} = 10mV$		8	μs
			$V_{OD} = 100mV$		3	
Rise and Fall Time	t_R , t_F	$R_L = 10k\Omega$, $C_L = 15pF$ (Note 5)		20		ns
Power-On Time		$R_L = 10k\Omega$, $C_L = 15pF$		150		ns
Maximum Capacitive Load	C_L	No sustained oscillations		150		pF

Note 1: All devices are production tested at $25^\circ C$. All temperature limits are guaranteed by design.

Note 2: Comparator Input Offset is defined as the center of the hysteresis zone.

Note 3: Hysteresis is defined as the difference of the trip points required to change comparator output states.

Note 4: V_{OD} is the overdrive voltage beyond the offset and hysteresis-determined trip points.

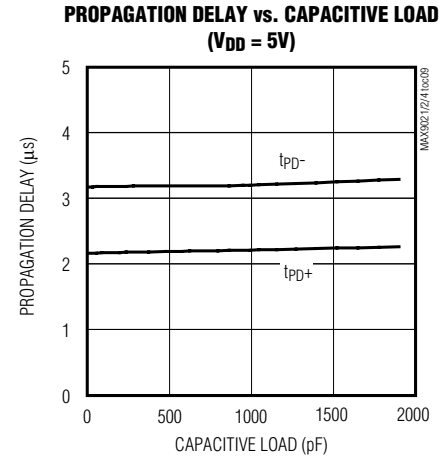
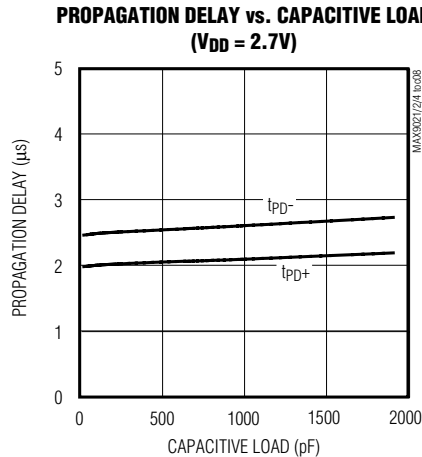
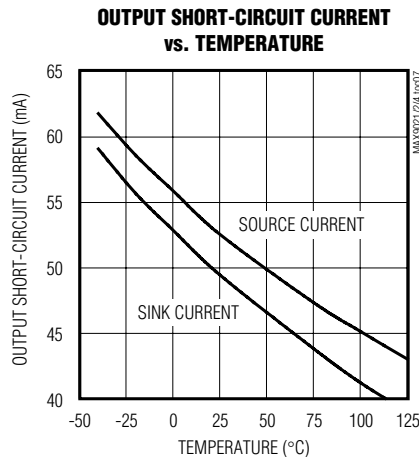
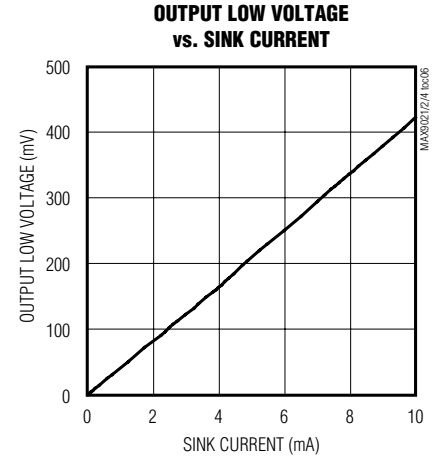
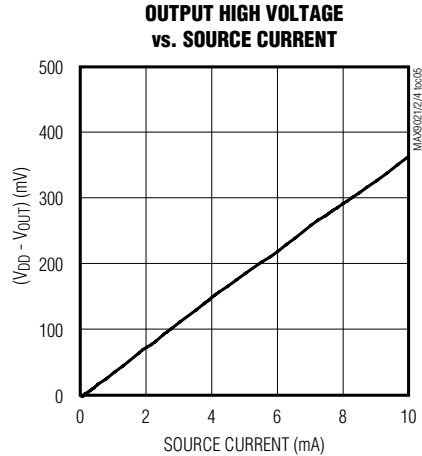
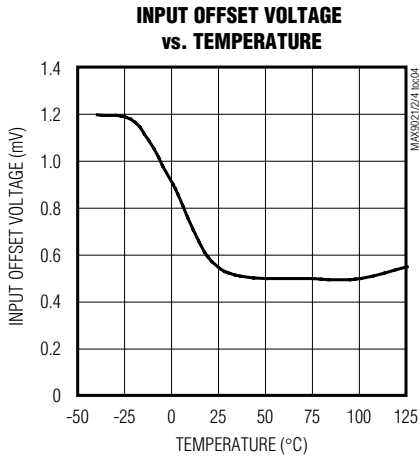
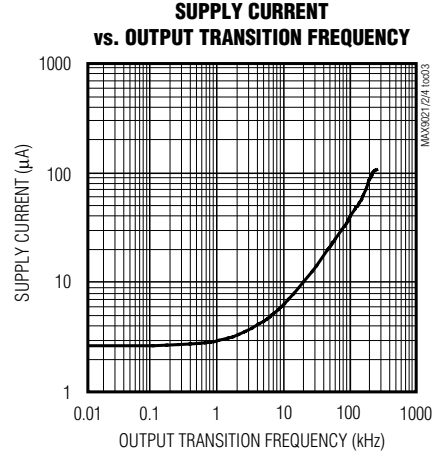
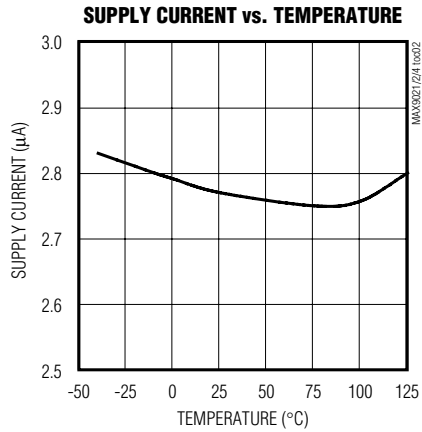
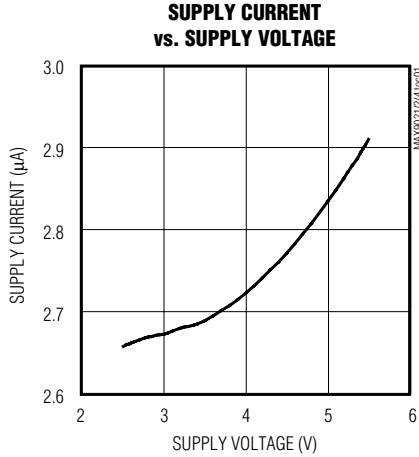
Note 5: Rise and fall times are measured between 10% and 90% at OUT.

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Typical Operating Characteristics

($V_{DD} = 5V$, $V_{SS} = 0$, $V_{CM} = 0$, $R_L = 10k\Omega$, $C_L = 15pF$, $V_{OD} = 100mV$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX9021/MAX9022/MAX9024

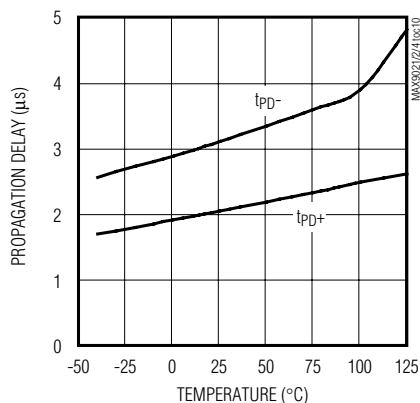


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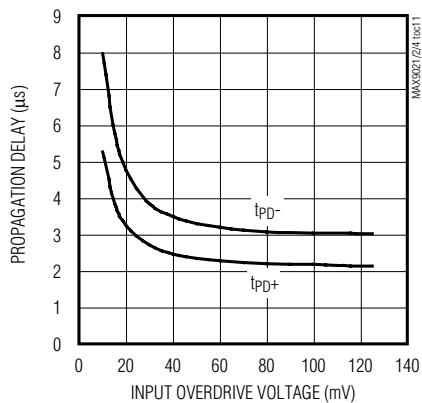
Typical Operating Characteristics (continued)

($V_{DD} = 5V$, $V_{SS} = 0$, $V_{CM} = 0$, $R_L = 10k\Omega$, $C_L = 15pF$, $V_{OD} = 100mV$, $T_A = +25^\circ C$, unless otherwise noted.)

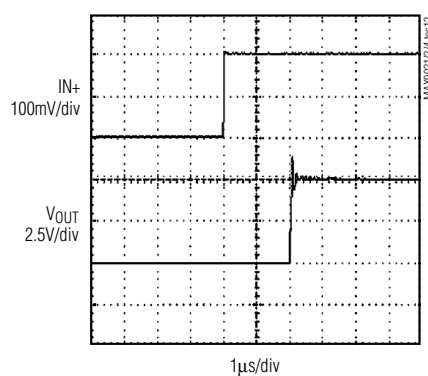
**PROPAGATION DELAY
vs. TEMPERATURE**



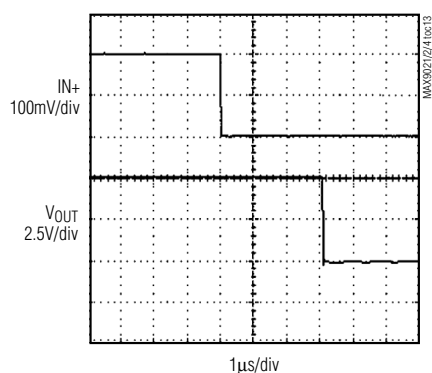
**PROPAGATION DELAY
vs. INPUT OVERDRIVE VOLTAGE**



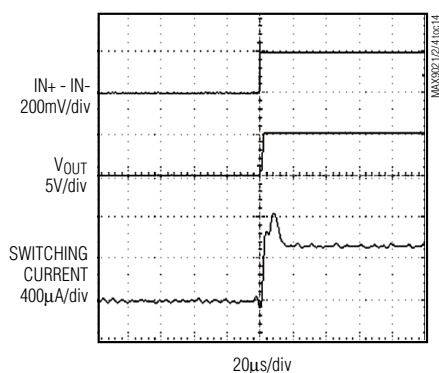
PROPAGATION DELAY (t_{PD+})



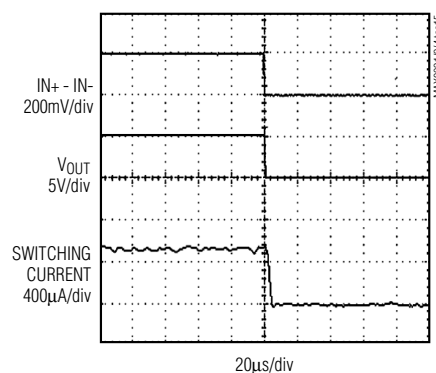
PROPAGATION DELAY (t_{PD-})



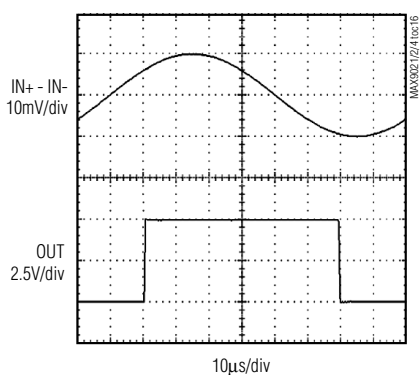
OUTPUT SWITCHING CURRENT, RISING



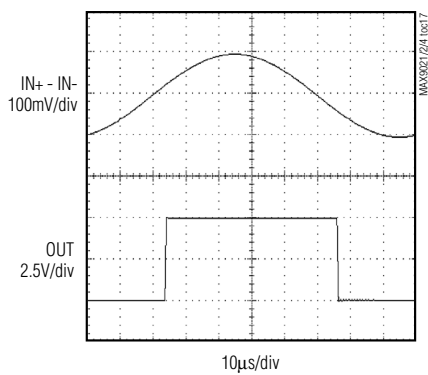
OUTPUT SWITCHING CURRENT, FALLING



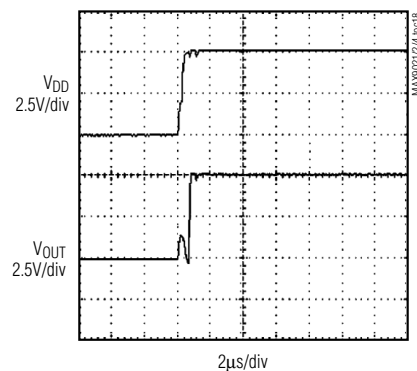
**10kHz RESPONSE
($V_{OD} = 10mV$)**



**10kHz RESPONSE
($V_{OD} = 100mV$)**



POWER-UP TIME



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Pin Description

PIN			NAME	FUNCTION
MAX9021	MAX9022	MAX9024		
1	—	—	IN+	Comparator Noninverting Input
2	4	11	V _{SS}	Negative Supply Voltage
3	—	—	IN-	Comparator Inverting Input
4	—	—	OUT	Comparator Output
5	8	4	V _{DD}	Positive Supply Voltage. Bypass with a 0.1µF capacitor to GND.
—	1	1	OUTA	Comparator A Output
—	2	2	INA-	Comparator A Inverting Input
—	3	3	INA+	Comparator A Noninverting Input
—	5	5	INB+	Comparator B Noninverting Input
—	6	6	INB-	Comparator B Inverting Input
—	7	7	OUTB	Comparator B Output
—	—	8	OUTC	Comparator C Output
—	—	9	INC-	Comparator C Inverting Input
—	—	10	INC+	Comparator C Noninverting Input
—	—	12	IND+	Comparator D Noninverting Input
—	—	13	IND-	Comparator D Inverting Input
—	—	14	OUTD	Comparator D Output

Detailed Description

The MAX9021/MAX9022/MAX9024 are single/dual/quad, low-cost, low-power comparators that consume only 2.8µA and provide a propagation delay, t_{PD} , typically 3µs. They have an operating-supply voltage from 2.5V to 5.5V when operating from a single supply and from ±1.25V to ±2.75V when operating from dual power supplies. Their common-mode input voltage range extends from the negative supply to within 1.1V of the positive supply. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

Applications Information

Adding Hysteresis

Hysteresis extends the comparator's noise margin by increasing the upper threshold and decreasing the lower threshold. A voltage-divider from the compara-

tor's output sets the trip voltage. Therefore, the trip voltage is related to the output voltage.

These comparators have 4mV internal hysteresis. Additional hysteresis can be generated with two resistors, using positive feedback (Figure 1). Use the following procedure to calculate resistor values:

- 1) Find the trip points of the comparator using these formulas:

$$V_{TH} = V_{REF} + ((V_{DD} - V_{REF})R_2) / (R_1 + R_2)$$

$$V_{TL} = V_{REF}(1 - (R_2 / (R_1 + R_2)))$$

where V_{TH} is the threshold voltage at which the comparator switches its output from high to low as V_{IN} rises above the trip point. V_{TL} is the threshold voltage at which the comparator switches its output from low to high as V_{IN} drops below the trip point.

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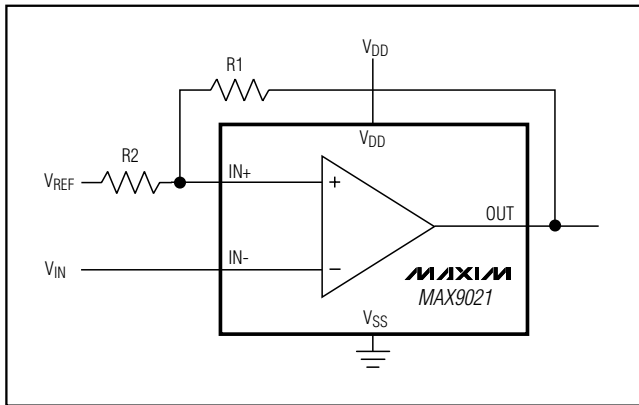


Figure 1. Additional Hysteresis

- 2) The hysteresis band will be:

$$V_{HYS} = V_{TH} - V_{TL} = V_{DD}(R2 / (R1 + R2))$$

- 3) In this example, let $V_{DD} = 5V$ and $V_{REF} = 2.5V$.

$$V_{TH} = 2.5V + 2.5V(R2 / (R1 + R2))$$

and

$$V_{TL} = 2.5V[(1 - (R2 / (R1 + R2)))]$$

- 4) Select $R2$. In this example, we will choose $1k\Omega$.
 5) Select V_{HYS} . In this example, we will choose $50mV$.
 6) Solve for $R1$.

$$V_{HYS} = V_{DD}(R2 / (R1 + R2))$$

$$0.050V = 5(1000\Omega / (R1 + 1000\Omega)) V$$

where $R1 \approx 100k\Omega$, $V_{TH} = 2.525V$, and $V_{TL} = 2.475V$.

The above-described design procedure assumes rail-to-rail output swing. If the output is significantly loaded, the results should be corrected.

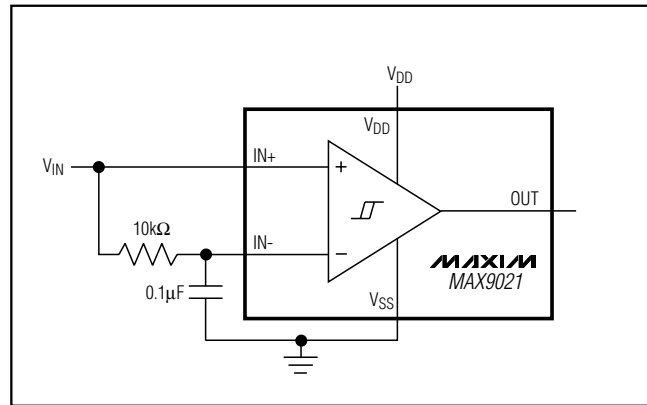


Figure 2. Time Averaging of the Input Signal for Data Recovery

Board Layout and Bypassing

Use $100nF$ bypass as a starting point. Minimize signal trace lengths to reduce stray capacitance. Minimize the capacitive coupling between $IN-$ and OUT . For slow-moving input signals (rise time $> 1ms$), use a $1nF$ capacitor between $IN+$ and $IN-$.

Biasing for Data Recovery

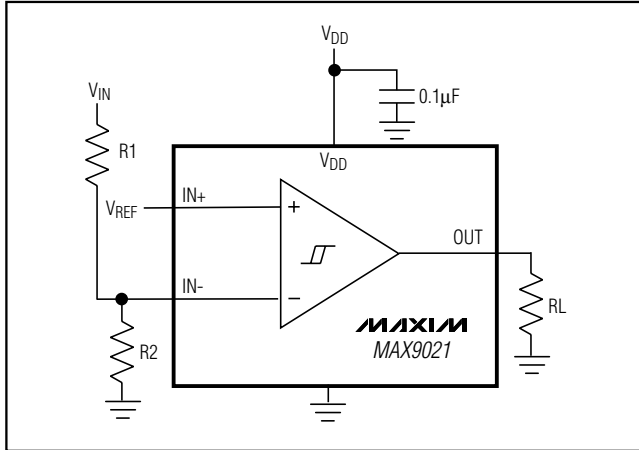
Digital data is often embedded into a bandwidth and amplitude-limited analog path. Recovering the data can be difficult. Figure 2 compares the input signal to a time-averaged version of itself. This self-biases the threshold to the average input voltage for optimal noise margin. Even severe phase distortion is eliminated from the digital output signal. Be sure to choose $R1$ and $C1$ so that:

$$f_{CAR} \gg 1 / (2\pi R1 C1)$$

where f_{CAR} is the fundamental carrier frequency of the digital data stream.

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Typical Application Circuit



Chip Information

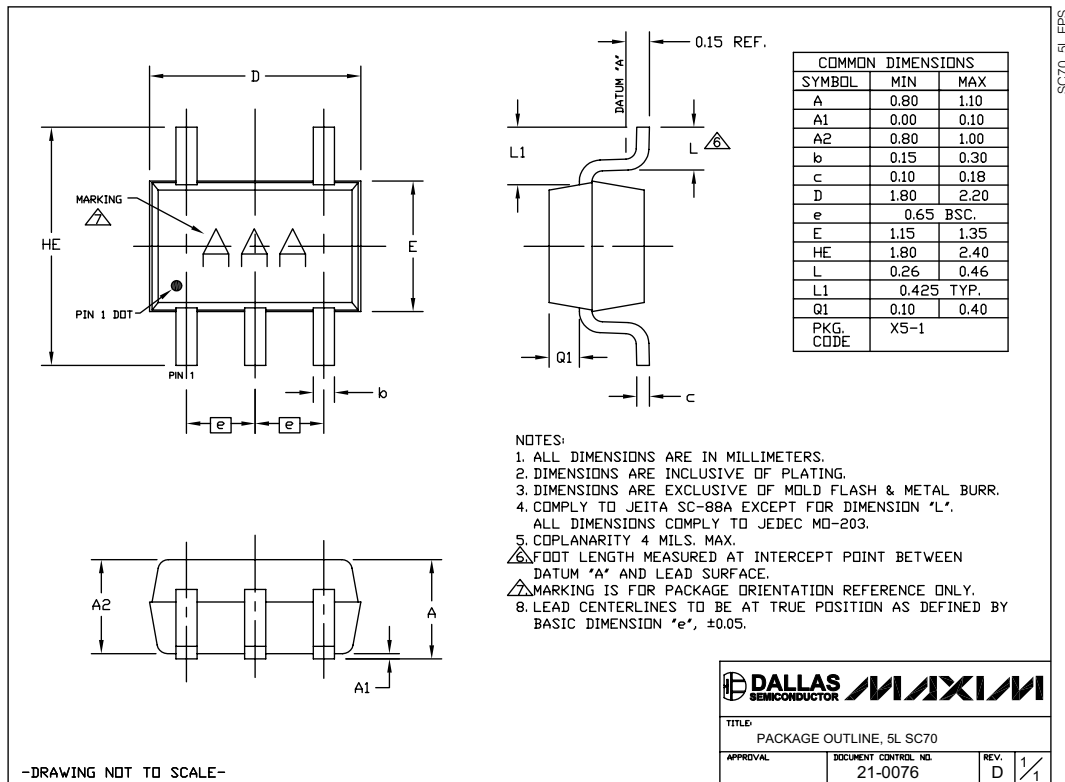
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MAX9022 TRANSISTOR COUNT: 212

MAX9024 TRANSISTOR COUNT: 424

Package Information

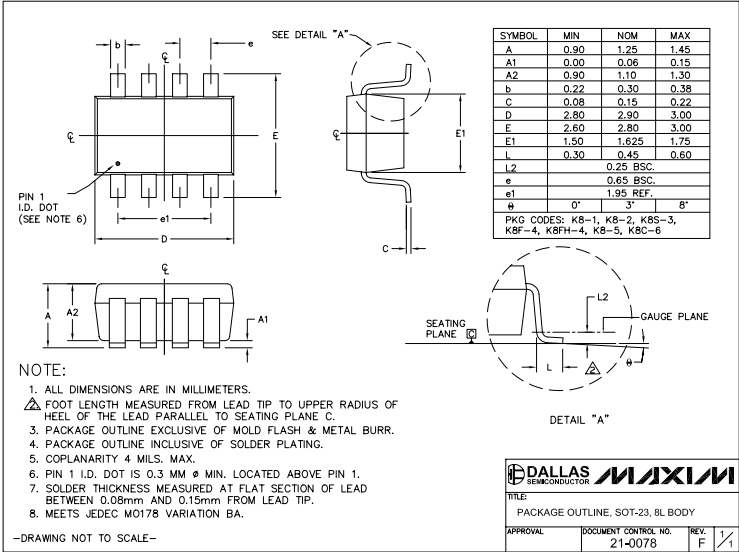
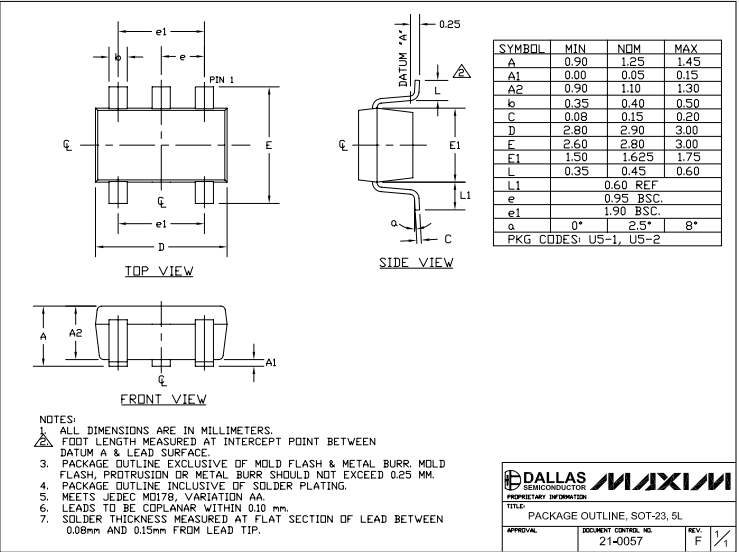
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



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Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



Revision History

Pages changed at Rev 2: 1, 2, 6, 7, 8

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