5th-Order, Lowpass, Switched-Capacitor Filters

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
IN, OUT, COM, OS, CLK, $\overline{SHDN}$ .....-0.3V to (V_{DD} + 0.3V)
OUT Short-Circuit Duration.....1s
Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 4.1mW/°C above +70°C) 330mW

Operating Temperature Ranges
MAX74 _ _C_A .....0°C to +70°C
MAX74 _ _E_A .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX7418–MAX7421

(V_{DD} = +5V, filter output measured at OUT, 10kΩ ll 50pF load to GND at OUT, OS = COM, 0.1µF capacitor from COM to GND, $\overline{SHDN}$ = V_{DD}, f_{CLK} = 2.2MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER CHARACTERISTICS							
Corner Frequency	f_C	V_{IN} = 4Vp-p (Note 1)			0.001 to 30		kHz
Clock-to-Corner Ratio	f_{CLK} / f_C				100:1		
Clock-to-Corner Tempco					10		ppm/°C
Output Voltage Range				0.25		V_{DD} - 0.25	V
Output Offset Voltage	V_{OFFSET}	V_{IN} = V_{COM} = V_{DD} / 2			±4	±25	mV
DC Insertion Gain with Output Offset Removed		V_{COM} = V_{DD} / 2 (Note 2)	MAX7418/MAX7421	0	0.2	0.4	dB
			MAX7419/MAX7420	-0.2	0	+0.2	
Total Harmonic Distortion plus Noise	THD+N	f_{IN} = 2KHz, V_{IN} = 4Vp-p, measurement bandwidth = 80kHz	MAX7418		-76		dB
			MAX7419		-78		
			MAX7420		-67		
			MAX7421		-78		
Offset Voltage Gain	A_{OS}	OS to OUT			1		V/V
COM Voltage Range	V_{COM}	Input, COM externally driven		2.0	2.5	3.0	V
		Output, COM unconnected		2.3	2.5	2.7	
Input Voltage Range at OS	V_{OS}	Input, OS externally driven			V_{COM} ±0.1		V
Input Resistance at COM	R_{COM}			100	140		kΩ
Clock Feedthrough					5		mVp-p
Resistive Output Load Drive	R_L			10	1		kΩ
Maximum Capacitive Output Load Drive	C_L			50	500		pF
Input Leakage Current at COM		$\overline{SHDN}$ = GND, V_{COM} = 0 to V_{DD}			±0.1	±10	µA
Input Leakage Current at OS		V_{OS} = 0 to V_{DD}			±0.1	±10	µA
CLOCK							
Internal Oscillator Frequency	f_{OSC}	C_{OSC} = 1000pF (Note 3)	MAX7418/MAX7421	68	87	106	kHz
			MAX7419/MAX7420	86	110	135	
Clock Output Current (Internal Oscillator Mode)	I_{CLK}	V_{CLK} = 0 or 5V	MAX7418/MAX7421		±40	±60	µA
			MAX7419/MAX7420		±50	±75	
Clock Input High	V_{IH}			4.5			V
Clock Input Low	V_{IL}					0.5	V

ELECTRICAL CHARACTERISTICS—MAX7418–MAX7421 (continued)

(V_{DD} = +5V, filter output measured at OUT, 10kΩ ll 50pF load to GND at OUT, OS = COM, 0.1µF capacitor from COM to GND, $\overline{SHDN}$ = V_{DD}, f_{CLK} = 2.2MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			4.5		5.5	V
Supply Current	I_{DD}	Operating mode, no load	MAX7418/MAX7421		2.9	3.6	mA
			MAX7419/MAX7420		3.4	4.1	
Shutdown Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = GND			0.2	1	µA
Power-Supply Rejection Ratio	PSRR	IN = COM (Note 4)			70		dB
SHUTDOWN							
$\overline{SHDN}$ Input High	V_{SDH}			4.5			V
$\overline{SHDN}$ Input Low	V_{SDL}					0.5	V
$\overline{SHDN}$ Input Leakage Current		$V_{\overline{SHDN}}$ = 0 to V_{DD}			±0.2	±10	µA

ELECTRICAL CHARACTERISTICS—MAX7422–MAX7425

(V_{DD} = +3V, filter output measured at OUT pin, 10kΩ ll 50pF load to GND at OUT, OS = COM, 0.1µF capacitor from COM to GND, $\overline{SHDN}$ = V_{DD}, f_{CLK} = 2.2MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER CHARACTERISTICS							
Corner-Frequency Range	f_C	V_{IN} = 2.5Vp-p (Note 1)	MAX7422/MAX7425	100:1 to 45			kHz
			MAX7423/MAX7424				
Clock-to-Corner Ratio	f_{CLK}/f_C				100:1		
Clock-to-Corner Tempco					10		ppm/°C
Output Voltage Range				0.25		V_{DD} - 0.25	V
Output Offset Voltage	V_{OFFSET}	V_{IN} = V_{COM} = V_{DD} / 2			±4	±25	mV
DC Insertion Gain with Output Offset Removed		V_{COM} = V_{DD} / 2 (Note 2)	MAX7422/MAX7425	0	0.2	0.4	dB
			MAX7423/MAX7424	-0.2	0	+0.2	
Total Harmonic Distortion plus Noise	THD+N	f_{IN} = 2kHz, V_{IN} = 2.5Vp-p, measurement bandwidth = 80kHz	MAX7422		-80		dB
			MAX7423		-81		
			MAX7424		-70		
			MAX7425		-80		
Offset Voltage Gain	A_{OS}	OS to OUT			1		V/V
COM Voltage Range	V_{COM}	Input, COM externally driven		1.4	1.5	1.6	V
		Output, COM internally driven		1.4	1.5	1.6	
Input Voltage Range at OS	V_{OS}	Measured with respect to COM			V_{COM} ±0.1		V
Input Resistance at COM	R_{COM}			100	140		kΩ
Clock Feedthrough					3		mVp-p
Resistive Output Load Drive	R_L			10	1		kΩ
Maximum Capacitive Load at OUT	C_L			50	500		pF
Input Leakage Current at COM		$\overline{SHDN}$ = GND, V_{COM} = 0 to V_{DD}			±0.1	±10	µA
Input Leakage Current at OS		V_{OS} = 0 to V_{DD}			±0.1	±10	µA

5th-Order, Lowpass, Switched-Capacitor Filters

ELECTRICAL CHARACTERISTICS—MAX7422–MAX7425 (continued)

(V_{DD} = +3V, filter output measured at OUT pin, 10kΩ II 50pF load to GND at OUT, OS = COM, 0.1µF capacitor from COM to GND, $\overline{SHDN}$ = V_{DD}, f_{CLK} = 2.2MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CLOCK							
Internal Oscillator Frequency	f_{OSC}	C_{OSC} = 1000pF (Note 3)	MAX7422/MAX7425	68	87	106	kHz
			MAX7423/MAX7424	86	110	135	
Clock Output Current (Internal Oscillator Mode)	I_{CLK}		MAX7422/MAX7425	68	87	106	kHz
			MAX7423/MAX7424	86	110	135	
Clock Input High	V_{IH}			2.5			
Clock Input Low	V_{IL}					0.5	
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			2.7		3.6	V
Supply Current	I_{DD}	Operating mode, no load	MAX7422/MAX7425		2.6	3.4	mA
			MAX7423/MAX7424		3.0	3.8	
Shutdown Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = GND			0.2	1	µA
Power-Supply Rejection Ratio	PSRR	Measured at DC			70		dB
SHUTDOWN							
$\overline{SHDN}$ Input High	V_{SDH}			2.5			V
$\overline{SHDN}$ Input Low	V_{SDL}					0.5	V
$\overline{SHDN}$ Input Leakage Current		$V_{\overline{SHDN}}$ = 0 to V_{DD}			±0.2	±10	µA

FILTER CHARACTERISTICS

(V_{DD} = +5V for MAX7418-MAX7420, V_{DD} = +3V for MAX7422-MAX7425 filter output measured at OUT, 10kΩ ll 50pF load to GND at OUT, $\overline{SHDN}$ = V_{DD}, f_{CLK} = 2.2MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ELLIPTIC, R = 1.2—MAX7421/MAX7425					
Insertion Gain with DC Gain Error Removed (Note 4)	$f_{IN} = 0.38f_C$	-0.4	-0.2	0.4	dB
	$f_{IN} = 0.68f_C$	-0.4	-0.2	0.4	
	$f_{IN} = 0.87f_C$	-0.4	-0.2	0.4	
	$f_{IN} = 0.97f_C$	-0.4	-0.2	0.4	
	$f_{IN} = f_C$	-0.7	-0.2	0.2	
	$f_{IN} = 1.25f_C$		-36	-33	
	$f_{IN} = 1.43f_C$		-37.2	-35	
	$f_{IN} = 3.25f_C$		-37.2	-35	
BESSEL FILTERS—MAX7419/MAX7423					
Insertion Gain Relative to DC Gain	$f_{IN} = 0.5f_C$	-1	-0.74		dB
	$f_{IN} = f_C$	-3.6	-3.0	-2.4	
	$f_{IN} = 4f_C$		-41.0	-35	
	$f_{IN} = 7f_C$		-67	-60	
BESSEL FILTERS—MAX7419/MAX7423					
Insertion Gain Relative to DC Gain	$f_{IN} = 0.5f_C$	-1.0	-0.74		dB
	$f_{IN} = 4f_C$	-3.6	-3.0	-2.4	
	$f_{IN} = 7f_C$		-41.0	-35	
	$f_{IN} = 7f_C$		-67	-60	
BUTTERWORTH FILTERS—MAX7420/MAX7424					
Insertion Gain Relative to DC Gain	$f_{IN} = 0.5f_C$	-0.3	0		dB
	$f_{IN} = f_C$	-3.6	-3.0	-2.4	
	$f_{IN} = 3f_C$		-47.5	-43	
	$f_{IN} = 5f_C$		-70	-65	

Note 1: The maximum f_C is defined as the clock frequency f_{CLK} = 100 x f_C at which the peak S / (THD+N) drops to 68dB with a sinusoidal input at 0.2f_C. Maximum f_C increases as V_{IN} signal amplitude decreases.

Note 2: DC insertion gain is defined as $\Delta V_{OUT} / \Delta V_{IN}$.

Note 3: MAX7418/MAX7421/MAX7422/MAX7425: f_{OSC} (kHz) ≅ $87x10^3$ / C_{OSC} (pF).
MAX7419/MAX7420/MAX7423/MAX7424: f_{OSC} (kHz) ≅ $110x10^3$ / C_{OSC} (pF).

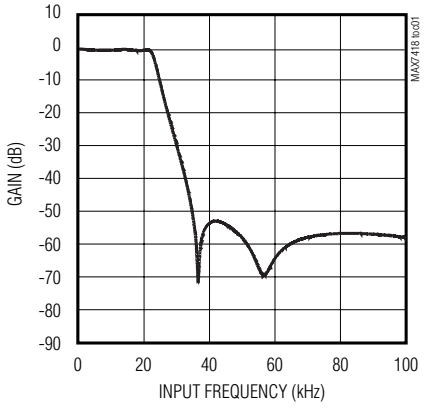
Note 4: PSRR is the change in output voltage from a V_{DD} of 4.5V and a V_{DD} of 5.5V.

5th-Order, Lowpass, Switched-Capacitor Filters

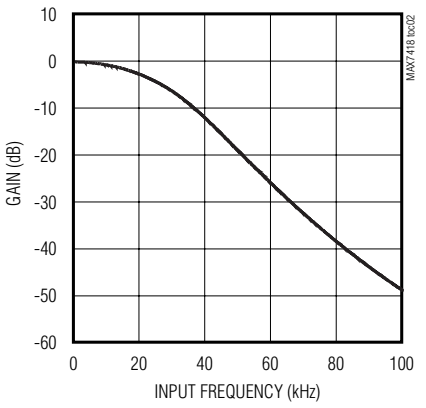
Typical Operating Characteristics

(V_{DD} = +5V for MAX7418–MAX7421, V_{DD} = +3V for MAX7422–MAX7425; f_{CLK} = 2.2MHz; $\overline{SHDN}$ = V_{DD}; V_{COM} = V_{OS} = V_{DD} / 2; T_A = +25°C; unless otherwise noted.)

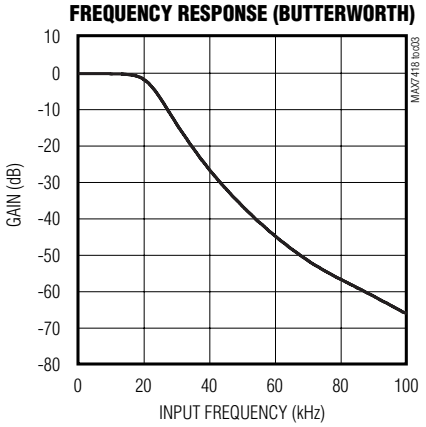
MAX7418/MAX7422
FREQUENCY RESPONSE (ELLIPTIC, R = 1.6)



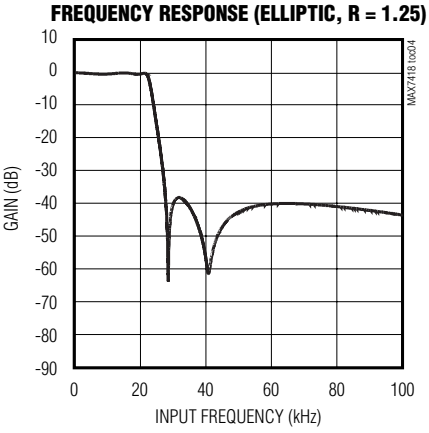
MAX7419/MAX7423
FREQUENCY RESPONSE (BESSEL)



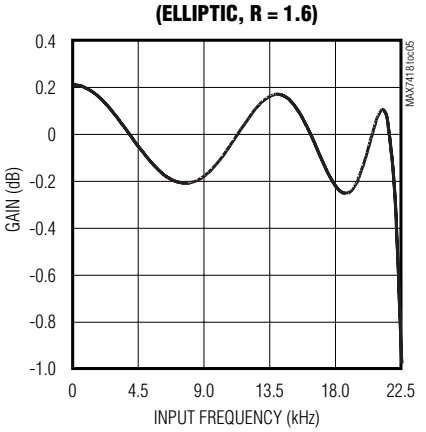
MAX7420/MAX7424
FREQUENCY RESPONSE (BUTTERWORTH)



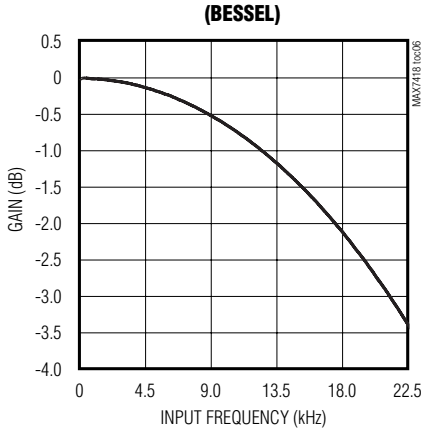
MAX7421/MAX7425
FREQUENCY RESPONSE (ELLIPTIC, R = 1.25)



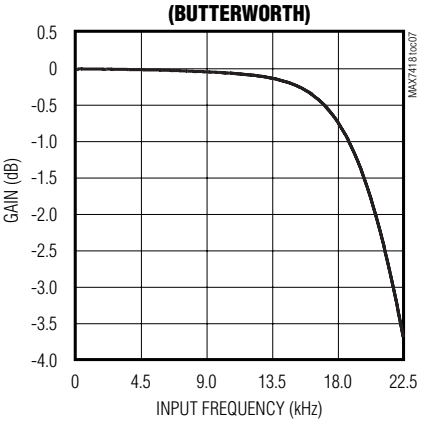
MAX7418/MAX7422
PASSBAND FREQUENCY RESPONSE
(ELLIPTIC, R = 1.6)



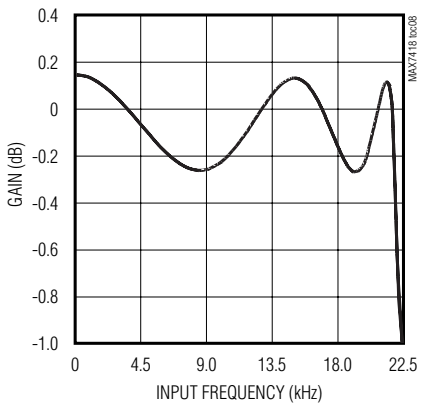
MAX7419/MAX7423
PASSBAND FREQUENCY RESPONSE
(BESSEL)



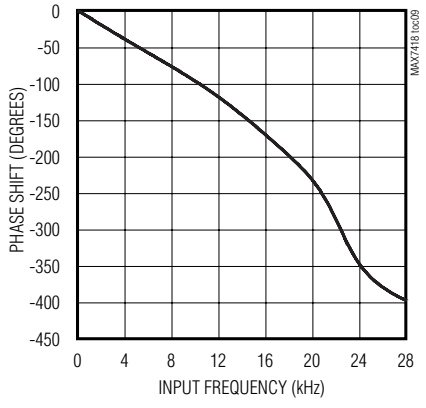
MAX7420/MAX7424
PASSBAND FREQUENCY RESPONSE
(BUTTERWORTH)



MAX7421/MAX7425
PASSBAND FREQUENCY RESPONSE
(ELLIPTIC, R = 1.25)



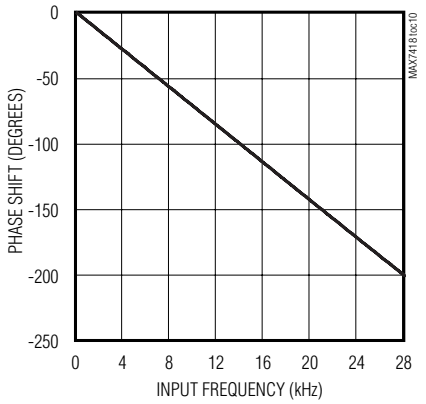
MAX7418/MAX7422
PHASE RESPONSE (ELLIPTIC, R = 1.6)



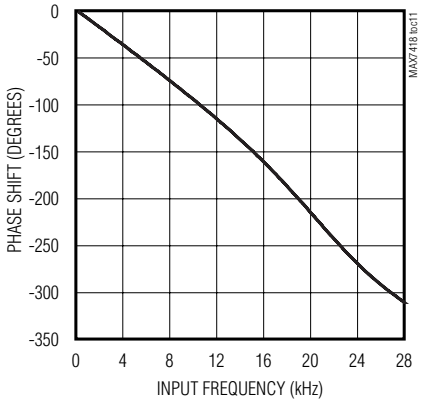
Typical Operating Characteristics (continued)

(V_{DD} = +5V for MAX7418–MAX7421, V_{DD} = +3V for MAX7422–MAX7425; f_{CLK} = 2.2MHz; $\overline{SHDN}$ = V_{DD}; V_{COM} = V_{OS} = V_{DD} / 2; T_A = +25°C; unless otherwise noted.)

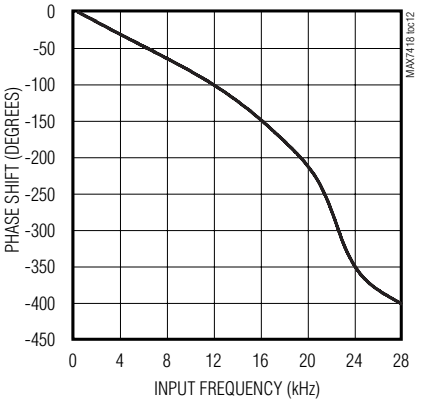
MAX7419/MAX7423
PHASE RESPONSE (BESSEL)



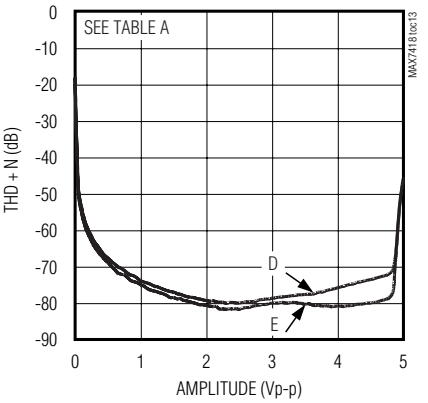
MAX7420/MAX7424
PHASE RESPONSE (BUTTERWORTH)



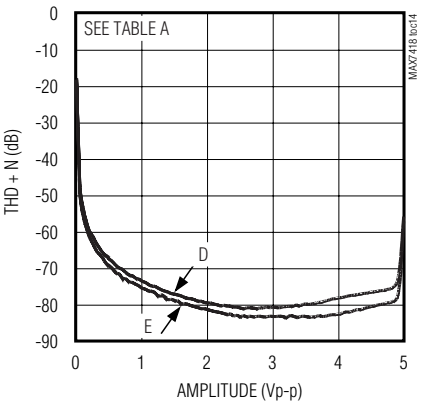
MAX7424/MAX7425
PHASE RESPONSE (ELLIPTIC, R = 1.25)



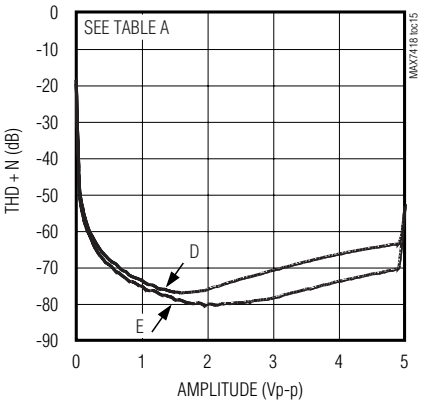
MAX7418
THD + NOISE vs. INPUT SIGNAL AMPLITUDE
(ELLIPTIC, R = 1.6)



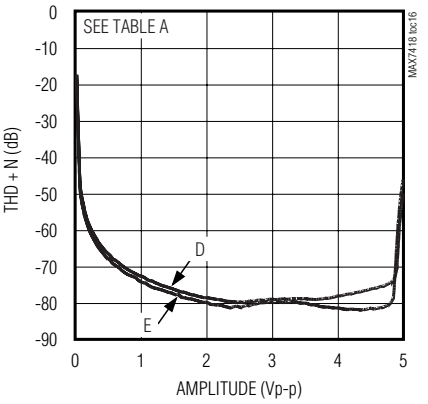
MAX7419
THD + NOISE vs. INPUT SIGNAL AMPLITUDE
(BESSEL)



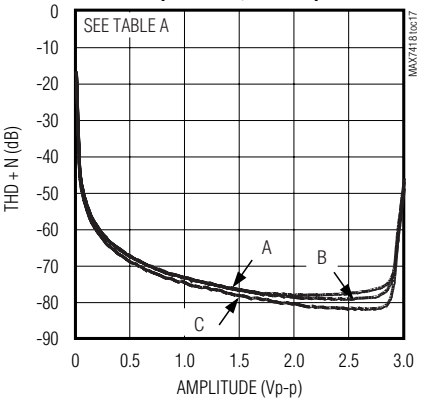
MAX7420
THD + NOISE vs. INPUT SIGNAL AMPLITUDE
(BUTTERWORTH)



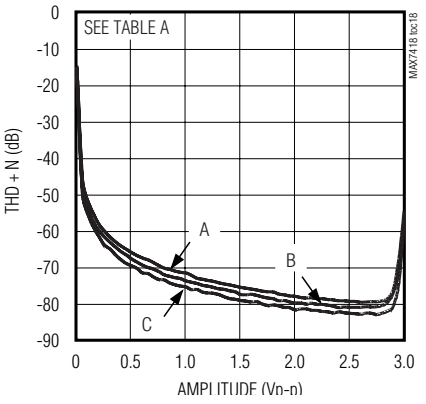
MAX7421
THD + NOISE vs. INPUT SIGNAL AMPLITUDE
(ELLIPTIC, R = 1.25)



MAX7422
THD + NOISE vs. INPUT SIGNAL AMPLITUDE
(ELLIPTIC, R = 1.6)



MAX7423
THD + NOISE vs. INPUT SIGNAL AMPLITUDE
(BESSEL)

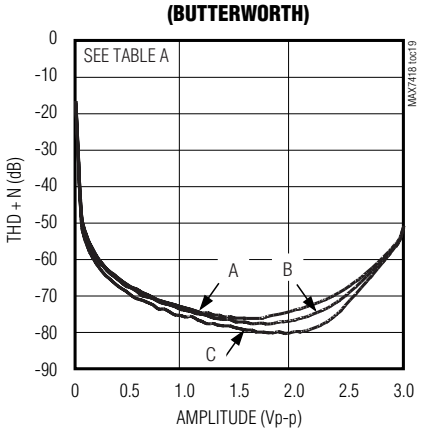


5th-Order, Lowpass, Switched-Capacitor Filters

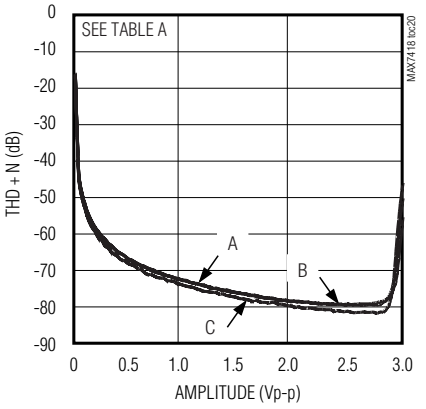
Typical Operating Characteristics (continued)

(V_{DD} = +5V for MAX7418–MAX7421, V_{DD} = +3V for MAX7422–MAX7425; f_{CLK} = 2.2MHz; $\overline{SHDN}$ = V_{DD}; V_{COM} = V_{OS} = V_{DD} / 2; T_A = +25°C; unless otherwise noted.)

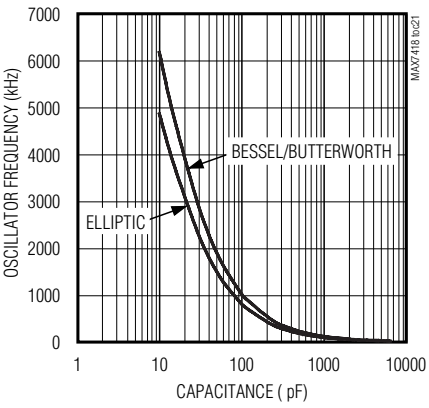
MAX7424
THD + NOISE vs. INPUT SIGNAL AMPLITUDE (BUTTERWORTH)



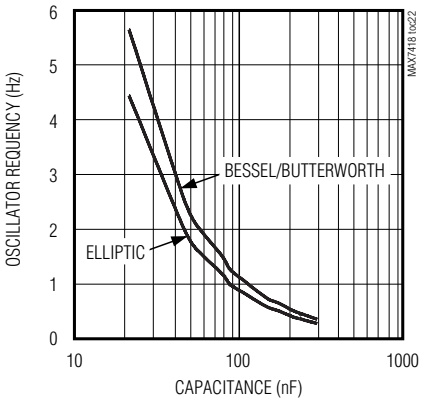
MAX7425
THD + NOISE vs. INPUT SIGNAL AMPLITUDE (ELLIPTIC, R = 1.25)



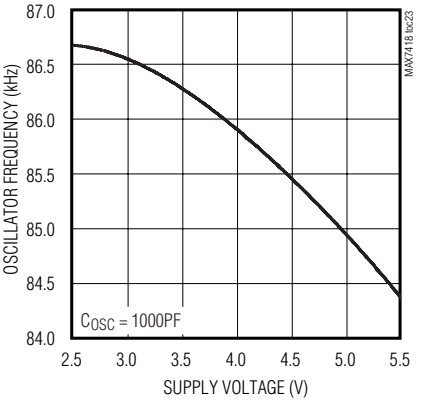
INTERNAL OSCILLATOR FREQUENCY vs. SMALL CAPACITANCE (pF)



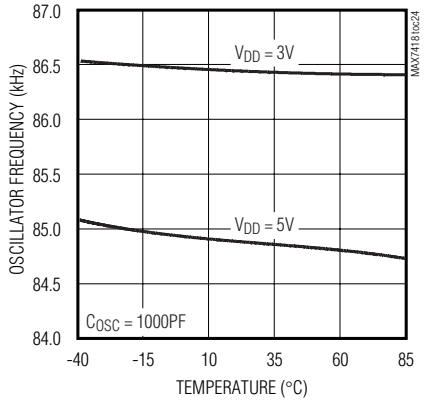
INTERNAL OSCILLATOR FREQUENCY vs. LARGE CAPACITANCE (nF)



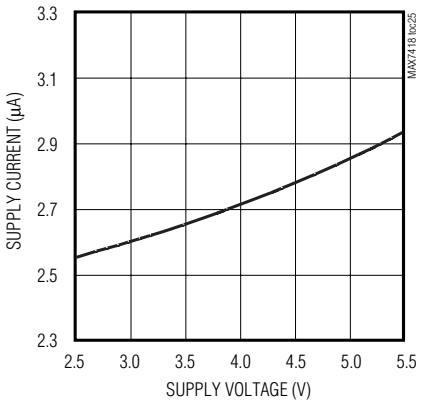
ELLIPTIC INTERNAL OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



ELLIPTIC INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE



ELLIPTIC SUPPLY CURRENT vs. SUPPLY VOLTAGE



ELLIPTIC SUPPLY CURRENT vs. TEMPERATURE

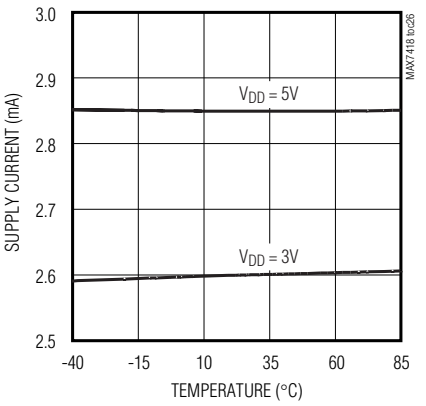


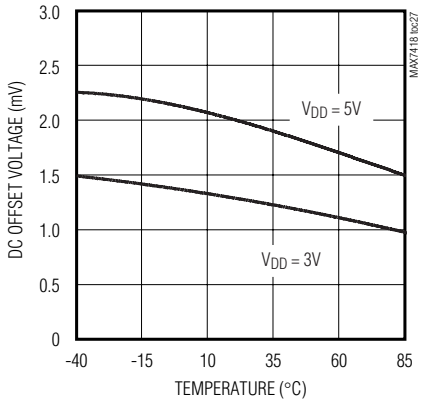
Table A.

LABEL	f_{IN} (kHz)	f_C (kHz)	f_{CLK} (kHz)	BW (kHz)
A	2	30	3000	80
B	2	22	2200	80
C	1	10	1000	22
D	2	22	2200	80
E	1	10	1000	22

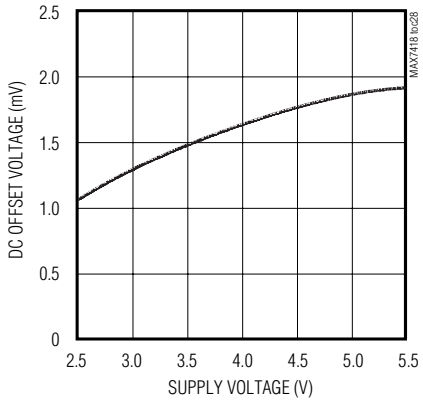
Typical Operating Characteristics (continued)

(V_{DD} = +5V for MAX7418–MAX7421, V_{DD} = +3V for MAX7422–MAX7425; f_{CLK} = 2.2MHz; $\overline{SHDN}$ = V_{DD}; V_{COM} = V_{OS} = V_{DD} / 2; T_A = +25°C; unless otherwise noted.)

DC OFFSET VOLTAGE vs. TEMPERATURE



DC OFFSET VOLTAGE vs. SUPPLY VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1	COM	Common Input Pin. Biased internally at midsupply. Bypass COM externally to GND with a 0.1µF capacitor. To override internal biasing, drive COM with an external supply.
2	IN	Filter Input
3	GND	Ground
4	V_{DD}	Positive Supply Input: +5V for MAX7418–MAX7421, +3V for MAX7422–MAX7425. Bypass V_{DD} to GND with a 0.1µF capacitor.
5	OUT	Filter Output
6	OS	Offset Adjust Input. To adjust output offset, connect OS to an external supply through a resistive voltage-divider (Figure 4). Connect OS to COM if no offset adjustment is needed. The *Offset and Common-Mode Input Adjustment* section.
7	$\overline{SHDN}$	Shutdown Input. Drive low to enable shutdown mode; drive high or connect to V_{DD} for normal operation.
8	CLK	Clock Input. Connect an external capacitor (C_{OSC}) from CLK to ground. To override the internal oscillator, connect CLK to an external clock: $f_C = f_{CLK}$ /100.

Detailed Description

The MAX7418/MAX7421/MAX7422/MAX7425 elliptic lowpass filters provide sharp rolloff with good stopband rejection. The MAX7419/MAX7423 Bessel filters provide low overshoot and fast settling responses, and the MAX7420/MAX7424 Butterworth filters provide a maximally flat passband response. All parts operate with a 100:1 clock-to-corner frequency ratio.

Most switch capacitor filters (SCFs) are designed with biquadratic sections. Each section implements two pole-zero pairs, and the sections can be cascaded to produce higher order filters. The advantage to this approach is ease of design. However, this type of design is highly sensitive to component variations if any section's Q is high. The MAX7418–MAX7425 use an alternative approach, which is to emulate a passive network using switched-capacitor integrators with summing and scaling. The passive network may be synthesized using CAD programs, or may be found in many filter books. Figure 1 shows a basic 5th-order ladder filter structure.

5th-Order, Lowpass, Switched-Capacitor Filters

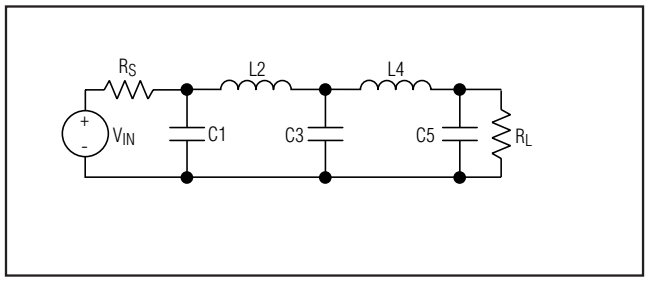


Figure 1. 5th-Order Ladder Filter Network

An SCF that emulates a passive ladder filter retains many of the same advantages. The component sensitivity of a passive ladder filter is low when compared to a cascaded biquadratic design because each component affects the entire filter shape rather than a single pole-zero pair. In other words, a mismatched component in a biquadratic design has a concentrated error on its respective poles, while the same mismatch in a ladder filter design spreads its error over all poles.

Elliptic Characteristics

Lowpass elliptic filters such as the MAX7418/MAX7421/MAX7422/MAX7425 provide the steepest possible rolloff with frequency of the four most common filter types (Butterworth, Bessel, Chebyshev, and elliptic). The high-Q value of the poles near the passband edge combined with the stopband zeros allow for the sharp attenuation characteristic of elliptic filters, making these devices ideal for anti-aliasing and post-DAC filtering in single-supply systems (see *Anti-Aliasing and Post-DAC Filtering*).

In the frequency domain, the first transmission zero causes the filter's amplitude to drop to a minimum level (Figure 2). Beyond this zero, the response rises as the frequency increases until the next transmission zero. The stopband begins at the stopband frequency, f_S. At frequencies above f_S, the filter's gain does not exceed the gain at f_S. The corner frequency, f_C, is defined as the point at which the filter output attenuation falls just below the passband ripple. The transition ratio (r) is defined as the ratio of the stopband frequency to the corner frequency:

$$r = f_S / f_C$$

The MAX7418/MAX7422 have a transition ratio of 1.6 and typically 53dB of stopband rejection. The MAX7421/MAX7425 have a transition ratio of 1.25 (providing a steeper rolloff) and typically 37dB of stopband rejection.

Bessel Characteristics

Lowpass Bessel filters such as the MAX7419/MAX7423 delay all frequency components equally, preserving the line up shape of step inputs (subject to the attenuation of the higher frequencies). Bessel filters settle quickly—an important characteristic in applications that use a multiplexer (mux) to select an input signal for an analog-to-digital converter (ADC). An anti-aliasing filter placed between the mux and the ADC must settle quickly after a new channel is selected.

Butterworth Characteristics

Lowpass Butterworth filters such as the MAX7420/MAX7424 provide a maximally flat passband response, making them ideal for instrumentation applications that require minimum deviation from the DC gain throughout the passband.

The difference between Bessel and Butterworth filters can be observed when a 1kHz square wave is applied to the filter input (Figure 3, trace A). With the filter cutoff frequencies set at 5kHz, trace B shows the Bessel filter response and trace C shows the Butterworth filter response.

Clock Signal

External Clock

These SCFs are designed for use with external clocks that have a 40% to 60% duty cycle. When using an external clock, drive the CLK pin with a CMOS gate powered from 0 to V_{DD}. Varying the rate of the external clock adjusts the corner frequency of the filter:

$$f_C = \frac{f_{CLK}}{100}$$

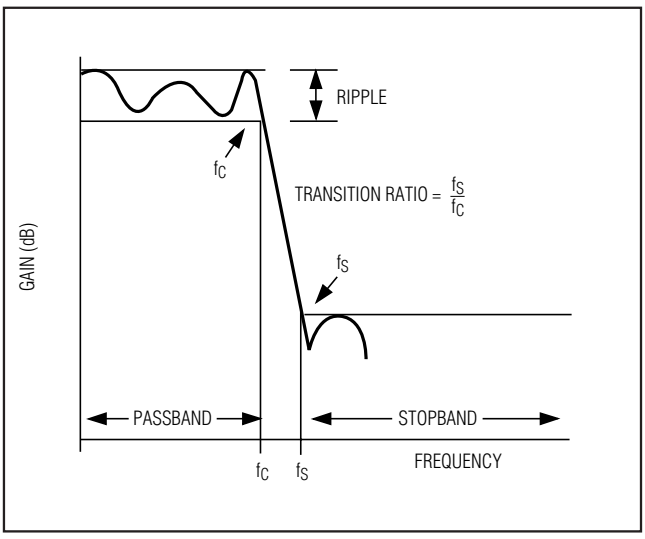


Figure 2. Elliptic Filter Response

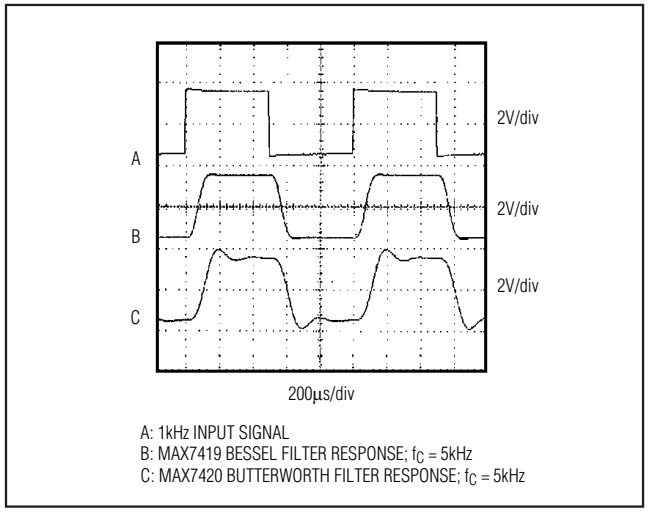


Figure 3. Bessel vs. Butterworth Filter Response

Internal Clock

When using the internal oscillator, the capacitance (C_{OSC}) on CLK determines the oscillator frequency:

$$f_{OSC}(kHz) = \frac{k}{C_{OSC}(pF)}$$

where

k=87x10^3 for the MAX7418/MAX7421/MAX7422/MAX7425

and

k=110X10^3 for the MAX7419/MAX7420/MAX7423/ MAX7424.

Since C_{OSC} is in the low picofarads, minimize the stray capacitance at CLK so that it does not affect the internal oscillator frequency. Varying the rate of the internal oscillator adjusts the filter's corner frequency by a 100:1 clock-to-corner frequency ratio. For example, an internal oscillator frequency of 2.2kHz produces a nominal corner frequency of 2.2MHz.

Input Impedance vs. Clock Frequencies

The MAX7418–MAX7425s' input impedance is effectively that of a switched-capacitor resistor (see the following equation), and is inversely proportional to frequency. The input impedance values determined by the equation represent the average input impedance, since the input current is not continuous. As a rule, use a driver with an output resistance less than 10% of the filter's input impedance.

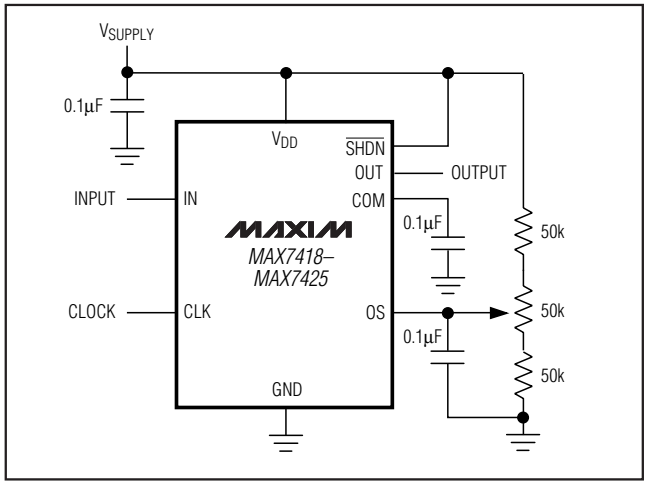


Figure 4. Offset Adjustment Circuit

Estimate the input impedance of the filter by using the following formula:

$$Z_{IN} = \frac{1}{(f_{CLK} \times C_{IN})}$$

where f_{CLK} = clock frequency and C_{IN} = 1pF.

Low-Power Shutdown Mode

The MAX7418–MAX7425 have a shutdown mode that is activated by driving $\overline{SHDN}$ low. In shutdown mode, the filter supply current reduces to 0.2µA, and the output of the filter becomes high impedance. For normal operation, drive $\overline{SHDN}$ high or connect to V_{DD}.

Applications Information

Offset (OS) and Common-Mode (COM) Input Adjustment

COM sets the common-mode input voltage and is biased at midsupply with an internal resistor-divider. If the application does not require offset adjustment, connect OS to COM. For applications in which offset adjustment is required, apply an external bias voltage through a resistor-divider network to OS, as shown in Figure 4. For applications that require DC level shifting, adjust OS with respect to COM. (**Note:** Do not leave OS unconnected.) The output voltage is represented by these equations:

$$V_{OUT} = (V_{IN} - V_{COM}) + V_{OS}$$

$$V_{COM} = \frac{V_{DD}}{2} \text{ (typical)}$$

where (V_{IN} - V_{COM}) is lowpass filtered by the SCF and OS is added at the output stage. See the *Electrical*

5th-Order, Lowpass, Switched-Capacitor Filters

Characteristics table for the input voltage range of COM and OS. Changing the voltage on COM or OS significantly from midsupply reduces the dynamic range.

Power Supplies

The MAX7418–MAX7421 operate from a single +5V supply and the MAX7422–MAX7425 operate from a single +3V supply. Bypass V_{DD} to GND with a 0.1µF capacitor. If dual supplies are required, connect COM to the system ground and GND to the negative supply. Figure 5 shows an example of dual-supply operation. Single-supply and dual-supply performance are equivalent. For either single-supply or dual-supply operation, drive CLK and $\overline{SHDN}$ from GND (V- in dual supply operation) to V_{DD}. Use the MAX7418–MAX7421 for ±2.5, and use the MAX7422–MAX7425 for ±1.5V. For ±5V dual-supply applications, refer to the MAX291/MAX292/MAX295/MAX296 and MAX293/MAX294/MAX297 data sheets.

Input Signal Amplitude Range

The optimal input signal range is determined by observing the voltage level at which the signal-to-noise plus distortion (SINAD) ratio is maximized for a given corner frequency. The *Typical Operating Characteristics* show the THD + Noise response as the input signal's peak-to-peak amplitude is varied.

Anti-Aliasing and Post-DAC Filtering

When using the MAX7418–MAX7425 for anti-aliasing or post-DAC filtering, synchronize the DAC (or ADC) and the filter clocks. If the clocks are not synchronized, beat frequencies may alias into the desired passband.

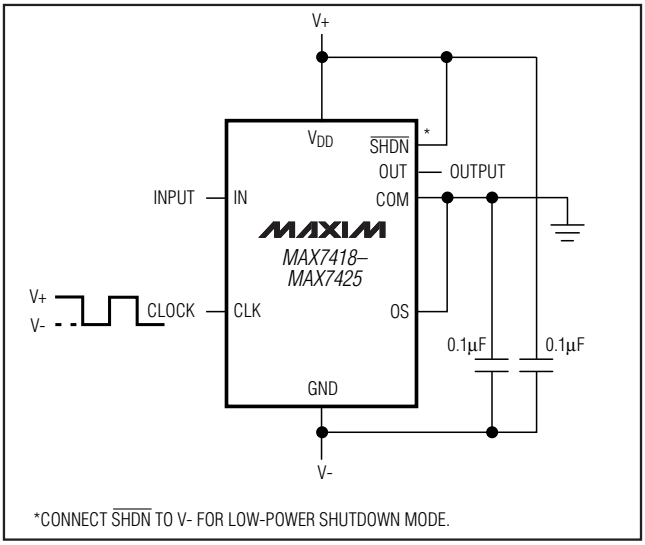


Figure 5. Dual-Supply Operation

Harmonic Distortion

Harmonic distortion arises from nonlinearities within the filter. These nonlinearities generate harmonics when a pure sine wave is applied to the filter input. Tables 1, 2, and 3 list typical harmonic distortion values with a 10kΩ load at T_A = +25°C.

Table 1. MAX7418/MAX7421/MAX7422/MAX7425 Typical Harmonic Distortion

FILTER	f_{CLK} (MHz)	f_{IN} (kHz)	V_{IN} (Vp-p)	TYPICAL HARMONIC DISTORTION (dB)			
				2nd	3rd	4th	5th
MAX7418	2.2	2	4	<-80	<-80	<-80	<-80
	1.5	2		<-80	<-80	<-80	<-80
MAX7421	2.2	2	4	<-80	<-80	<-80	<-80
	1.5	2		<-80	<-80	<-80	<-80
MAX7422	4.0	4	2	<-80	<-80	<-80	<-80
	2.2	2		<-80	<-80	<-80	<-80
MAX7425	4.0	4	2	<-80	<-80	<-80	<-80
	2.2	2		<-80	<-80	<-80	<-80

Table 2. MAX7420/MAX7424 Typical Harmonic Distortion

FILTER	f_{CLK} (MHz)	f_{IN} (kHz)	V_{IN} (Vp-p)	TYPICAL HARMONIC DISTORTION (dB)			
				2nd	3rd	4th	5th
MAX7420	2.2	2	4	-77	-67	< -80	-76
	1.5	2		< -80	-70	< -80	< -80
MAX7424	3.5	3	2	< -80	-70	< -80	< -80
	2.2	2		< -80	-77	< -80	< -80

Table 3. MAX7419/MAX7423 Typical Harmonic Distortion

FILTER	f_{CLK} (MHz)	f_{IN} (kHz)	V_{IN} (Vp-p)	TYPICAL HARMONIC DISTORTION (dB)			
				2nd	3rd	4th	5th
MAX7419	2.2	2	4	< -80	-77	< -80	< -80
	1.5	2		< -80	-80	< -80	< -80
MAX7423	3.5	3	2	< -80	-75	< -80	< -80
	2.2	2		< -80	< -80	< -80	< -80

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX7422CUA	0°C to +70°C	8 µMAX
MAX7422EUA	-40°C to +85°C	8 µMAX
MAX7423CUA	0°C to +70°C	8 µMAX
MAX7423EUA	-40°C to +85°C	8 µMAX
MAX7424CUA	0°C to +70°C	8 µMAX
MAX7424EUA	-40°C to +85°C	8 µMAX
MAX7425CUA	0°C to +70°C	8 µMAX
MAX7425EUA	-40°C to +85°C	8 µMAX

Selector Guide (continued)

PART	FILTER RESPONSE	OPERATING VOLTAGE (V)
MAX7422	r = 1.6	+3
MAX7423	Bessel	+3
MAX7424	Butterworth	+3
MAX7425	r = 1.25	+3

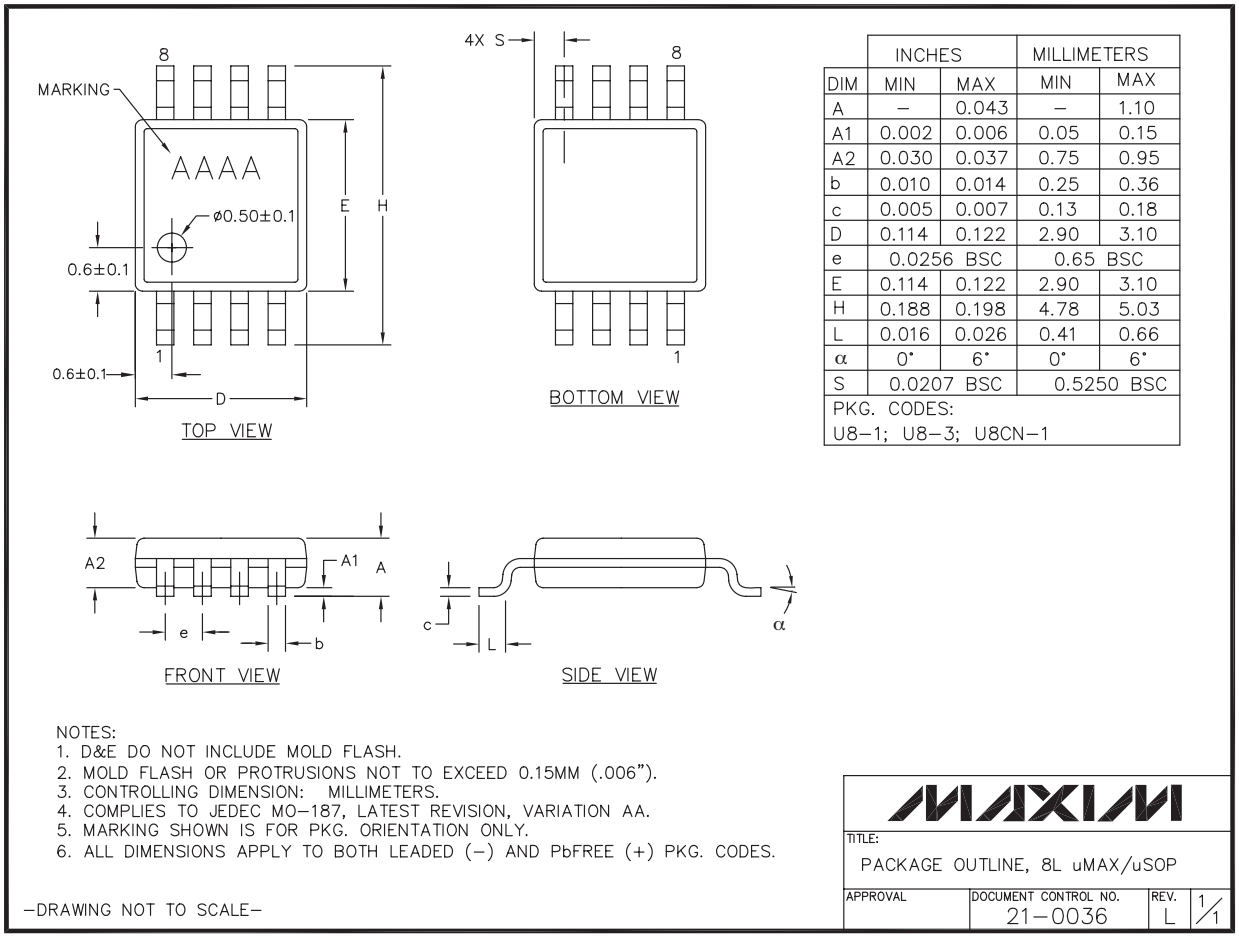
Chip Information

TRANSISTOR COUNT: 1457

PROCESS: BiCMOS

5th-Order, Lowpass, Switched-Capacitor Filters

Package Information



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	–	0.043	–	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.114	0.122	2.90	3.10
e	0.0256 BSC		0.65 BSC	
E	0.114	0.122	2.90	3.10
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	

PKG. CODES:
U8–1; U8–3; U8CN–1

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COMPLIES TO JEDEC MO–187, LATEST REVISION, VARIATION AA.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (–) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–

MAXIM

TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21–0036	L	1/1