12-Bit Low-Power, 2-Wire, Serial Voltage-Output DAC

ABSOLUTE MAXIMUM RATINGS

V_{DD}, SCL, SDA to GND .....-0.3V to +6V
OUT, ADD to GND .....-0.3V to V_{DD} + 0.3V
Maximum Current Into Any Pin 50mA
Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23 (derate 9.1mW above +70°C).....727mW

Operating Temperature Range .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.5V, GND = 0, R_L = 5kΩ, C_L = 200pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY (Note 2)						
Resolution	N		12			Bits
Integral Nonlinearity	INL	(Note 3)		±2	±16	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic (Note 3)			±1	LSB
Zero-Code Error	ZCE	Code = 000 hex, V_{DD} = 2.7V		±6	±40	mV
Zero-Code Error Tempco				2.3		ppm/°C
Gain Error	GE	Code = FFF hex		-0.8	-3	%FS
Gain-Error Tempco				0.26		ppm/°C
DAC OUTPUT						
Output Voltage Range		No load (Note 4)	0		V_{DD}	V
DC Output Impedance		Code = 800 hex		1.2		Ω
Short-Circuit Current		V_{DD} = 5V, V_{OUT} = full scale (short to GND)		42.2		mA
		V_{DD} = 3V, V_{OUT} = full scale (short to GND)		15.1		
Wake-Up Time		V_{DD} = 5V		8		µs
		V_{DD} = 3V		8		
DAC Output Leakage Current		Power-down mode = high impedance, V_{DD} = 5.5V, V_{OUT} = V_{DD} or GND		±0.1	±1	µA
DIGITAL INPUTS (SCL, SDA)						
Input High Voltage	V_{IH}		0.7 × V_{DD}			V
Input Low Voltage	V_{IL}				0.3 × V_{DD}	V
Input Hysteresis			0.05 × V_{DD}			V
Input Leakage Current		Digital inputs = 0 or V_{DD}		±0.1	±1	µA
Input Capacitance				6		pF
DIGITAL OUTPUT (SDA)						
Output Logic Low Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V
Three-State Leakage Current	I_L	Digital inputs = 0 or V_{DD}		±0.1	±1	µA
Three-State Output Capacitance				6		pF
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR			0.5		V/µs
Voltage-Output Settling Time		To 1/2LSB code 400 hex to C00 hex or C00 hex to 400 hex (Note 5)		4	12	µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V, GND = 0, R_L = 5kΩ, C_L = 200pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Feedthrough		Code = 000 hex, digital inputs from 0 to V_{DD}		0.2		nV-s
Digital-to-Analog Glitch Impulse		Major carry transition, code = 7FF hex to 800 hex and 800 hex to 7FF hex		12		nV-s
POWER SUPPLIES						
Supply Voltage Range	V_{DD}		2.7		5.5	V
Supply Current with No Load		All digital inputs at 0 or V_{DD} = 3.6V		100	170	µA
		All digital inputs at 0 or V_{DD} = 5.5V		130	190	
Power-Down Supply Current		All digital inputs at 0 or V_{DD} = 5.5V		0.3	1	µA
TIMING CHARACTERISTICS (Figure 1)						
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Condition Hold Time		$t_{HD, STA}$	0.6			µs
SCL Pulse Width Low	t_{LOW}		1.3			µs
SCL Pulse Width High	t_{HIGH}		0.6			µs
Repeated START Setup Time	$t_{SU, STA}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$		0		0.9	µs
Data Setup Time	$t_{SU, DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_r	(Note 5)	0		300	ns
SDA and SCL Receiving Fall Time	t_f	(Note 5)	0		300	ns
SDA Transmitting Fall Time	t_f	(Note 5)	$20 + 0.1C_b$		250	ns
STOP Condition Setup Time	t_{SU-STO}		0.6			µs
Bus Capacitance	C_b	(Note 5)			400	pF
Maximum Duration of Suppressed Pulse Widths	t_{SP}		0		50	ns

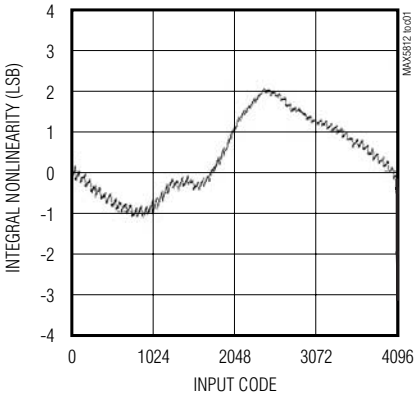
Note 1: All devices are 100% production tested at T_A = +25°C and are guaranteed by design for T_A = T_{MIN} to T_{MAX}.
Note 2: Static specifications are tested with the output unloaded.
Note 3: Linearity is guaranteed from codes 115 to 3981.
Note 4: Offset and gain error limit the FSR.
Note 5: Guaranteed by design. Not production tested.

12-Bit Low-Power, 2-Wire, Serial Voltage-Output DAC

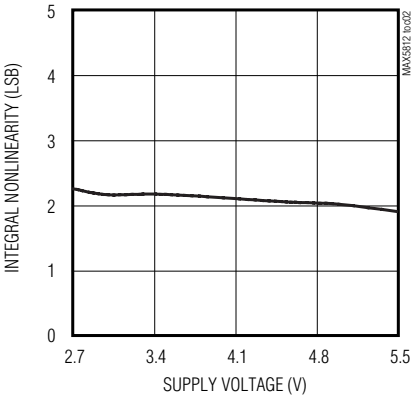
Typical Operating Characteristics

(V_{DD} = +5V, R_L = 5kΩ, T_A = +25°C.)

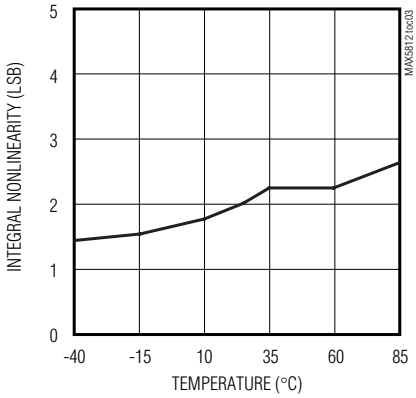
INTEGRAL NONLINEARITY vs. INPUT CODE



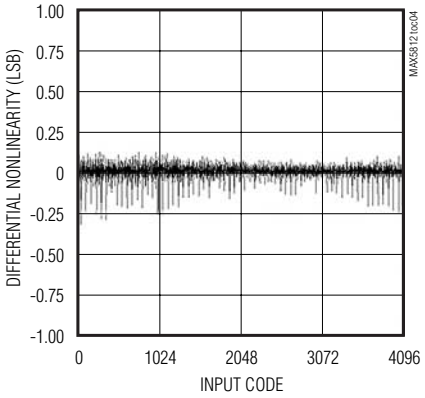
INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



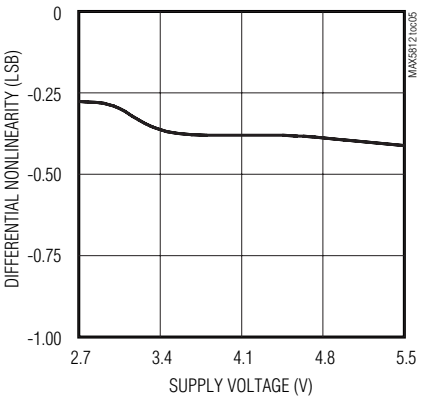
INTEGRAL NONLINEARITY vs. TEMPERATURE



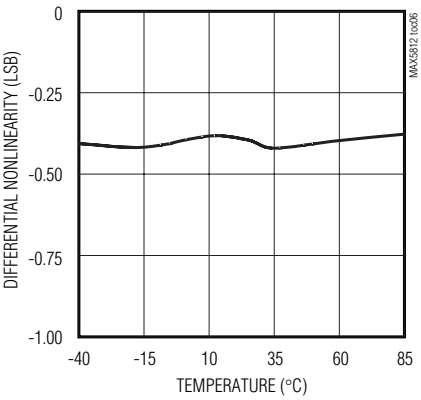
DIFFERENTIAL NONLINEARITY vs. INPUT CODE



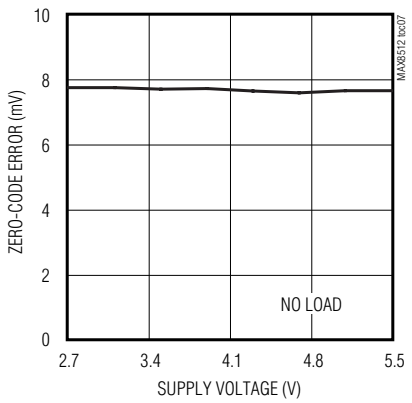
DIFFERENTIAL NONLINEARITY vs. SUPPLY VOLTAGE



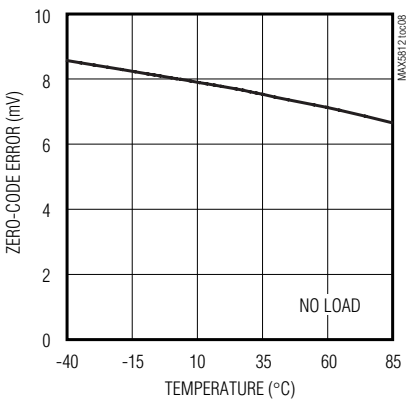
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE



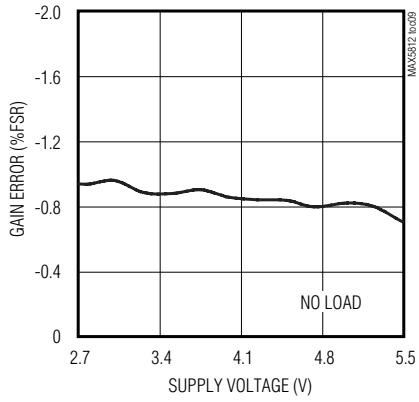
ZERO-CODE ERROR vs. SUPPLY VOLTAGE



ZERO-CODE ERROR vs. TEMPERATURE



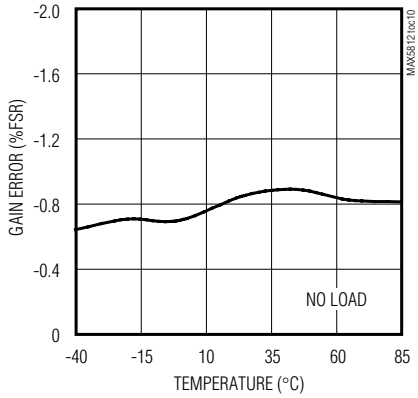
GAIN ERROR vs. SUPPLY VOLTAGE



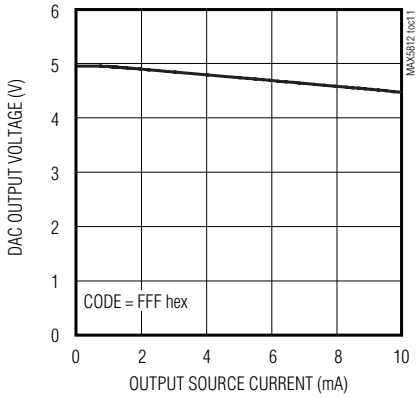
Typical Operating Characteristics (continued)

(V_{DD} = +5V, R_L = 5kΩ, T_A = +25°C.)

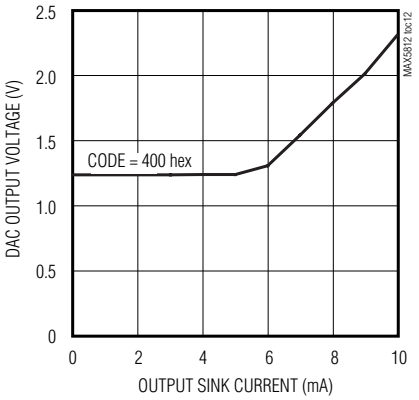
GAIN ERROR vs. TEMPERATURE



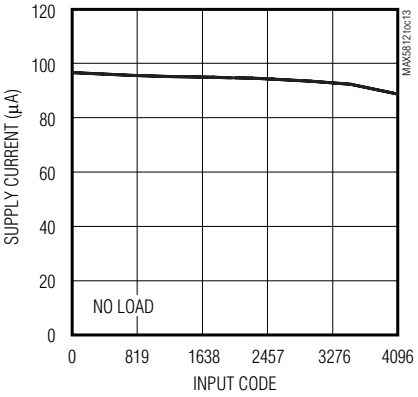
DAC OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT (NOTE 6)



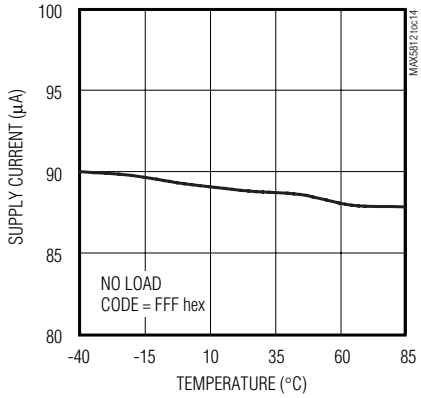
DAC OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT (NOTE 6)



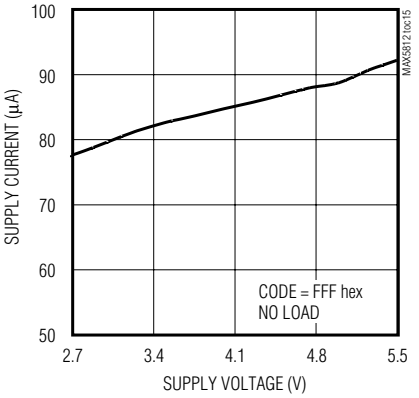
SUPPLY CURRENT vs. INPUT CODE



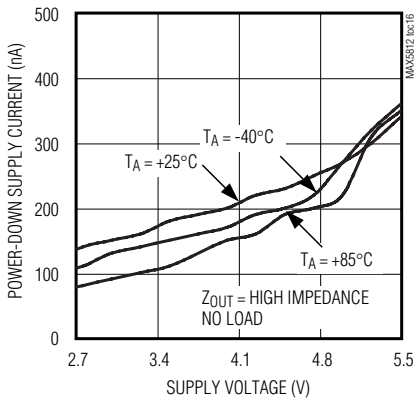
SUPPLY CURRENT vs. TEMPERATURE



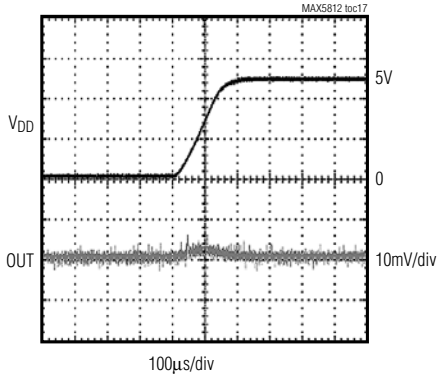
SUPPLY CURRENT vs. SUPPLY VOLTAGE



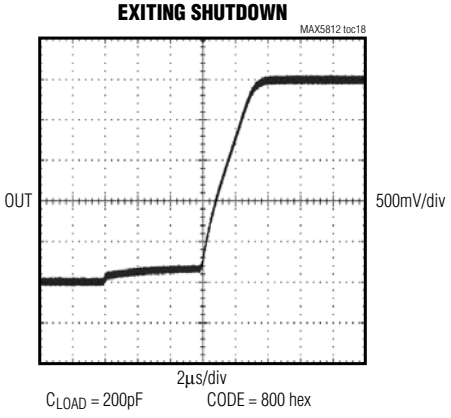
POWER-DOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



POWER-UP GLITCH



EXITING SHUTDOWN



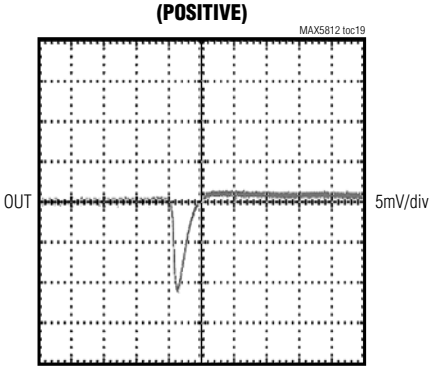
Note 6: The ability to drive loads less than 5kΩ is not implied.

12-Bit Low-Power, 2-Wire, Serial Voltage-Output DAC

Typical Operating Characteristics (continued)

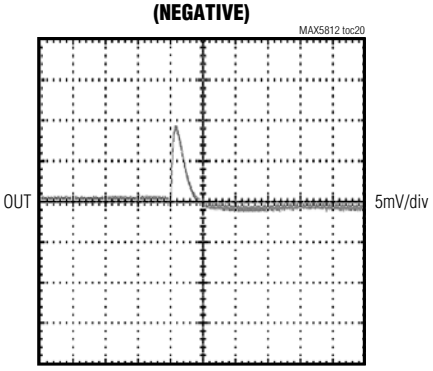
(V_{DD} = +5V, R_L = 5kΩ, T_A = +25°C.)

MAJOR CARRY TRANSITION (POSITIVE)



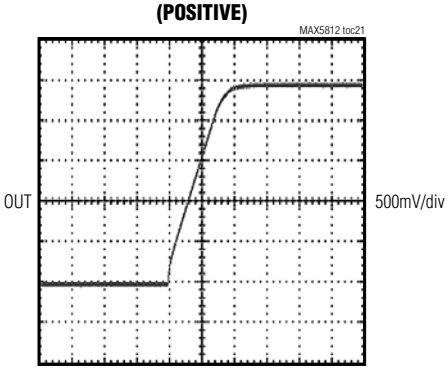
C_{LOAD} = 200pF
R_L = 5kΩ
CODE = 7FF hex TO 800 hex

MAJOR CARRY TRANSITION (NEGATIVE)



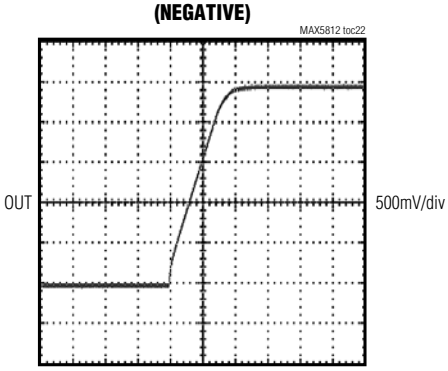
C_{LOAD} = 200pF
R_L = 5kΩ
CODE = 7FF hex TO 800 hex

SETTLING TIME (POSITIVE)



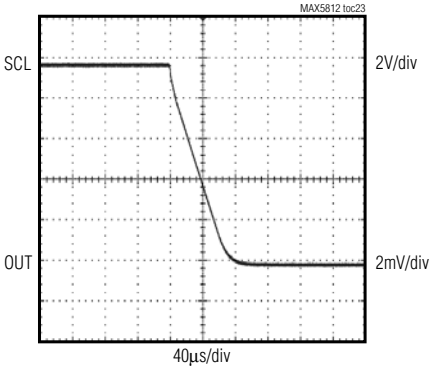
C_{LOAD} = 200pF
CODE = 400 hex to C00 hex

SETTLING TIME (NEGATIVE)



C_{LOAD} = 200pF
CODE = C00 hex to 400 hex

DIGITAL FEEDTHROUGH



C_{LOAD} = 200pF
f_{SCL} = 12kHz
CODE = 000 hex

Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Power Supply and DAC Reference Input
2	GND	Ground
3	SDA	Bidirectional Serial Data I/O
4	SCL	Serial Clock Line
5	ADD	Address Select. A logic high sets the address LSB to 1; a logic low sets the address LSB to 0.
6	OUT	Analog Output

Detailed Description

The MAX5812 is a 12-bit, voltage-output DAC with an I²C/SMBus-compatible 2-wire interface. The device consists of a serial interface, power-down circuitry, input and DAC registers, a 12-bit resistor string DAC, unity-gain output buffer, and output resistor network. The serial interface decodes the address and control bits, routing the data to either the input or DAC register. Data can be directly written to the DAC register immediately updating the device output, or can be written to the input register without changing the DAC output. Both registers retain data as long as the device is powered.

DAC Operation

The MAX5812 uses a segmented resistor string DAC architecture, which saves power in the overall system and guarantees output monotonicity. The MAX5812's input coding is straight binary with the output voltage given by the following equation:

$$V_{OUT} = \frac{V_{REF} \times (D)}{2^N}$$

where N = 12(bits), and D = the decimal value of the input code (0 to 4095).

Output Buffer

The MAX5812 analog output is buffered by a precision unity-gain follower that slews 0.5V/µs. The buffer output swings rail-to-rail and is capable of driving 5kΩ in parallel with 200pF. The output settles to ±0.5LSB within 4µs.

Power-On Reset

The MAX5812 features an internal power-on-reset (POR) circuit that initializes the device upon power-up. The DAC registers are set to zero-scale and the device is powered down with the output buffer disabled and the output pulled to GND through the 100kΩ termination resistor. Following power-up, a wake-up command must be initiated before conversions are performed.

Power-Down Modes

The MAX5812 has three software-controlled, low-power, power-down modes. All three modes disable the output buffer and disconnect the DAC resistor string from V_{DD}, reducing supply current draw to 300nA. In power-down mode 0, the device output is high impedance. In power-down mode 1, the device output is internally pulled to GND by a 1kΩ termination resistor. In power-down mode 2, the device output is internally pulled to GND by a 100kΩ termination resistor. Table 1 shows the power-down mode command words.

Upon wake-up, the DAC output is restored to its previous value. Data is retained in the input and DAC registers during power-down mode.

Digital Interface

The MAX5812 features an I²C/SMBus-compatible 2-wire interface consisting of a serial data line (SDA)

Table 1. Power-Down Command Bits

POWER-DOWN COMMAND BITS		MODE/FUNCTION
PD1	PD0	
0	0	Power-up device. DAC output restored to previous value.
0	1	Power-down mode 0. Powers down device with output floating.
1	0	Power-down mode 1. Powers down device with output terminated with 1kΩ to GND.
1	1	Power-down mode 2. Powers down device with output terminated with 100kΩ to GND.

12-Bit Low-Power, 2-Wire, Serial Voltage-Output DAC

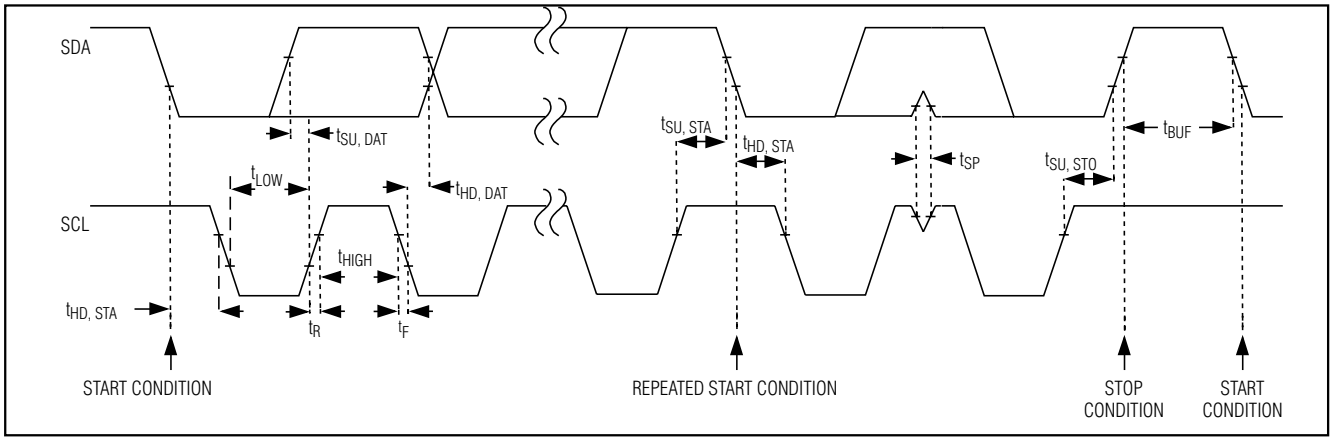


Figure 1. Two-Wire Serial Interface Timing Diagram

and a serial clock line (SCL). The MAX5812 is SMBus compatible within the range of V_{DD} = 2.7V to 3.6V. SDA and SCL facilitate bidirectional communication between the MAX5812 and the master at rates up to 400kHz. Figure 1 shows the 2-wire interface timing diagram. The MAX5812 is a transmit/receive slave-only device, relying upon a master to generate a clock signal. The master, typically a microcontroller, initiates data transfer on the bus and generates SCL to permit that transfer.

A master device communicates to the MAX5812 by transmitting the proper address followed by command and/or data words. Each transmit sequence is framed by a START (S) or REPEATED START (S_r) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX5812 SDA and SCL drivers are open-drain outputs, requiring a pullup resistor (500Ω or greater) to generate a logic high voltage (see the *Typical Operating Circuit*). Series resistors R_S are optional. These series resistors protect the input stages of the MAX5812 from high-voltage spikes on the bus lines and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while the SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

START and STOP Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-

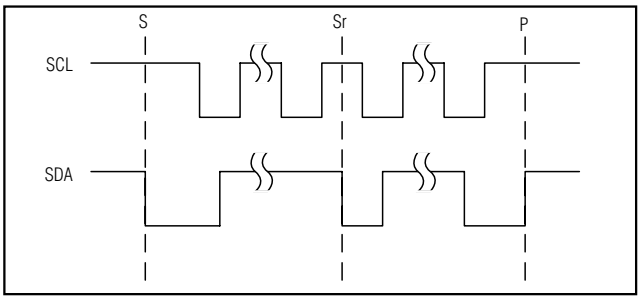


Figure 2. START/STOP Conditions

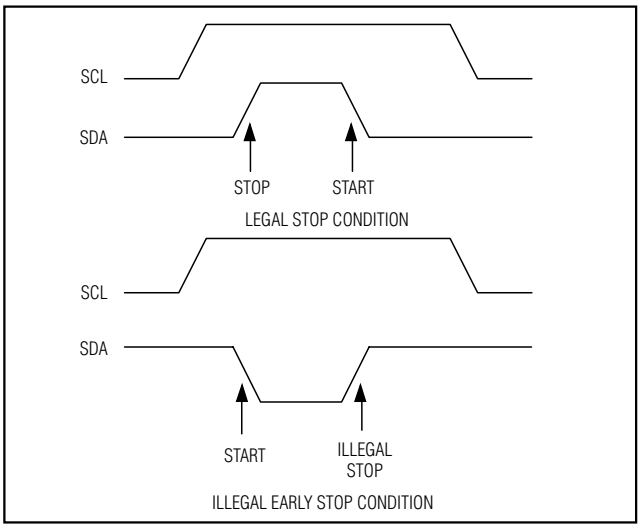


Figure 3. Early STOP condition

low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 2). A START condition from the master signals the beginning of a transmission to the MAX5812. The master terminates transmission by issuing a not acknowledge followed by a STOP condition (see the *Acknowledge Bit* section). The STOP condition frees the bus. If a repeated START condition (S_r) is generated instead of a STOP condition, the bus remains active. When a STOP condition or incorrect address is detected, the MAX5812 internally disconnects SCL from the serial interface until the next START condition, minimizing digital noise and feedthrough.

Early STOP Conditions

The MAX5812 recognizes a STOP condition at any point during transmission except when a START condition occurs in the same high pulse as a START condition (Figure 3). This condition is not a legal I²C format, at least one clock pulse must separate any START and STOP conditions.

Repeated START Conditions

A repeated start (S_r) condition might indicate a change of data direction on the bus. Such a change occurs when a command word is required to initiate a read operation. S_r also can be used when the bus master is writing to several I²C devices and does not want to relinquish control of the bus. The MAX5812 serial interface supports continuous write operations with or without an S_r condition separating them. Continuous read operations require S_r conditions because of the change in direction of data flow.

Acknowledge Bit (ACK)

The acknowledge bit (ACK) is the ninth bit attached to any 8-bit data word. ACK is always generated by the receiving device. The MAX5812 generates an ACK when receiving an address or data by pulling SDA low during the ninth clock period. When transmitting data, the MAX5812 waits for the receiving device to generate an ACK. Monitoring ACK allows detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by the 7-bit slave address (Figure 4). When idle, the MAX5812 waits for a START condition followed by its slave address. The serial interface compares each address value bit-by-bit, allowing the interface to power-down immediately when an incorrect address is detected. The LSB of the address word is the Read/Write (R/$\overline{W}$) bit. R/$\overline{W}$ indicates whether the master is writing to or reading from the MAX5812 (R/$\overline{W}$ = 0 selects the write condition, R/$\overline{W}$ = 1 selects the read condition). After receiving the proper address, the MAX5812 issues an ACK by pulling SDA low for one clock cycle.

The MAX5812 has eight factory/user-programmed addresses (Table 2). Address bits A6 through A1 are preset; A0 is controlled by ADD. Connecting ADD to GND sets A0 = 0. Connecting ADD to V_{DD} sets A0 = 1. This feature allows up to eight MAX5812s to share a bus.

Table 2. MAX5812 I²C Slave Addresses

PART	V_{ADD}	DEVICE ADDRESS (A_6...A_0)
MAX5812L	GND	0010 000
MAX5812L	V_{DD}	0010 001
MAX5812M	GND	0010 010
MAX5812M	V_{DD}	0010 011
MAX5812N	GND	0110 100
MAX5812N	V_{DD}	0110 101
MAX5812P	GND	1010 100
MAX5812P	V_{DD}	1010 101

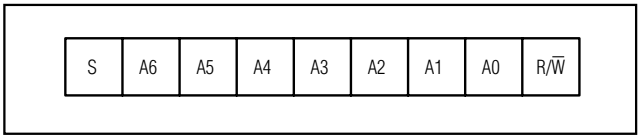


Figure 4. Slave Address Byte Definition

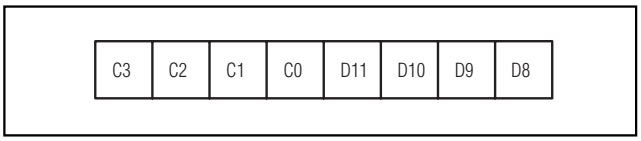


Figure 5. Command Byte Definition

Write Data Format

In write mode (R/$\overline{W}$ = 0), data that follows the address byte controls the MAX5812 (Figure 5). Bits C3–C0 configure the MAX5812 (Table 3). Bits D11–D0 are DAC data. Input and DAC registers update on the falling edge of SCL during the acknowledge bit. Should the write cycle be prematurely aborted, data will not be updated and the write cycle must be repeated. Figure 6 shows two example write data sequences.

12-Bit Low-Power, 2-Wire, Serial Voltage-Output DAC

Table 3. Command Byte Definitions

SERIAL DATA INPUT							FUNCTION
C3	C2	C1	C0	D11/PD1*	D10/PD0*	D9–D8	
1	1	0	0	DAC DATA	DAC DATA	DAC DATA	Load DAC with a new data from the following data byte and update DAC output simultaneously as soon as data is available from the serial bus. The DAC and input registers are updated with the new data.
1	1	0	1	DAC DATA	DAC DATA	DAC DATA	Load input register with the data from the following data byte. DAC output remains unchanged.
1	1	1	0	DAC DATA	DAC DATA	DAC DATA	Load input register with data from the following data byte. Update DAC output to the previously stored data.
1	1	1	1	X	X	XX	Update DAC output from input register. The device will ignore any new data.
1	0	X	X	X	X	XX	Read data request. Data bits are ignored. The contents of the DAC register are available on the bus.
0	1	X	X	0	0	XX	Powers up device.
0	1	X	X	0	1	XX	Power-down mode 0. Powers down device with output floating.
0	1	X	X	1	0	XX	Power-down mode 1. Powers down device with output terminated with 1kΩ to GND.
0	1	X	X	1	1	XX	Power-down mode 2. Powers down device with output terminated with 100kΩ to GND.

**When C3 = 0 and C2 = 1, data bits D11 and D10 write to the power-down registers (PD1 and PD0).*
X = Don't care.

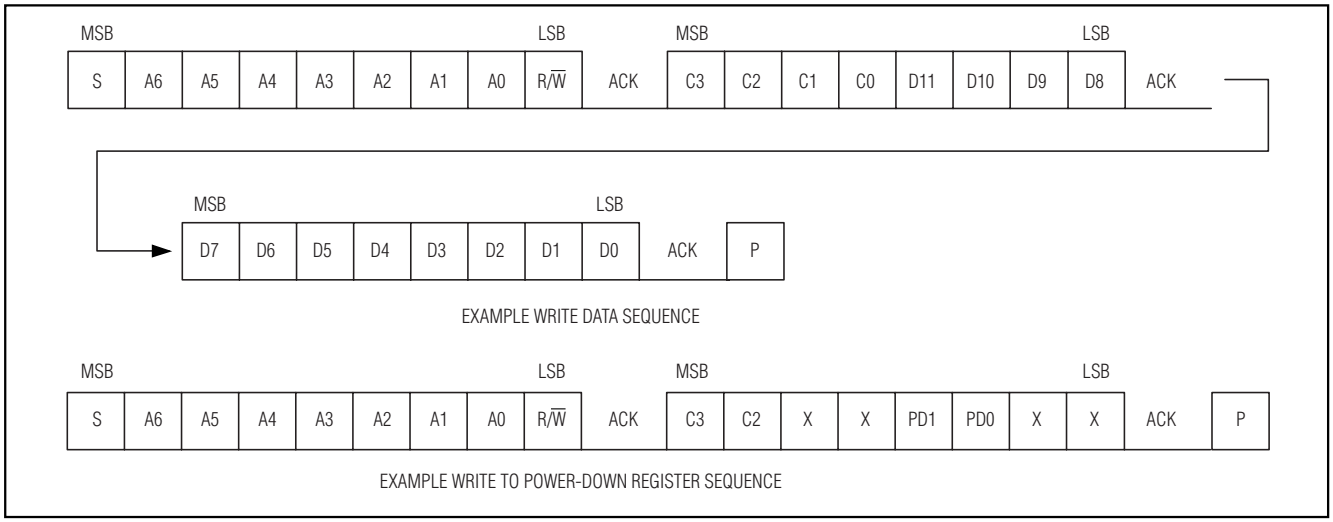


Figure 6. Example Write Command Sequences

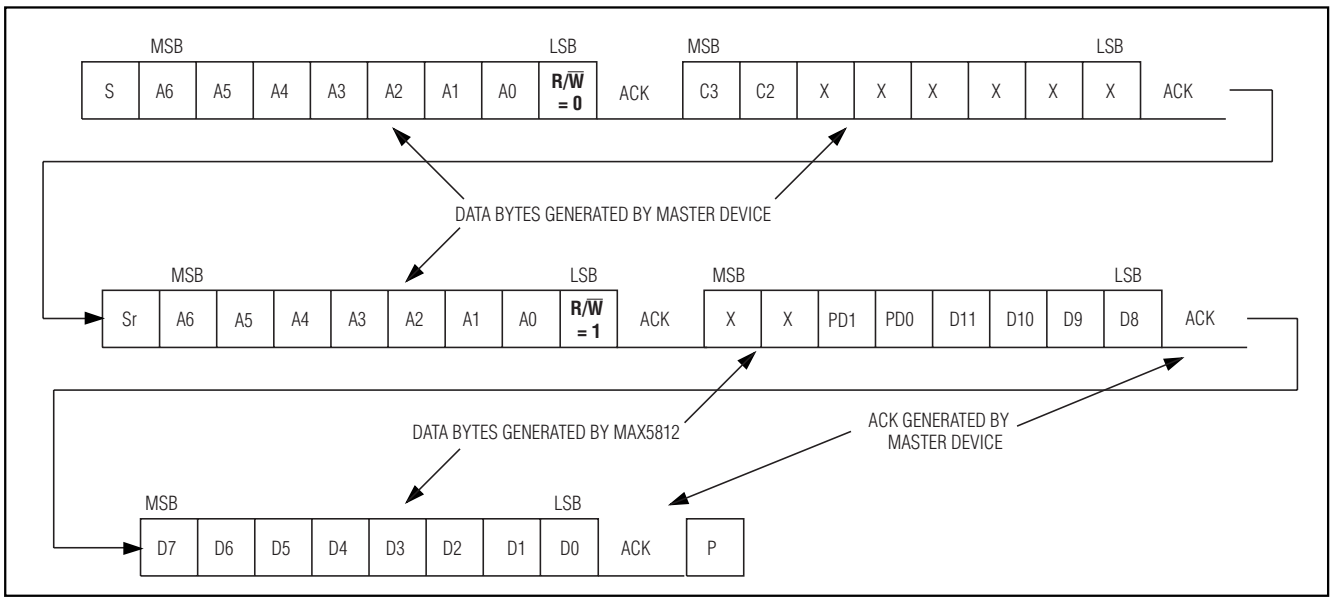


Figure 7. Example Read Word Data Sequence

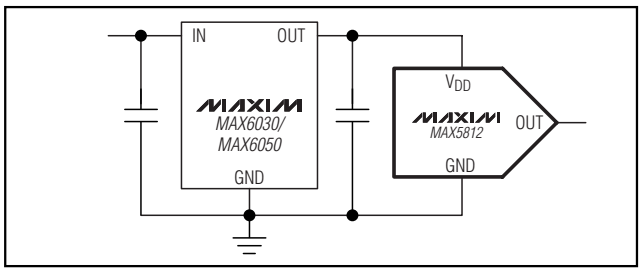


Figure 8. Powering the MAX5812 from An External Reference

Read Data Format

In read mode (R/$\overline{W}$ = 1), the MAX5812 writes the contents of the DAC register to the bus. The direction of data flow reverses after the address acknowledge by the MAX5812. The device transmits the first byte of data, waits for the master to acknowledge, and then transmits the second byte. Figure 7 shows an example-read data sequence.

I²C Compatibility

The MAX5812 is compatible with existing I²C systems. SCL and SDA are high-impedance inputs; SDA has an open drain that pulls the data line low during the ninth clock pulse. The *Typical Operating Circuit* shows a typical I²C application. The communication protocol supports standard I²C 8-bit communications. The general call address is ignored. The MAX5812 address is compatible only with the 7-bit I²C addressing protocol. Ten-bit address formats are not supported.

Digital Feedthrough Suppression

When the MAX5812 detects an address mismatch, the serial interface disconnects the SCL signal from the core circuitry. This minimizes digital feedthrough caused by the SCL signal on a static output. The serial interface reconnects the SCL signal when a valid START condition is detected.

Applications Information

Powering the Device From an External Reference

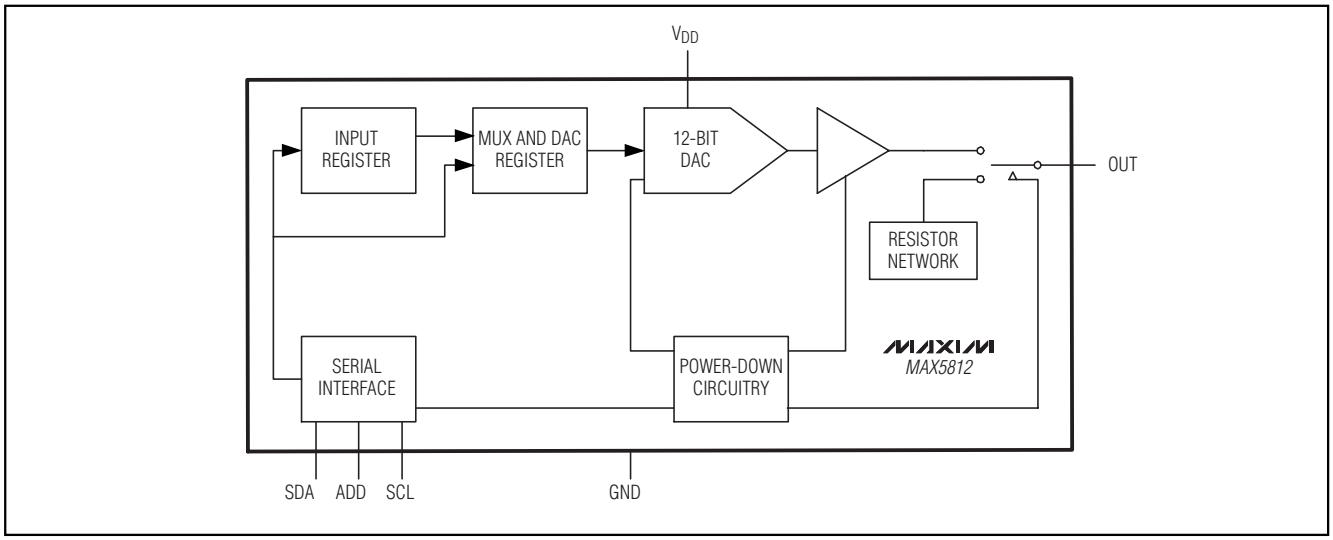
The MAX5812 uses the V_{DD} as the DAC voltage reference. Any power-supply noise is directly coupled to the device output. The circuit in Figure 8 uses a precision voltage reference to power the MAX5812, isolating the device from any power-supply noise. Powering the MAX5812 in such a manner greatly improves overall performance, especially in noisy systems. The MAX6030 (3V, 75ppm/°C) or the MAX6050 (5V, 75ppm/°C) precision voltage references are ideal choices because of the low power requirements of the MAX5812.

Digital Inputs and Interface Logic

The MAX5812 2-wire digital interface is I²C and SMBus-compatible. The two digital inputs (SCL and SDA) load

12-Bit Low-Power, 2-Wire, Serial Voltage-Output DAC

Functional Diagram



the digital input serially into the DAC. Schmitt-trigger buffered inputs allow slow transition interfaces such as optocouplers to interface directly to the device. The digital inputs are compatible with CMOS logic levels.

Power-Supply Bypassing and Ground Management

Careful PC board layout is important for optimal system performance. Keep analog and digital signals separate to reduce noise injection and digital feedthrough. Use a ground plane to ensure that the ground return from GND to the power supply ground is short and low impedance. Bypass V_{DD} with a 0.1µF capacitor to ground as close to the device as possible.

Selector Guide

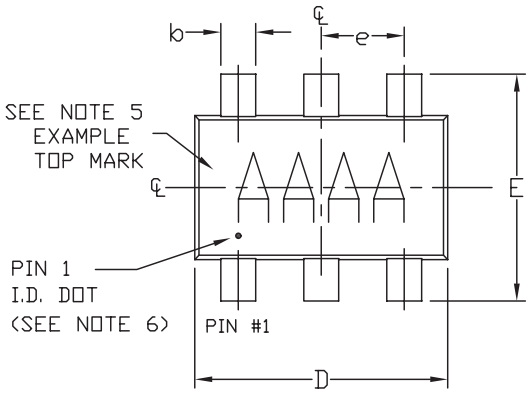
PART	ADDRESS
MAX5812LEUT	0010 00X
MAX5812MEUT	0010 01X
MAX5812NEUT	0110 10X
MAX5812PEUT	1010 10X

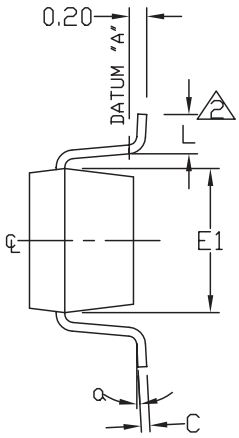
Chip Information

TRANSISTOR COUNT: 7172

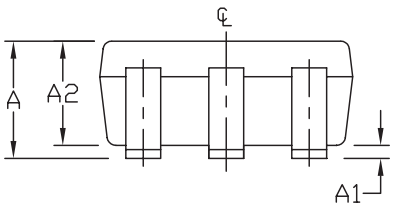
PROCESS: BiCMOS

Package Information





SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
α	0°	10°



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178.

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, SOT-23, 6L

APPROVAL	DOCUMENT CONTROL NO.	REV	
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