ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND.....-0.3V to +6V
V_{DD} to DGND.....-0.3V to +6V
AGND to DGND.....±0.3V
FBA, FBB to AGND.....-0.3V to (V_{DD} + 0.3V)
REF_, OUT_ to AGND.....-0.3V to (V_{DD} + 0.3V)
Digital Inputs (SCLK, DIN, $\overline{CS}$, $\overline{CL}$, $\overline{PDL}$) to DGND.....-0.3V to +6V
Digital Outputs (DOUT, UPO) to DGND.....-0.3V to (V_{DD} + 0.3V)
Maximum Current into Any Pin.....±20mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.5mW/°C above +70°C).....593mW
QSOP (derate 8.30mW/°C above +70°C).....667mW
CERDIP (derate 10.00mW/°C above +70°C).....800mW
Operating Temperature Ranges
MAX5152_C_E/MAX5153_C_E.....0°C to +70°C
MAX5152_E_E/MAX5153_E_E.....-40°C to +85°C
MAX5152_MJE/MAX5153_MJE.....-55°C to +125°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX5152

(V_{DD} = +5V ±10%, V_{REFA} = V_{REFB} = 2.5V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			13			Bits
Integral Nonlinearity	INL	(Note 1)	MAX5152A			±1/2	LSB
			MAX5152B			±1	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Offset Error	V_{OS}	Code = 20				±6	mV
Offset Tempco	TCV_{OS}	Normalized to 2.5V			3		ppm/°C
Gain Error					-0.5	±6	LSB
Gain-Error Tempco		Normalized to 2.5V			3		ppm/°C
V_{DD} Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V			20	200	µV/V
REFERENCE INPUT							
Reference Input Range	REF			0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Minimum with code 1555 hex		14	20		kΩ
MULTIPLYING-MODE PERFORMANCE							
Reference 3dB Bandwidth		Input code = 1FFF hex, V_{REF} = 0.67Vp-p at 2.5V_{DC}			600		kHz
Reference Feedthrough		Input code = 0000 hex, V_{REF} = (V_{DD} - 1.4Vp-p) at 1kHz			-85		dB
Signal-to-Noise plus Distortion Ratio	SINAD	Input code = 1FFF hex, V_{REF} = 1Vp-p at 2.5V_{DC}, f = 25kHz			82		dB
DIGITAL INPUTS							
Input High Voltage	V_{IH}	$\overline{CL}$, $\overline{PDL}$, $\overline{CS}$, DIN, SCLK		3.0			V
Input Low Voltage	V_{IL}	$\overline{CL}$, $\overline{PDL}$, $\overline{CS}$, DIN, SCLK				0.8	V
Input Hysteresis	V_{HYS}				200		mV
Input Leakage Current	I_{IN}	V_{IN} = 0V to V_{DD}			0.001	±1	µA
Input Capacitance	C_{IN}				8		pF

ELECTRICAL CHARACTERISTICS—MAX5152 (continued)

(V_{DD} = +5V ±10%, V_{REFA} = V_{REFB} = 2.5V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS (DOUT, UPO)						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA		0.13	0.40	V
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.75		V/µs
Output Settling Time		To 1/2LSB of full-scale, V_{STEP} = 2.5V		20		µs
Output Voltage Swing		Rail-to-rail (Note 2)		0 to V_{DD}		V
Current into FBA or FBB	$I_{FB\_}$			0	±0.1	µA
Time Required to Exit Shutdown				25		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, f_{DIN} = 100kHz, V_{SCLK} = 5Vp-p		5		nV-s
Digital Crosstalk				5		nV-s
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}		4.5		5.5	V
Power-Supply Current	I_{DD}	(Note 3)		0.5	0.65	mA
Power-Supply Current in Shutdown	$I_{DD(SHDN)}$	(Note 3)		2	10	µA
Reference Current in Shutdown					±1	µA
TIMING CHARACTERISTICS						
SCLK Clock Period	t_{CP}	(Note 4)	100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CHS}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay	t_{DO1}	C_{LOAD} = 200pF			80	ns
SCLK Fall to DOUT Valid Propagation Delay	t_{DO2}	C_{LOAD} = 200pF			80	ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns
$\overline{CS}$ Rise to SCLK Rise Hold	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Note 1: Accuracy is specified from code 20 to code 8191.

Note 2: Accuracy is better than 1LSB for V_{OUT} greater than 6mV and less than V_{DD} - 50mV. Guaranteed by PSRR test at the end points.

Note 3: Digital inputs are set to either V_{DD} or DGND, code = 0000 hex, R_L = ∞

Note 4: SCLK minimum clock period includes rise and fall times.

ELECTRICAL CHARACTERISTICS—MAX5153

(V_{DD} = +2.7V to +3.6V, V_{REFA} = V_{REFB} = 1.25V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			13			Bits
Integral Nonlinearity	INL	(Note 5)	MAX5153A			±1	LSB
			MAX5153B			±2	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Offset Error	V_{OS}	Code = 40				±6	mV
Offset Tempco	TCV_{OS}	Normalized to 1.25V			6		ppm/°C
Gain Error					-0.5	±8	LSB
Gain-Error Tempco		Normalized to 1.25V			6		ppm/°C
V_{DD} Power-Supply Rejection Ratio	PSRR	2.7V ≤ V_{DD} ≤ 3.6V			20	320	µV/V
REFERENCE INPUT (V_{REF})							
Reference Input Range	REF			0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Minimum with code 1555 hex		14			kΩ
MULTIPLYING-MODE PERFORMANCE							
Reference 3dB Bandwidth		Input code = 1FFF hex, $V_{REF(AC)}$ = 0.67Vp-p at 1.25V_{DC}			600		kHz
Reference Feedthrough		Input code = 0000 hex, V_{REF} = (V_{DD} - 1.4V) at 1kHz			-92		dB
Signal-to-Noise plus Distortion Ratio	SINAD	Input code = 1FFF hex, V_{REF} = 1Vp-p at 1.25V_{DC}, f = 15kHz			73		dB
DIGITAL INPUTS							
Input High Voltage	V_{IH}	$\overline{CL}$, $\overline{PDL}$, $\overline{CS}$, DIN, SCLK		2.2			V
Input Low Voltage	V_{IL}	$\overline{CL}$, $\overline{PDL}$, $\overline{CS}$, DIN, SCLK				0.8	V
Input Hysteresis	V_{HYS}				200		mV
Input Leakage Current	I_{IN}	V_{IN} = 0V to V_{DD}			0	±0.1	µA
Input Capacitance	C_{IN}				8		pF
DIGITAL OUTPUTS (DOUT, UPO)							
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA		V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA			0.13	0.4	V

ELECTRICAL CHARACTERISTICS—MAX5153 (continued)

(V_{DD} = +2.7V to +3.6V, V_{REFA} = V_{REFB} = 1.25V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.75		V/µs
Output Settling Time		To 1/2LSB of full-scale, V_{STEP} = 1.25V		25		µs
Output Voltage Swing		Rail-to-rail (Note 6)		0 to V_{DD}		V
Current into FBA or FBB	$I_{FB\_}$			0	±0.1	µA
Time Required to Exit Shutdown				25		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, f_{DIN} = 100kHz, V_{SCLK} = 3Vp-p		5		nV-s
Digital Crosstalk				5		nV-s
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}		2.7		3.6	V
Power-Supply Current	I_{DD}	(Note 7)		0.5	0.6	mA
Power-Supply Current in Shutdown	$I_{DD(SHDN)}$	(Note 7)		1	8	µA
Reference Current in Shutdown					±1	µA
TIMING CHARACTERISTICS						
SCLK Clock Period	t_{CP}	(Note 4)	100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CHS}		0			ns
DIN Setup Time	t_{DS}		50			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay	t_{DO1}	C_{LOAD} = 200pF			120	ns
SCLK Fall to DOUT Valid Propagation Delay	t_{DO2}	C_{LOAD} = 200pF			120	ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns
$\overline{CS}$ Rise to SCLK Rise Hold	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Note 4: SCLK minimum clock period includes rise and fall times.
Note 5: Accuracy is specified from code 40 to code 8191.
Note 6: Accuracy is better than 1LSB for V_{OUT} greater than 6mV and less than V_{DD} - 100mV. Guaranteed by PSRR test at the end points.
Note 7: Digital inputs are set to either V_{DD} or DGND, code = 0000 hex, R_L = ∞

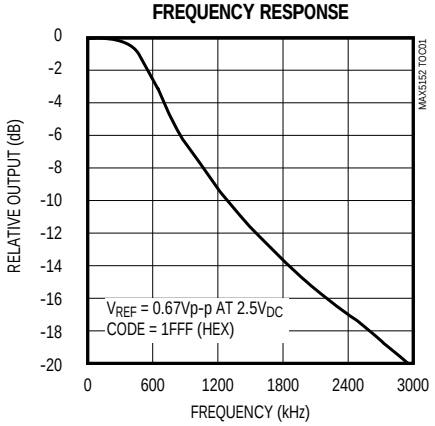
Low-Power, Dual, 13-Bit Voltage-Output DACs with Configurable Outputs

Typical Operating Characteristics

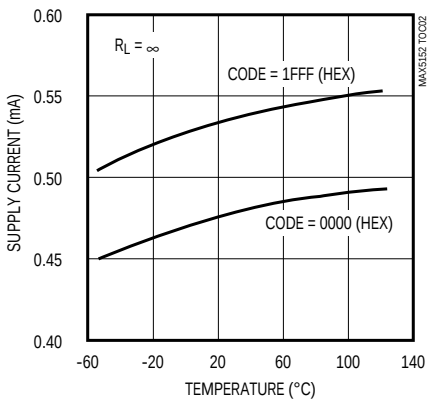
(V_{DD} = +5V, R_L = 10kΩ, C_L = 100pF, FB_ tied to OUT_, T_A = +25°C, unless otherwise noted.)

MAX5152

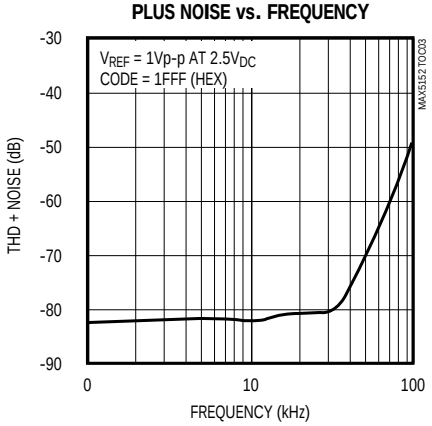
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



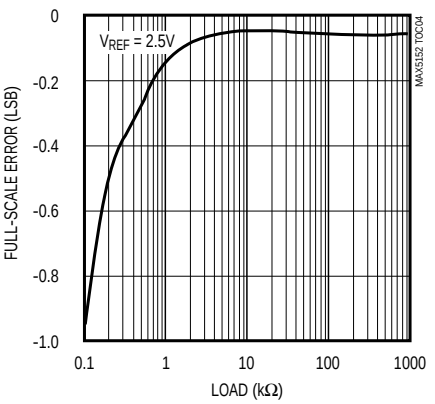
SUPPLY CURRENT vs. TEMPERATURE



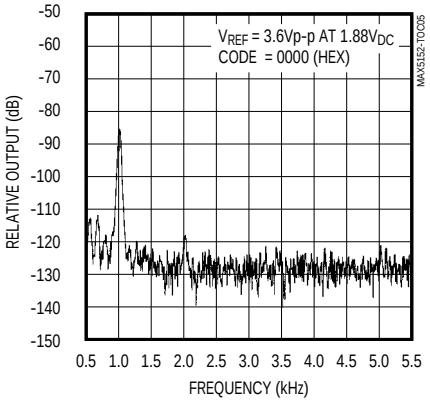
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



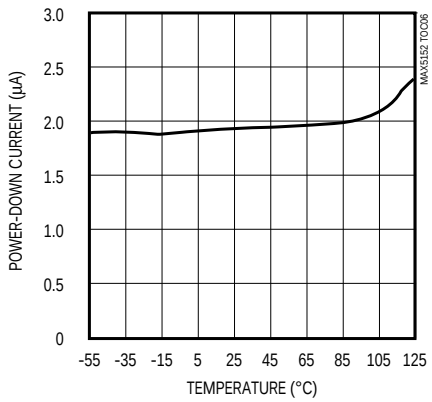
FULL-SCALE ERROR vs. LOAD



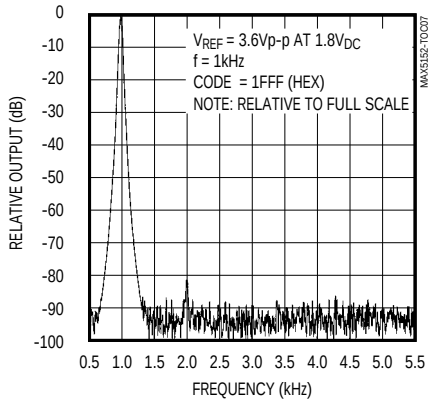
REFERENCE FEEDTHROUGH AT 1kHz



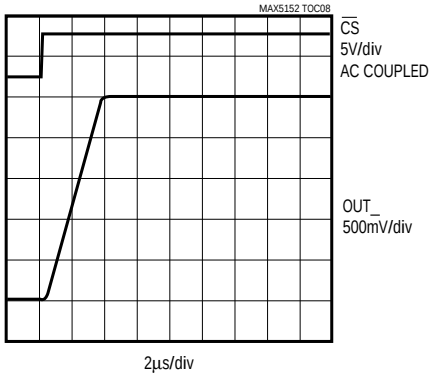
POWER-DOWN CURRENT vs. TEMPERATURE



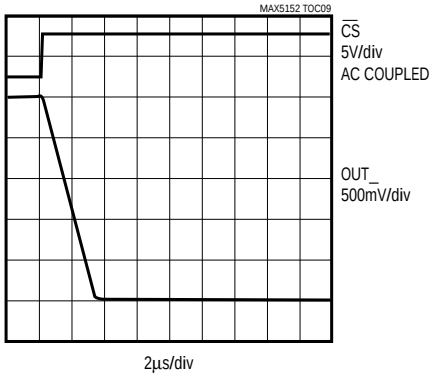
OUTPUT FFT PLOT



DYNAMIC-RESPONSE RISE TIME



DYNAMIC-RESPONSE FALL TIME

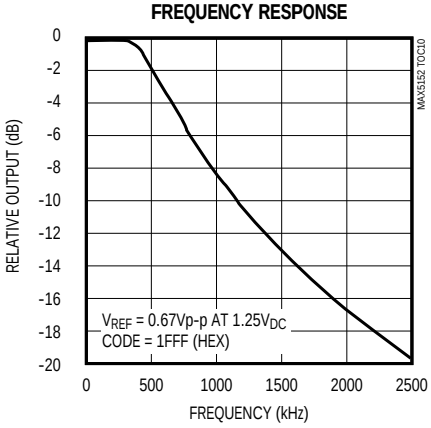


Typical Operating Characteristics (continued)

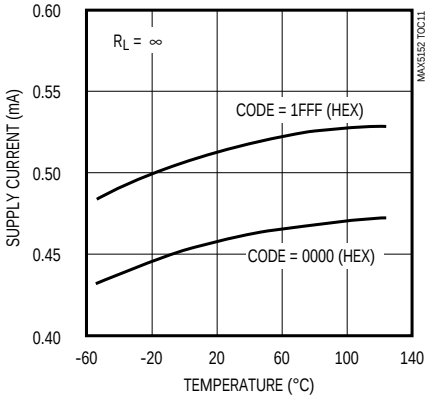
(V_{DD} = +3V, R_L = 10kΩ, C_L = 100pF, FB_ tied to OUT_, T_A = +25°C, unless otherwise noted.)

MAX5153

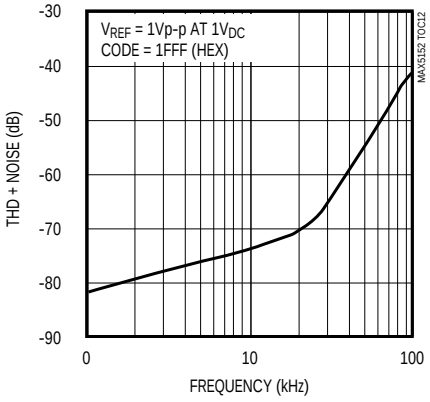
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



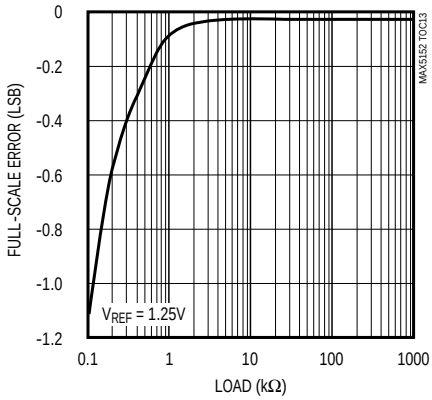
SUPPLY CURRENT vs. TEMPERATURE



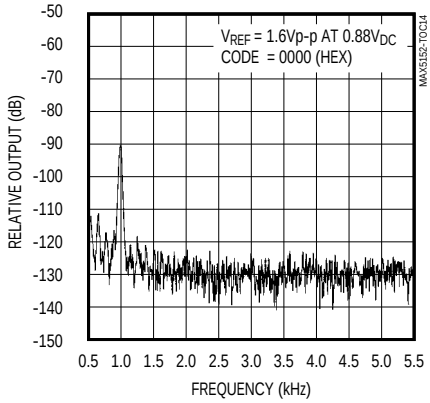
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



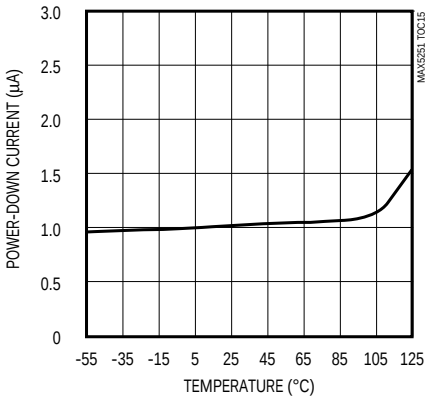
FULL-SCALE ERROR vs. LOAD



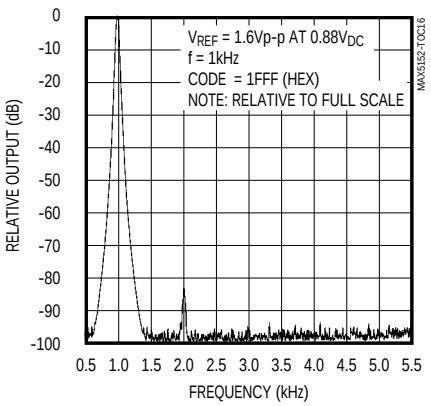
REFERENCE FEEDTHROUGH AT 1kHz



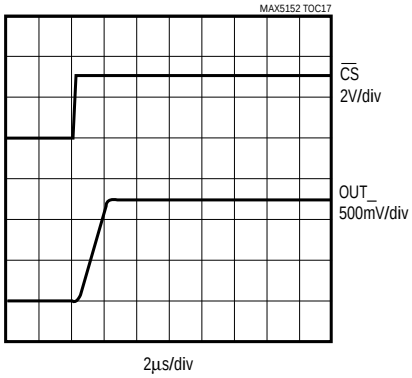
POWER-DOWN CURRENT vs. TEMPERATURE



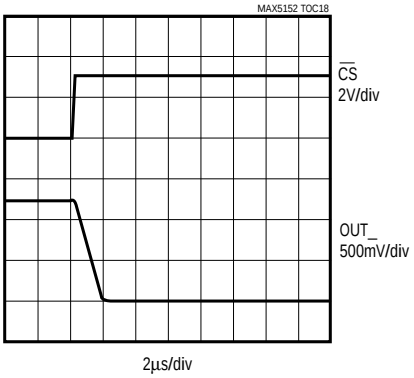
OUTPUT FFT PLOT



DYNAMIC-RESPONSE RISE TIME



DYNAMIC-RESPONSE FALL TIME



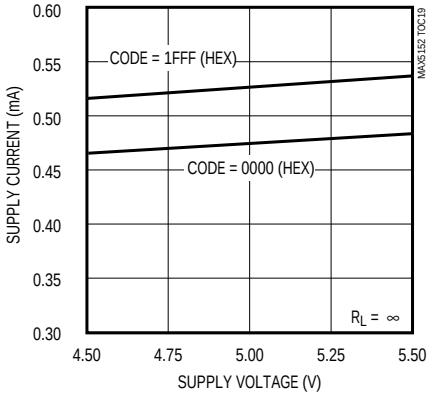
Low-Power, Dual, 13-Bit Voltage-Output DACs with Configurable Outputs

Typical Operating Characteristics (continued)

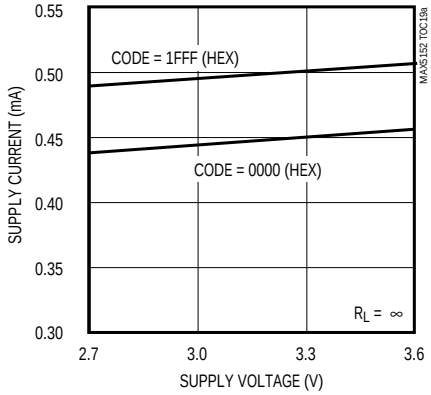
(V_{DD} = +5V (MAX5152), V_{DD} = +3V (MAX5153), R_L = 10kΩ, C_L = 100pF, FB_ tied to OUT_, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

MAX5152/MAX5153

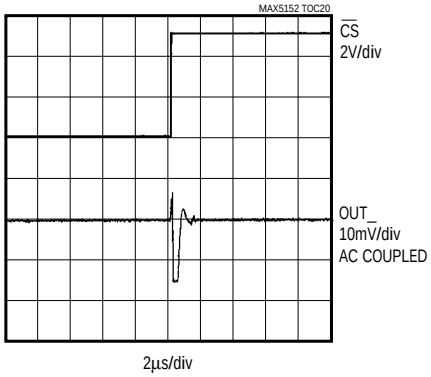
MAX5152
SUPPLY CURRENT
vs. SUPPLY VOLTAGE



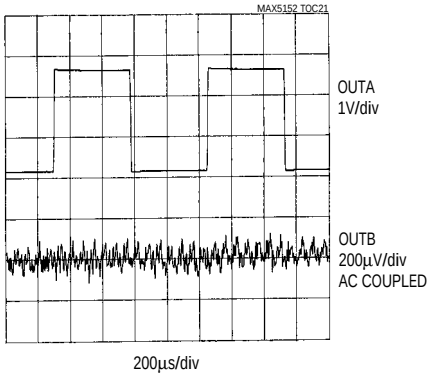
MAX5153
SUPPLY CURRENT
vs. SUPPLY VOLTAGE



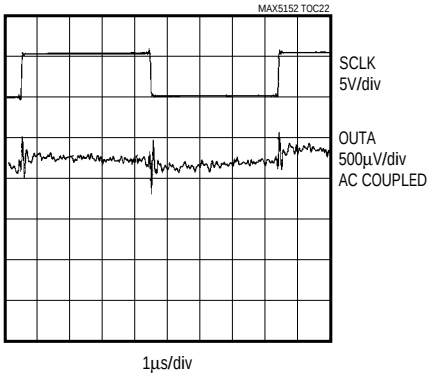
MAX5152
MAJOR-CARRY TRANSITION



MAX5152
ANALOG CROSSTALK



MAX5152
DIGITAL FEEDTHROUGH



Pin Description

PIN	NAME	FUNCTION
1	AGND	Analog Ground
2	OUTA	DAC A Output Voltage
3	FBA	DAC A Output Amplifier Feedback Input. Inverting input of the output amplifier.
4	REFA	Reference for DAC A
5	$\overline{CL}$	Active-Low Clear Input. Resets all registers to zero. DAC outputs go to 0V.
6	$\overline{CS}$	Chip-Select Input
7	DIN	Serial Data Input
8	SCLK	Serial Clock Input
9	DGND	Digital Ground
10	DOUT	Serial Data Output
11	UPO	User-Programmable Output
12	$\overline{PDL}$	Power-Down Lockout. The device cannot be powered down when $\overline{PDL}$ is low.
13	REFB	Reference Input for DAC B
14	FBB	DAC B Output Amplifier Feedback Input. Inverting input of the output amplifier.
15	OUTB	DAC B Output Voltage
16	V_{DD}	Positive Power Supply

Detailed Description

The MAX5152/MAX5153 dual, 13-bit, voltage-output DACs are easily configured with a 3-wire serial interface. These devices include a 16-bit data-in/data-out shift register, and each DAC has a double-buffered input comprised of an input register and a DAC register (see *Functional Diagram*). Both DACs use an inverted R-2R ladder network that produces a weighted voltage proportional to the input voltage value. Each DAC has its own reference input to facilitate independent full-scale values. Figure 1 depicts a simplified circuit diagram of one of the two DACs.

Reference Inputs

The reference inputs accept both AC and DC values with a voltage range extending from 0V to (V_{DD} - 1.4V). Determine the output voltage using the following equation:

$$V_{OUT} = V_{REF} \times NB / 8192$$

where NB is the numeric value of the DAC's binary input code (0 to 8191) and V_{REF} is the reference voltage.

The reference input impedance ranges from 14kΩ (1555 hex) to several giga ohms (with an input code of 0000 hex). This reference input capacitance is code dependent and typically ranges from 15pF with an input code of all zeros to 50pF with an input code of all ones.

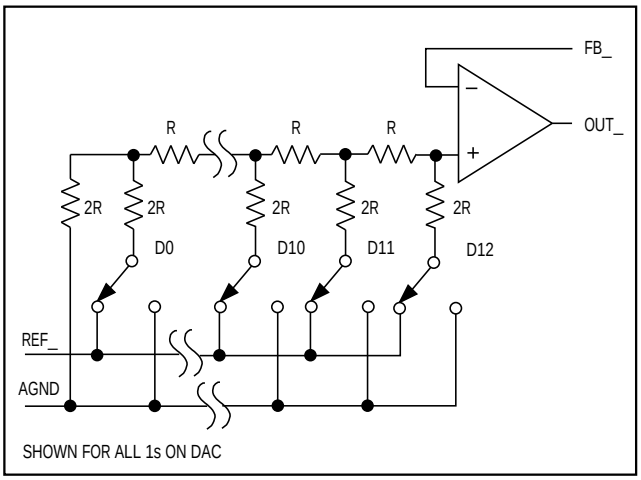


Figure 1. Simplified DAC Circuit Diagram

Output Amplifier

The output amplifier's inverting input is available to the user, allowing force and sense capability for remote sensing and specific gain configurations. The inverting input can be connected to the output to provide a unity-gain buffered output. The output amplifiers have a typical slew rate of 0.75V/µs and settle to 1/2LSB within 25µs, with a load of 10kΩ in parallel to 100pF. Loads less than 2kΩ degrade performance.

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD				FUNCTION
A0	C1	C0	D12.....D0 MSB LSB	
0	0	1	13 bits of DAC data	Load input register A; DAC register is unchanged.
1	0	1	13 bits of DAC data	Load input register B; DAC register is unchanged.
0	1	0	13 bits of DAC data	Load input register A; all DAC registers are updated.
1	1	0	13 bits of DAC data	Load input register B; all DAC registers are updated.
0	1	1	13 bits of DAC data	Load all DAC registers from the shift register (start up both DACs with new data).
1	0	0	xxxxxxxxxxxxx	Update both DAC registers from their respective input registers (start up both DACs with data previously stored in the input registers).
1	1	1	xxxxxxxxxxxxx	Shut down both DACs if $\overline{PDL}$ = 1.
0	0	0	0 0 1 x xxxxxxxxx	Update DAC register A from input register A (start up DAC A with data previously stored in input register A).
0	0	0	1 0 1 x xxxxxxxxx	Update DAC register B from input register B (start up DAC B with data previously stored in input register B).
0	0	0	1 1 0 x xxxxxxxxx	Shut down DAC A when $\overline{PDL}$ = 1.
0	0	0	1 1 1 x xxxxxxxxx	Shut down DAC B when $\overline{PDL}$ = 1.
0	0	0	0 1 0 x xxxxxxxxx	UPO goes low (default).
0	0	0	0 1 1 x xxxxxxxxx	UPO goes high.
0	0	0	1 0 0 1 xxxxxxxxx	Mode 1, DOUT clocked out on SCLK's rising edge.
0	0	0	1 0 0 0 xxxxxxxxx	Mode 0, DOUT clocked out on SCLK's falling edge (default).
0	0	0	0 0 0 x xxxxxxxxx	No operation (NOP).

"x" = don't care

Note: When A0, C1, and C0 = "0", D12, D11, D10, and D9 become control bits.

Power-Down Mode

The MAX5152/MAX5153 feature a software-programmable shutdown mode that reduces the typical supply current to 2µA. The two DACs can be shut down independently or simultaneously by using the appropriate programming word. For instance, enter shutdown mode (for both DACs) by writing an input control word of 111XXXXXXXXXXXX (Table 1). In shutdown mode, the reference inputs and amplifier outputs become high impedance, and the serial interface remains active. Data in the input registers is saved, allowing the MAX5152/MAX5153 to recall the output state prior to entering shutdown when returning to normal mode. Exit shutdown by recalling the previous condition or by updating the DAC with new information. When returning to normal operation (exiting shutdown), wait 20µs for output stabilization.

Serial Interface

The MAX5152/MAX5153 3-wire serial interface is compatible with both Microwire (Figure 2) and SPI/QSPI (Figure 3) serial-interface standards. The 16-bit serial input word consists of an address bit, two control bits, and 13 bits of data (MSB to LSB) as shown in Figure 4. The address and control bits determines the response of the MAX5152/MAX5153, as outlined in Table 1.

The MAX5152/MAX5153's digital inputs are double buffered, which allows any of the following: loading the input register(s) without updating the DAC register(s), updating the DAC register(s) from the input register(s), or updating the input and DAC registers concurrently. The address and control bits allow for the DACs to act independently.

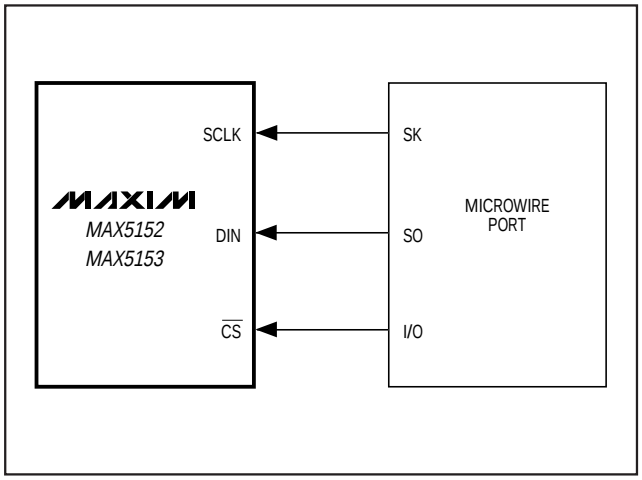


Figure 2. Connections for Microwire

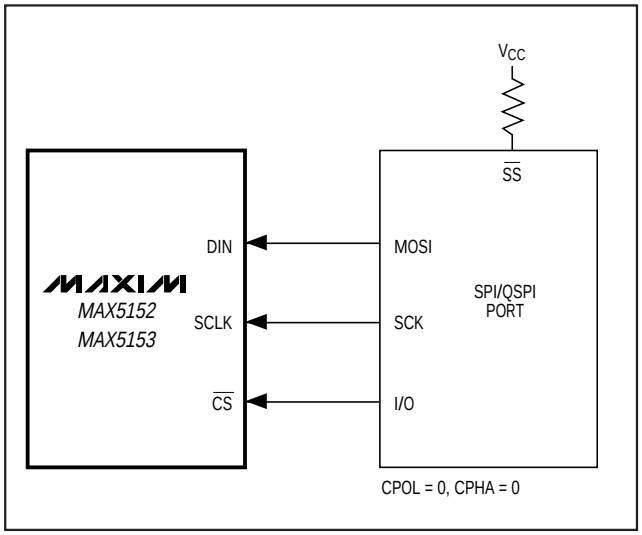


Figure 3. Connections for SPI/QSPI

MSB .....LSB		
← 16 Bits of Serial Data →		
Address Bits	Control Bits	MSB.....Data Bits.....LSB
A0	C1, C0	D12.....D0
← 1 Address/2 Control Bits →		← 13 Data Bits →

Figure 4. Serial-Data Format

Send the 16-bit data as two 8-bit packets (SPI, Microwire) or one 16-bit word (QSPI), with $\overline{CS}$ low during this period. The address and control bits determine which register will be updated, as well as the state of the registers when exiting shutdown. The 3-bit address/control determines:

- registers to be updated
- clock edge on which data is clocked out via the serial data output (DOUT)
- state of the user-programmable logic output
- configuration of the device after shutdown

The general timing diagram in Figure 5 illustrates how data is acquired. Driving $\overline{CS}$ low enables the device to receive data. Otherwise, the interface control circuitry is disabled. With $\overline{CS}$ low, data at DIN is clocked into the register on the rising edge of SCLK. As $\overline{CS}$ goes high, data is latched into the input and/or DAC registers depending on the address and control bits. The maximum clock frequency guaranteed for proper operation is 10MHz. Figure 6 depicts a more detailed timing diagram of the serial interface.

Serial Data Output (DOUT)

DOUT is the internal shift register's output. It allows for daisy-chaining and data readback. The MAX5152/MAX5153 can be programmed to shift data out of DOUT on SCLK's falling edge (Mode 0) or rising edge (Mode 1). Mode 0 provides a lag of 16 clock cycles, which maintains compatibility with SPI/QSPI and Microwire interfaces. In Mode 1, the output data lags 15.5 clock cycles. On power-up, the device defaults to Mode 0.

User-Programmable Logic Output (UPO)

UPO allows an external device to be controlled through the MAX5152/MAX5153 serial interface (Table 1), thereby reducing the number of microcontroller I/O pins required. On power-up, UPO is low.

Power-Down Lockout Input ($\overline{PDL}$)

$\overline{PDL}$ disables software shutdown when low. When in shutdown, transitioning $\overline{PDL}$ from high to low wakes up the part with the output set to the state prior to shutdown. $\overline{PDL}$ can also be used to asynchronously wake up the device.

Daisy Chaining Devices

Any number of MAX5152/MAX5153s can be daisy chained by connecting the DOUT pin of one device to the DIN pin of the following device in the chain (Figure 7).

Low-Power, Dual, 13-Bit Voltage-Output DACs with Configurable Outputs

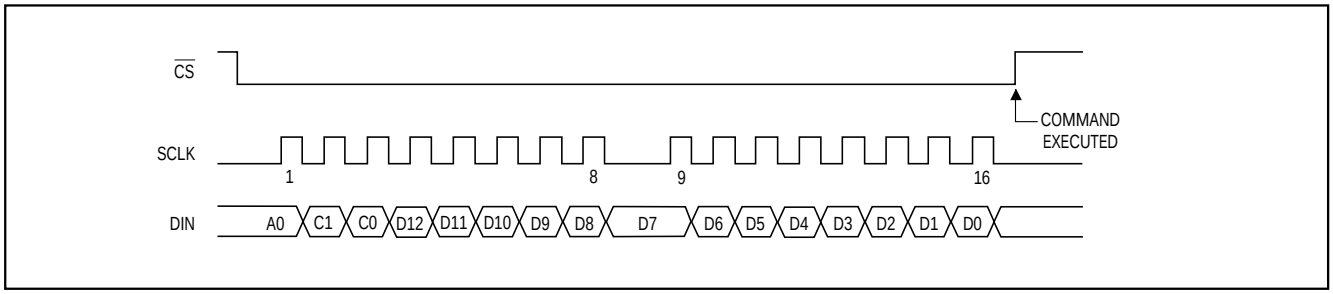


Figure 5. Serial-Interface Timing Diagram

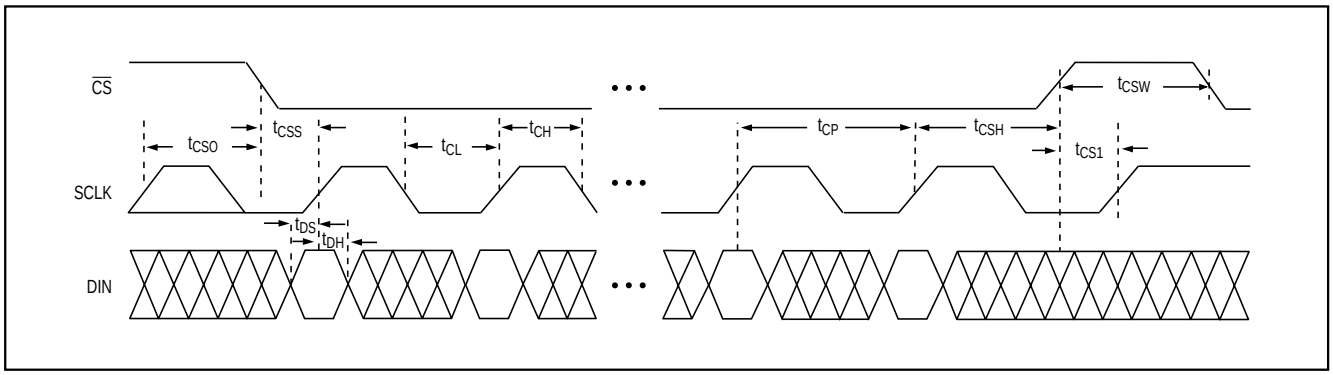


Figure 6. Detailed Serial-Interface Timing Diagram

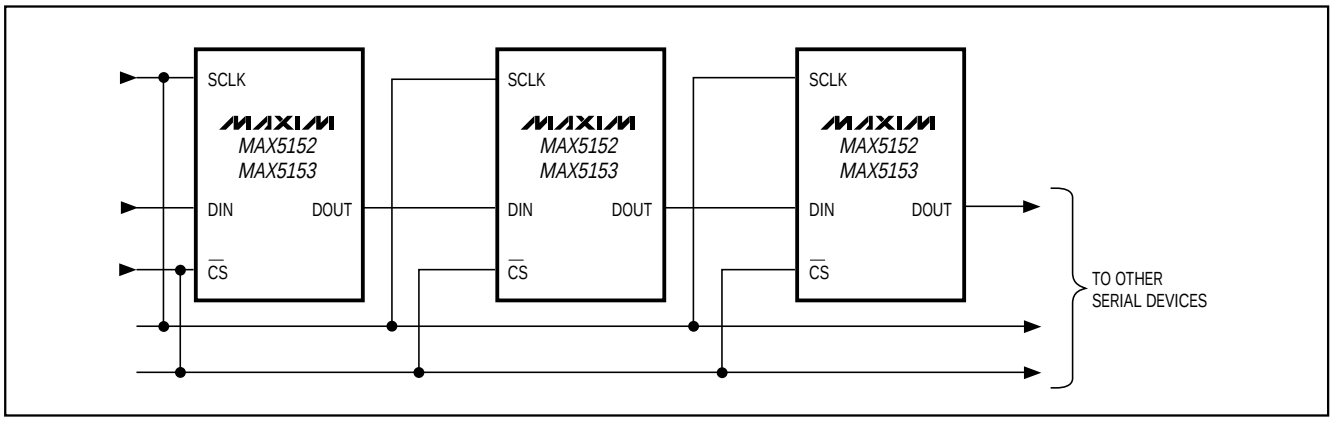


Figure 7. Daisy Chaining MAX5152/MAX5153s

Since the MAX5152/MAX5153's DOUT has an internal active pull-up, the DOUT sink/source capability determines the time required to discharge/charge a capacitive load. Refer to the digital output V_{OH} and V_{OL} specifications in the *Electrical Characteristics*.

Figure 8 shows an alternative method of connecting several MAX5152/MAX5153s. In this configuration, the data bus is common to all devices; data is not shifted through a daisy-chain. More I/O lines are required in this configuration because a dedicated chip-select input ($\overline{CS}$) is required for each IC.

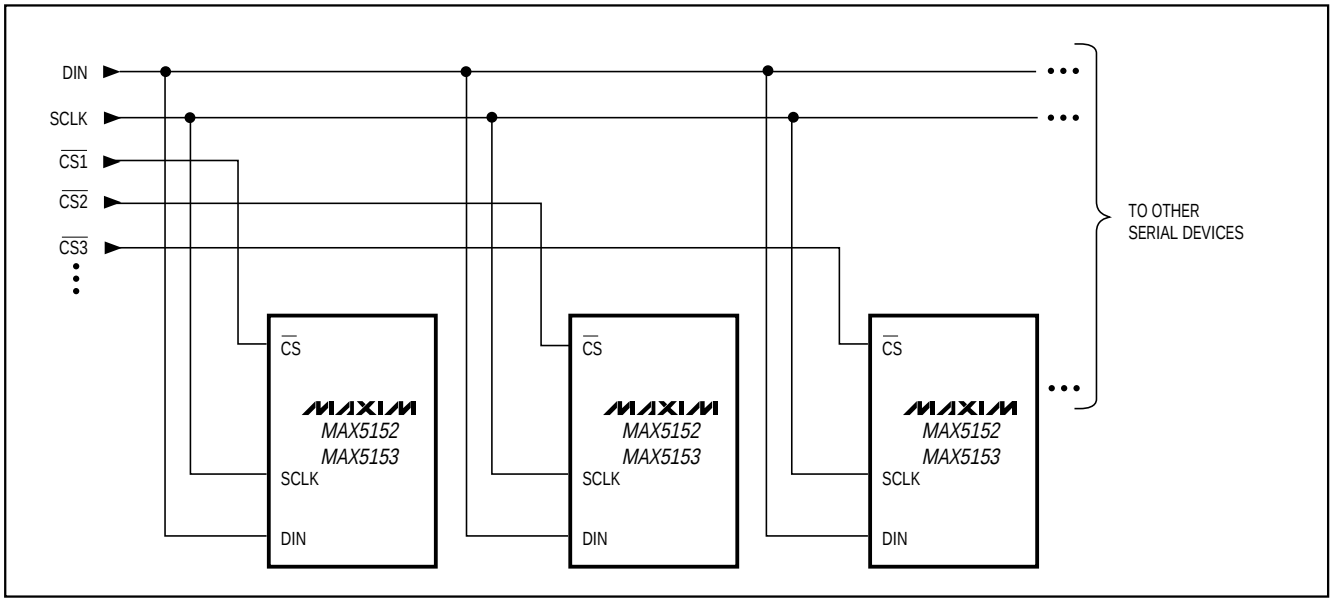


Figure 8. Multiple MAX5152/MAX5153s Sharing a Common DIN Line

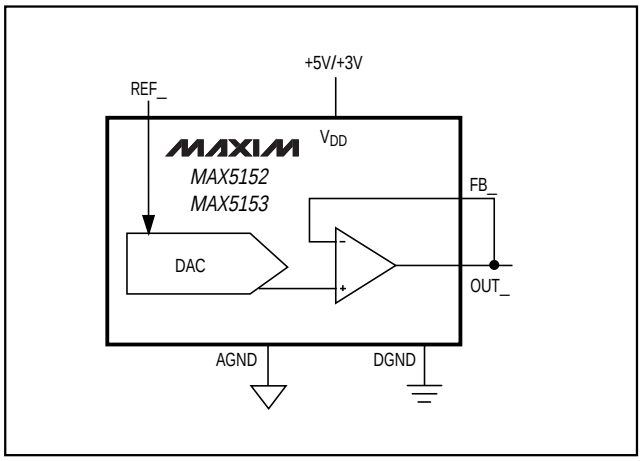


Figure 9. Unipolar Output Circuit

Table 2. Unipolar Code Table (Gain = +1)

DAC CONTENTS MSB LSB	ANALOG OUTPUT
11111 1111 1111	$+V_{REF}\left(\frac{8191}{8192}\right)$
10000 0000 0001	$+V_{REF}\left(\frac{4097}{8192}\right)$
10000 0000 0000	$+V_{REF}\left(\frac{4096}{8192}\right) = \frac{V_{REF}}{2}$
01111 1111 1111	$+V_{REF}\left(\frac{4095}{8192}\right)$
00000 0000 0001	$+V_{REF}\left(\frac{1}{8192}\right)$
00000 0000 0000	0V

Applications Information

Unipolar Output

Figure 9 depicts the MAX5152/MAX5153 configured for unity-gain, unipolar operation. Table 2 lists the unipolar output codes. To increase dynamic range, specific gain configurations can be used as shown in Figure 10.

Bipolar Output

The MAX5152/MAX5153 can be configured for a bipolar output, as shown in Figure 11. The output voltage is given by the equation:

$$V_{OUT} = V_{REF}\,[((2 \times NB) / 8192) - 1]$$

where NB represents the numeric value of the DAC's binary input code. Table 3 shows digital codes and the corresponding output voltage for Figure 11's circuit.

Low-Power, Dual, 13-Bit Voltage-Output DACs with Configurable Outputs

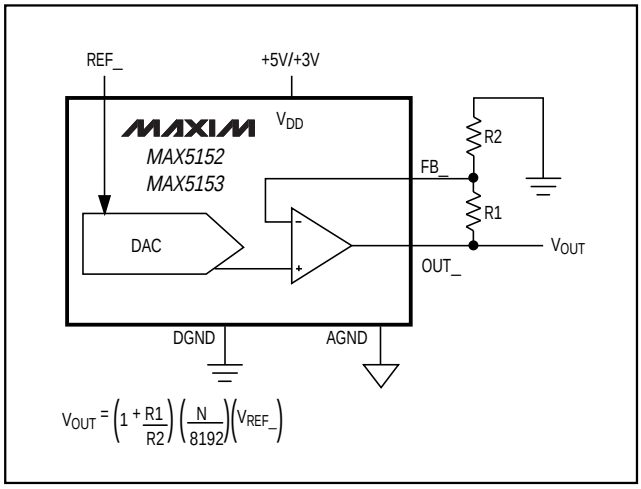


Figure 10. Configurable Output Gain

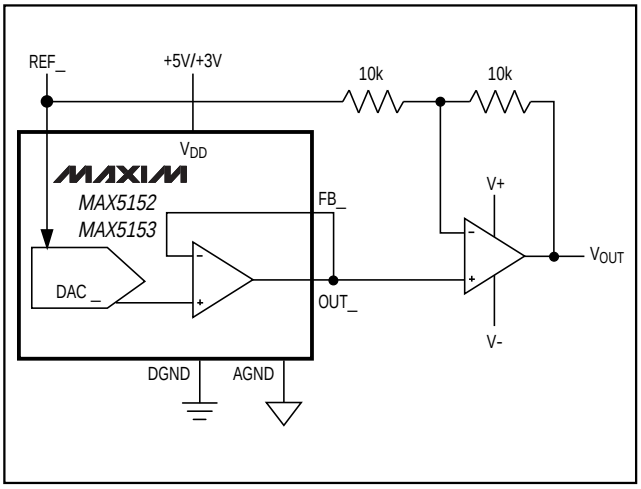


Figure 11. Bipolar Output Circuit

Table 3. Bipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
11111 1111 1111	$+V_{REF}\left(\frac{4095}{4096}\right)$
10000 0000 0001	$+V_{REF}\left(\frac{1}{4096}\right)$
10000 0000 0000	0V
01111 1111 1111	$-V_{REF}\left(\frac{1}{4096}\right)$
00000 0000 0001	$-V_{REF}\left(\frac{4095}{4096}\right)$
00000 0000 0000	$-V_{REF}\left(\frac{4096}{4096}\right) = -V_{REF}$

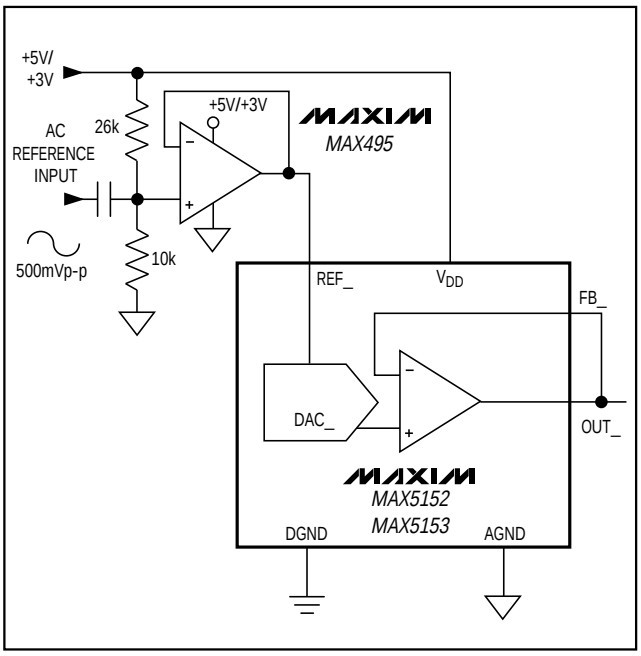


Figure 12. AC Reference Input Circuit

Using an AC Reference

In applications where the reference has an AC signal component, the MAX5152/MAX5153 have multiplying capabilities within the reference input voltage range specifications. Figure 12 shows a technique for applying a sinusoidal input to the reference input to REF_, where the AC signal is offset before being applied to the reference input.

Harmonic Distortion and Noise

The total harmonic distortion plus noise (THD+N) is typically less than -80dB at full scale with a 1Vp-p input swing at 5kHz. The typical -3dB frequency is 600kHz for both devices, as shown in the *Typical Operating Characteristics*.

Digital Calibration and Threshold Selection

Figure 13 shows the MAX5152/MAX5153 in a digital calibration application. With a bright value applied to the photodiode (on), the DAC is digitally ramped up until it trips the comparator. The microprocessor stores this high calibration value. Repeat the process with a dim light (off) to obtain the dark current calibration. The microprocessor then programs the DAC to set an output voltage that is the midpoint of the two calibration values. Applications include tachometers, motion sensing, automatic readers, and liquid clarity analysis.

Digital Control of Gain and Offset

The two DACs can be used to control the offset and gain for curve-fitting nonlinear functions, such as transducer linearization or analog compression/expansion applications. The input signal is used as the reference for the gain-adjust DAC, whose output is summed with the output from the offset-adjust DAC. The relative weight of each DAC output is adjusted by R1, R2, R3, and R4 (Figure 14).

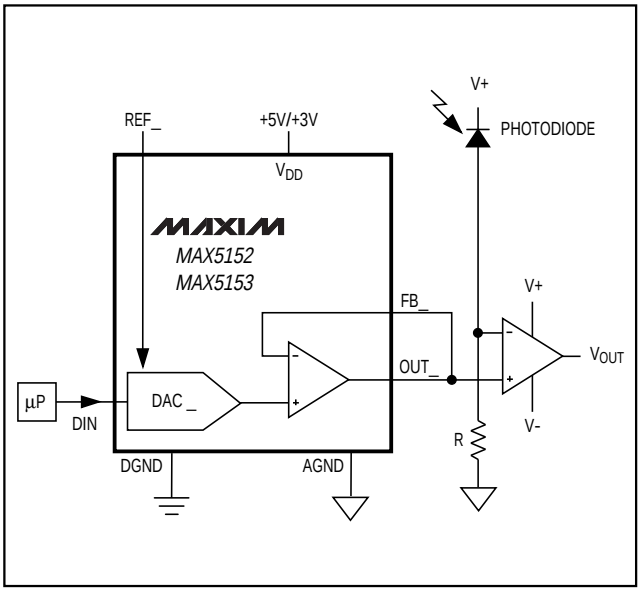


Figure 13. Digital Calibration

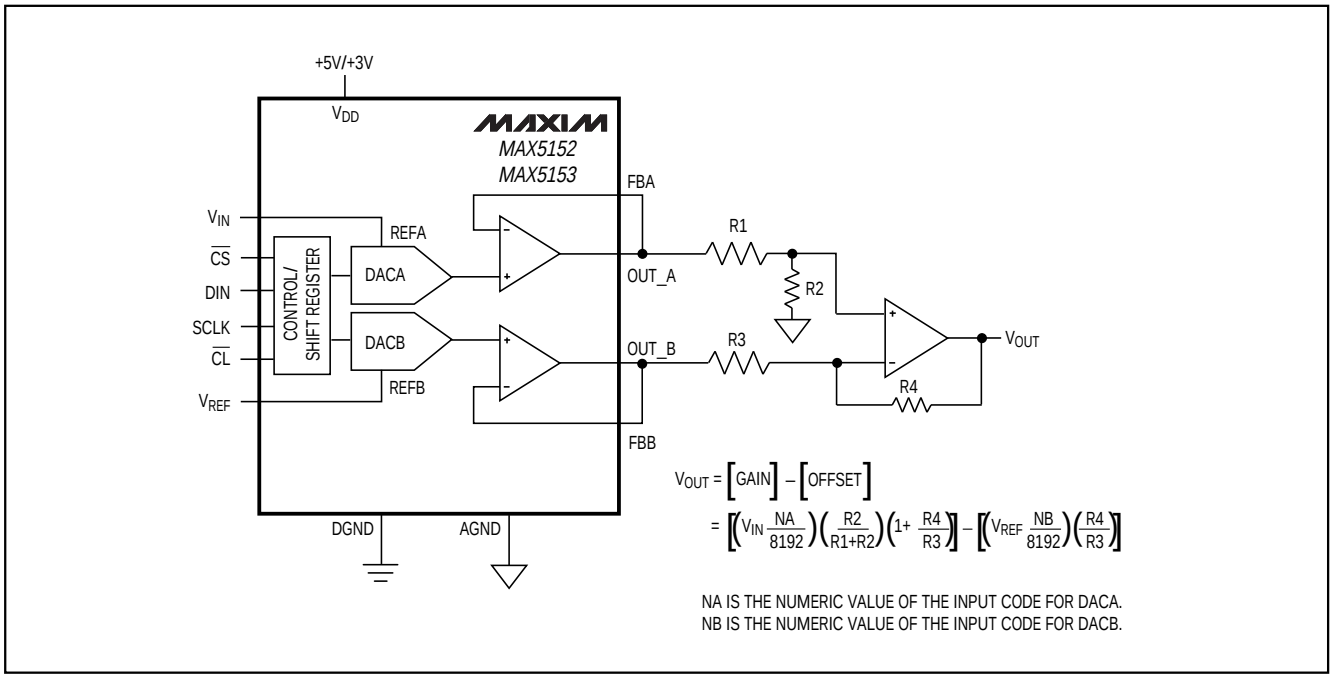


Figure 14. Digital Control of Gain and Offset

Digital Programmable Current Source

Figure 15 depicts a digitally programmable, unidirectional current source that can be used in industrial control applications. The output current is:

$$I_{OUT} = (V_{REF} / R) (NB / 8192)$$

where NB is the DAC code and R is the sense resistor.

Power-Supply Considerations

On power-up, the input and DAC registers clear (reset to zero code). For rated performance, $V_{REF\_}$ should be at least 1.4V below V_{DD}. Bypass the power supply with a 4.7µF capacitor in parallel with a 0.1µF capacitor to GND. Minimize lead lengths to reduce lead inductance.

Grounding and Layout Considerations

Digital and AC transient signals on AGND can create noise at the output. Connect AGND to the highest quality ground available. Use proper grounding techniques, such as a multilayer board with an unbroken, low-inductance ground plane. Carefully lay out the traces between channels to reduce AC cross-coupling and crosstalk. Wire-wrapped boards and sockets are not recommended. If noise becomes an issue, shielding may be required.

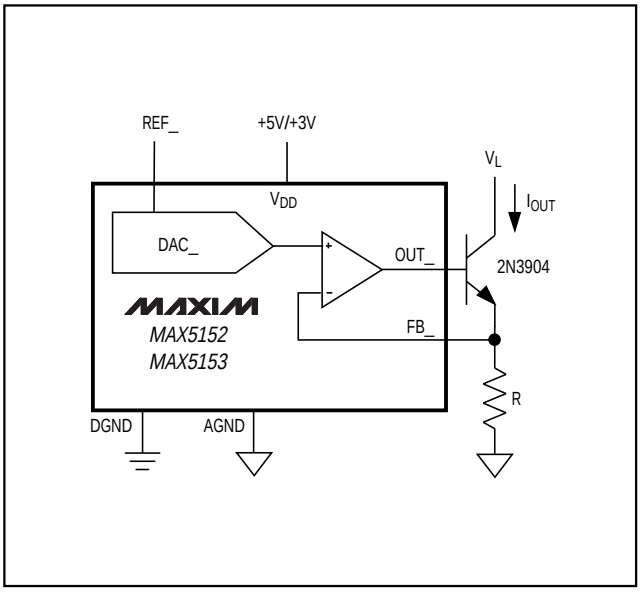


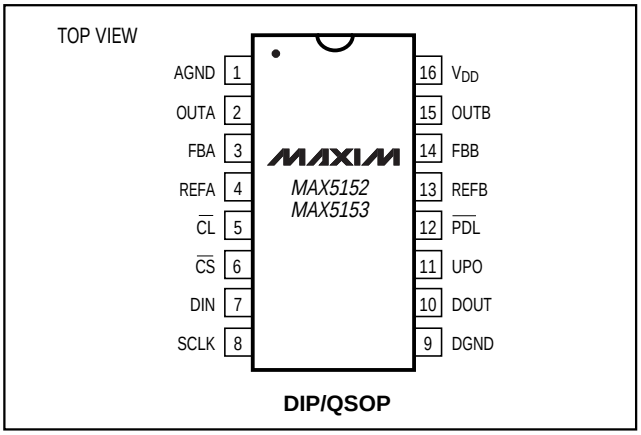
Figure 15. Digitally Programmable Current Source

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5152AEPE	-40°C to +85°C	16 Plastic DIP	±1/2
MAX5152BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX5152AEEE	-40°C to +85°C	16 QSOP	±1/2
MAX5152BEEE	-40°C to +85°C	16 QSOP	±1
MAX5152BMJE	-55°C to +125°C	16 CERDIP**	±1
MAX5153ACPE	0°C to +70°C	16 Plastic DIP	±1
MAX5153BCPE	0°C to +70°C	16 Plastic DIP	±2
MAX5153ACEE	0°C to +70°C	16 QSOP	±1
MAX5153BCEE	0°C to +70°C	16 QSOP	±2
MAX5153BC/D	0°C to +70°C	Dice*	±2
MAX5153AEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX5153BEPE	-40°C to +85°C	16 Plastic DIP	±2
MAX5153AEEE	-40°C to +85°C	16 QSOP	±1
MAX5153BEEE	-40°C to +85°C	16 QSOP	±2
MAX5153BMJE	-55°C to +125°C	16 CERDIP**	±2

**Dice are tested at T_A = +25°C, DC parameters only.*
***Contact factory for availability.*

_____Pin Configuration



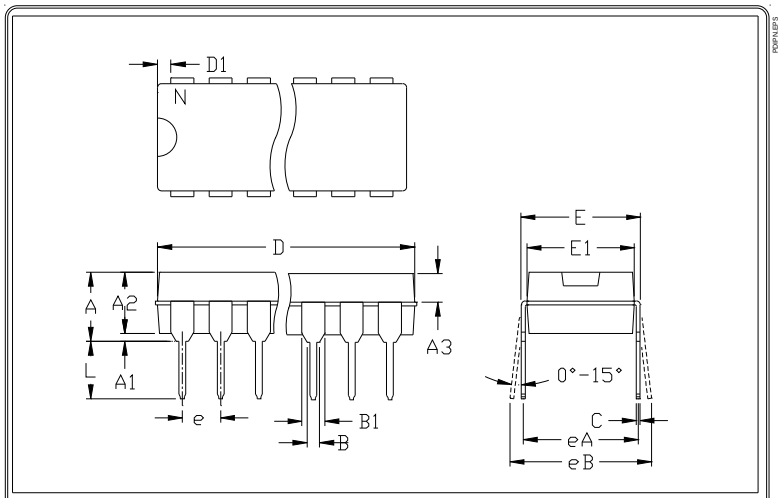
_____Chip Information

TRANSISTOR COUNT: 3053

SUBSTRATE CONNECTED TO AGND

Low-Power, Dual, 13-Bit Voltage-Output DACs with Configurable Outputs

Package Information



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

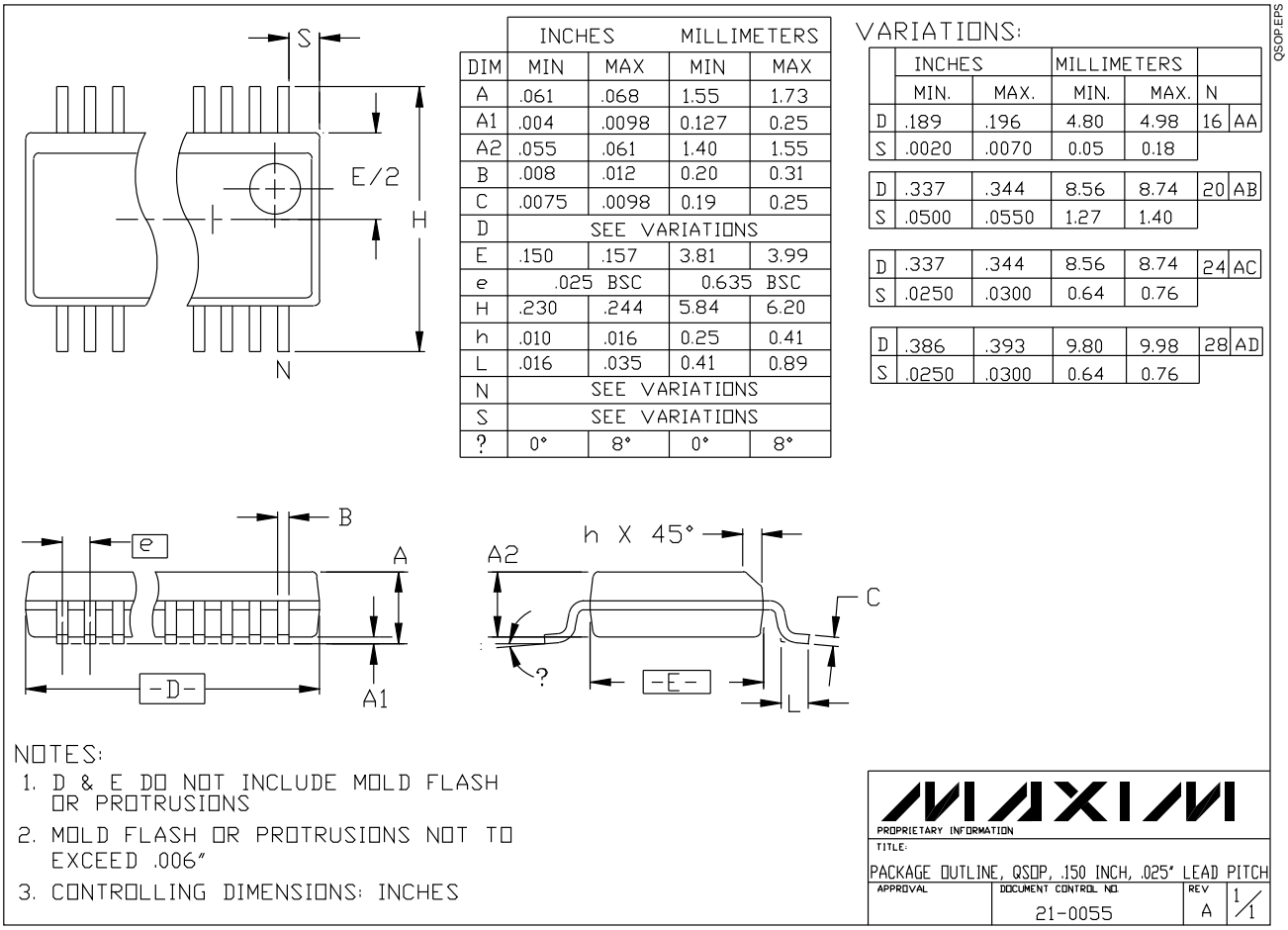
	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM — 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION

TITLE: PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 A DOCUMENT CONTROL NUMBER REV

Package Information (continued)



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.127	0.25
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.19	0.25
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
S	SEE VARIATIONS			
?	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.27	1.40		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.64	0.76		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.64	0.76		

QSOP.EPS

NOTES:

1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006"
3. CONTROLLING DIMENSIONS: INCHES

MAXIM

PROPRIETARY INFORMATION

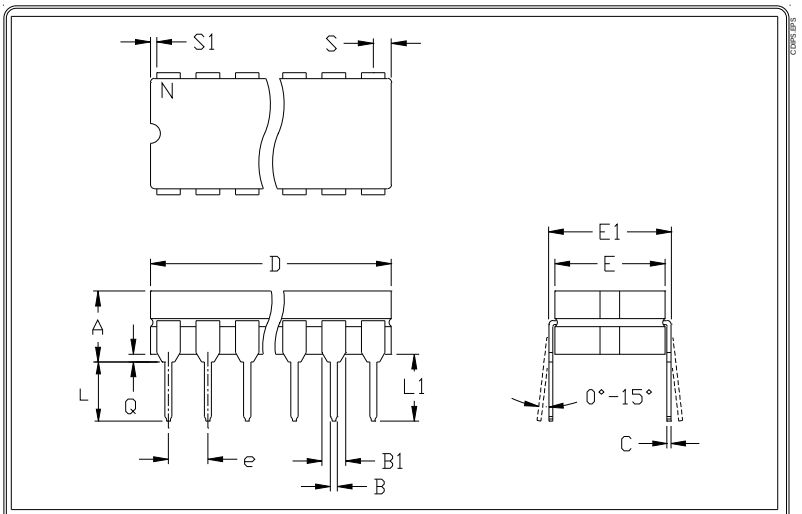
TITLE:

PACKAGE OUTLINE, QSOP, .150 INCH, .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	A	1/1

Low-Power, Dual, 13-Bit Voltage-Output DACs with Configurable Outputs

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	---	0.00	---
Q	0.015	0.070	0.38	1.78
S	---	0.098	---	2.49
S1	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	0.405	---	10.29	8	P:D4
D	---	0.785	---	19.94	14	C:D1
D	---	0.840	---	21.34	16	E:D2
D	---	0.960	---	24.38	18	V:D6
D	---	1.060	---	26.92	20	R:D8
D	---	1.280	---	32.51	24	L:D9

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #1 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION | TITLE: PACKAGE FAMILY OUTLINE: CDIP .300" | 1/1 | DOCUMENT CONTROL NUMBER 21-0045 A REV