

Absolute Maximum Ratings

IN, EN, LX, BSOUT to SGND.....-0.3V to +80V
 PGND_BST, PGND_LDO to SGND.....-0.3V to +0.3V
 RESET, OUT, OUT_SENSE to SGND.....-0.3V to +12V
 BSOUT to LX (MAX5092_).....-0.3V to +12V
 VL, SET, BSFB, SGND.....-0.3V to +6V
 HOLD to SGND.....-0.3V to ($V_{OUT} + 0.3V$)
 CT to SGND.....-0.3V to ($V_{VL} + 0.3V$)
 OUT Current (I_{OUT}) Short Circuit to PGND_LDO,
 ($V_{IN} \leq 28V$).....Continuous

RESET Sinking Current.....5mA
 Continuous Power Dissipation ($T_A = +70^\circ C$)
 Thin QFN (derate 33.3mW/ $^\circ C$
 above $+70^\circ C$).....2666mW (Note 1)
 Operating Temperature Range-40 $^\circ C$ to +125 $^\circ C$
 Maximum Junction Temperature+150 $^\circ C$
 Storage Temperature Range-60 $^\circ C$ to +150 $^\circ C$
 Lead Temperature (soldering, 10s)+300 $^\circ C$

Note 1: As per JEDEC Standard 51 (Multilayer Board).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

($V_{IN} = V_{EN} = 14V$, $I_{OUT} = 1mA$, $C_{IN} = 47\mu F$, $C_{BSOUT} = 22\mu F$, $C_{OUT} = 10\mu F$, $C_{VL} = 1\mu F$, $T_A = T_J = -40^\circ C$ to +125 $^\circ C$, unless otherwise noted. See Figures 4–7 as applicable. Typical specifications are at $T_A = +25^\circ C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage Range	V_{IN}	(Note 3)	4		72	V
Internal Input Undervoltage Lockout	V_{UVLOF}	V_{IN} falling	3.0	3.2	3.4	V
	V_{UVLOR}	V_{IN} rising	3.4	3.6	3.8	
Supply Current (Boost Converter Off)	I_Q	LDO mode, $I_{OUT} = 100\mu A$ $T_J = -40^\circ C$ to +125 $^\circ C$ (Note 4)		65	85	μA
		LDO mode, $I_{OUT} = 250mA$		70	100	
Supply Current (Boost Converter On)	I_S	$V_{IN} = 5V$		0.4	1.0	mA
Shutdown Supply Current	I_{SHDN}	$V_{EN} \leq +0.4V$ $T_J = -40^\circ C$ to +125 $^\circ C$ (Note 4)		6	10	μA
BOOST CONVERTER						
Minimum BSOUT Output Current	I_{BSOUT}	$V_{IN} = 4V$		250		mA
Boost Converter Enable Threshold	V_{BST_EN}	$V_{BSOUT} - V_{OUT}$ falling (Note 5)	1.7	2.0	2.3	V
Boost Converter Disable Threshold	V_{BST_DIS}	$V_{BSOUT} - V_{OUT}$ rising (Note 5)	2.2	2.5	2.8	V
Boost Converter Disable Hysteresis	V_{BST_HYS}			0.5		V
BSOUT Output Voltage	V_{BSOUT}	$V_{IN} = 4V$, BSFB = SGND, $V_{OUT} = 5V$		7.00		V
Maximum BSOUT Output Voltage	$V_{BSOUT(MAX)}$	MAX5092_		11		V
		MAX5093_		12		
BSFB Regulation Voltage	V_{BSFB}		1.18	1.24	1.30	V
BSFB Input Bias Current	I_{BSFB}				100	nA
Boost Internal Switch On-Resistance	$R_{DS(ON)}$			0.5	1.2	Ω
Boost Internal Switch Minimum Off-Time	t_{OFF}		0.80	1	1.25	μs

Electrical Characteristics (continued)

($V_{IN} = V_{EN} = 14V$, $I_{OUT} = 1mA$, $C_{IN} = 47\mu F$, $C_{BSOUT} = 22\mu F$, $C_{OUT} = 10\mu F$, $C_{VL} = 1\mu F$, $T_A = T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. See Figures 4–7 as applicable. Typical specifications are at $T_A = +25^{\circ}C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Boost Internal Switch Maximum On-Time	t _{ON-max}			1.80	2.25	2.70	μs
Internal Switch Current Limit	I _{LIM}	Measured in steady-state condition		1.5		3.0	A
Boost Turn-On Response Time		Time from V _{BSOUT} falling below regulation to switch on-time			2	5	μs
Internal Diode Forward Voltage Drop	V _F	MAX5092_ only, I _F = 1A			0.95		V
LDO							
Guaranteed Output Current	I _{OUT}	V _{BSOUT} - V _{OUT} = 2V (Note 6)		250			mA
Output Voltage	V _{OUT}	SET = SGND, MAX5092A/ MAX5093A	I _{OUT} = 1mA	3.25	3.3	3.35	V
			100μA ≤ I _{OUT} ≤ 250mA	3.2	3.3	3.4	
		SET = SGND, MAX5092B/ MAX5093B	I _{OUT} = 1mA	4.900	5	5.075	
			100μA ≤ I _{OUT} ≤ 250mA	4.85	5	5.10	
Minimum Adjustable Output Voltage	V _{ADJMIN}	Boost operation, V _{IN} = 4V, V _{BSOUT} = 7V		1.5			V
Maximum Adjustable Output Voltage	V _{ADJMAX}	Boost operation, V _{IN} = 4V	MAX5092_, V _{BSOUT} = 11V	9			V
			MAX5093_, V _{BSOUT} = 12V	10			
Adjustable Output Voltage	V _{ADJ}	LDO operation, V _{IN} ≥ V _{BST_DIS} (boost converter off) (Note 7)		1.5		10.0	V
Dropout Voltage	ΔV _{DO}	I _{OUT} = 250mA (Note 8)			0.9	1.6	V
LDO Startup Response Time		Rising edge of V _{BSOUT} to the rising edge of V _{OUT} , R _L = 500Ω, SET = SGND			200		μs
Line Regulation	ΔV _{OUT} / ΔV _{IN}	7V ≤ V _{IN} ≤ 72V, I _{LOAD} = 10mA	MAX5092A/MAX5093A	0.4			mV/V
			MAX5092B/MAX5093B	0.5			
		7V ≤ V _{IN} ≤ 28V, I _{LOAD} = 250mA			1.6		
SET Reference Voltage	V _{SET}			1.205	1.235	1.265	V
SET Input Bias Current	I _{SET}				0.5	100	nA
Load Regulation	ΔV _{OUT} / ΔI _{OUT}	I _{OUT} = 1mA to 250mA			0.2	0.6	mV/mA
Power-Supply Rejection Ratio	PSRR	f = 100Hz	I _{OUT} = 10mA, V _{BSOUT(AC)} = 500mV _{P-P} , V _{OUT} = 5V	80			dB
		f = 1MHz	I _{OUT} = 10mA, V _{BSOUT(AC)} = 500mV _{P-P} , V _{OUT} = 5V	60			
Short-Circuit Current	I _{SC}			255	490		mA

Electrical Characteristics (continued)

($V_{IN} = V_{EN} = 14V$, $I_{OUT} = 1mA$, $C_{IN} = 47\mu F$, $C_{BSOUT} = 22\mu F$, $C_{OUT} = 10\mu F$, $C_{VL} = 1\mu F$, $T_A = T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. See Figures 4–7 as applicable. Typical specifications are at $T_A = +25^{\circ}C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE, $\overline{HOLD}$ and $\overline{RESET}$						
EN High Input Threshold	EN_H		2.4			V
EN Low Input Threshold	EN_L				0.4	V
EN Input Bias Current	I_{EN}			0.25	2	μA
$\overline{HOLD}$ Low Input Threshold	V_{IL}	Regulator on, EN transition from high to low			0.4	V
$\overline{HOLD}$ Release Voltage	V_{IH}	EN = low	$V_{OUT} - 0.4$			V
$\overline{HOLD}$ Pullup Current	I_{HOLD}	Internally connected to OUT		4		μA
$\overline{RESET}$ Voltage Threshold	V_{RESET}	% of V_{OUT} , V_{OUT} falling	87	90	92	%
$\overline{RESET}$ Threshold Hysteresis	V_{RHYST}	% of V_{OUT}		2		%
$\overline{RESET}$ Output Low Voltage	V_{RL}	$I_{SINK} = 1mA$			0.4	V
$\overline{RESET}$ Output High Leakage Current	I_{RH}	$V_{RESET} = 5V$			1	μA
$\overline{RESET}$ Output Minimum Timeout Period		C_{CT} not connected		25		μs
EN to $\overline{RESET}$ Minimum Timeout Delay		C_{CT} not connected		260		μs
Delay Comparator Threshold (Rising)	V_{CTTH}		1.205	1.24	1.265	V
Delay Comparator Threshold Hysteresis	$V_{CTTH-HYS}$			100		mV
CT Charge Current	I_{CT-CHG}		1.5	2	2.5	μA
CT Discharge Current	I_{CT-DIS}			5		mA
Thermal Shutdown Temperature Threshold	$T_{J(SHDN)}$	Temperature rising		+165		$^{\circ}C$
Thermal Shutdown Temperature Hysteresis	$T_{J(HYST)}$			20		$^{\circ}C$

Note 2: Limits at $-40^{\circ}C$ are guaranteed by design and characterization; not production tested.

Note 3: Guaranteed minimum operating voltage is 3.5V on V_{IN} falling only.

Note 4: Guaranteed by design and not production tested.

Note 5: The boost converter disable threshold (V_{BST_DIS}) is a static measurement. Internal comparator delay may cause a higher disable level.

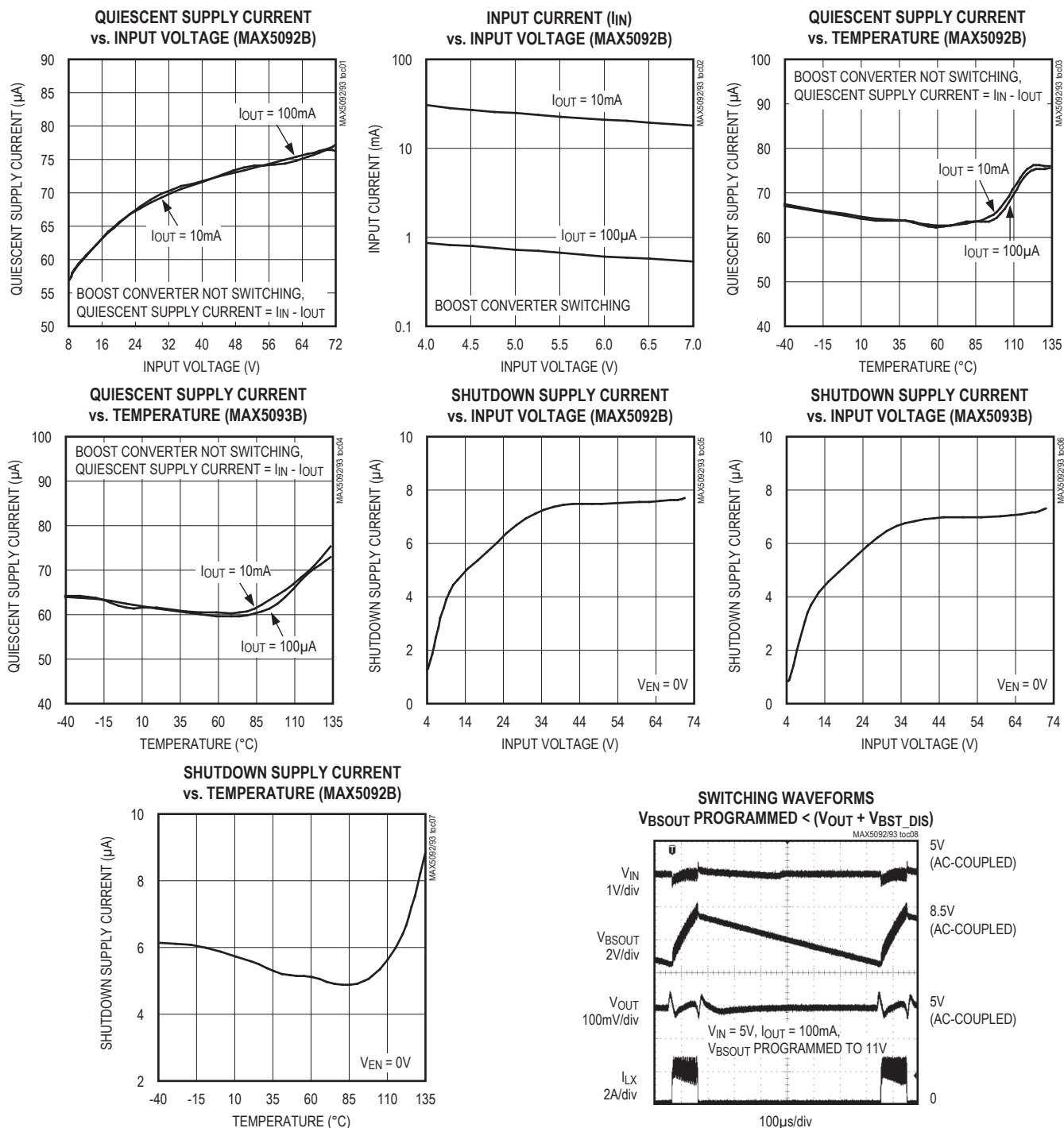
Note 6: The continuous maximum output current from the LDO is guaranteed according to the maximum power dissipation imposed by the package thermal constraints.

Note 7: Maximum output adjustable value is conditioned by the maximum adjustable BSOUT Output Voltage Range minus the maximum dropout across the pass transistor.

Note 8: Dropout voltage is defined as ($V_{BSOUT} - V_{OUT}$) when V_{OUT} is 2% below the value of V_{OUT} for $V_{BSOUT} = V_{OUT} + 2V$.

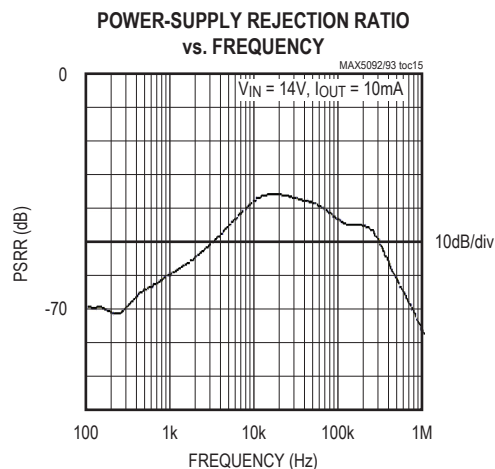
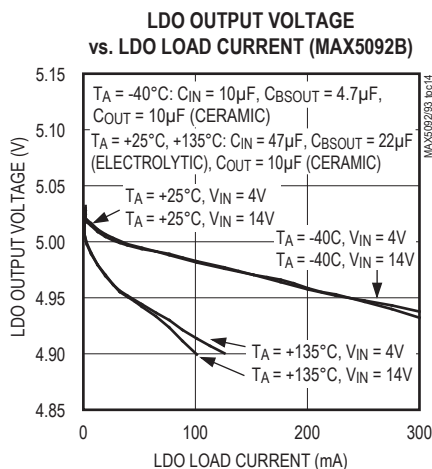
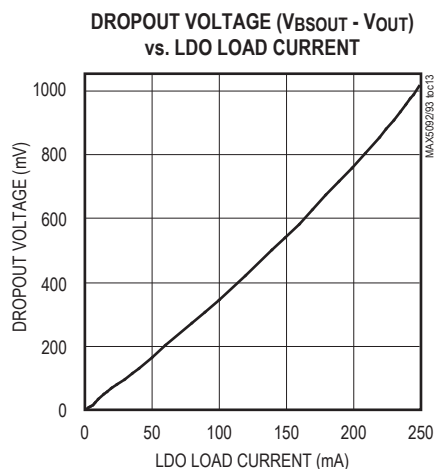
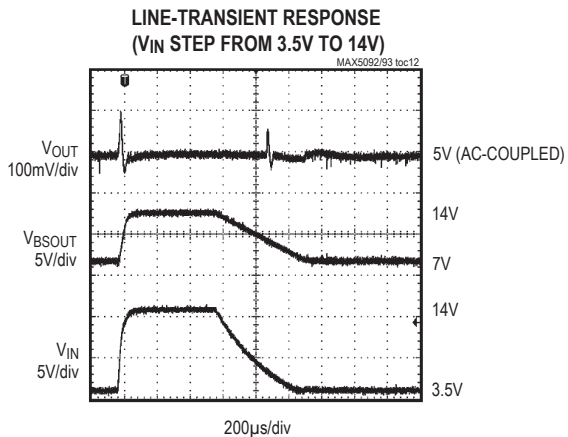
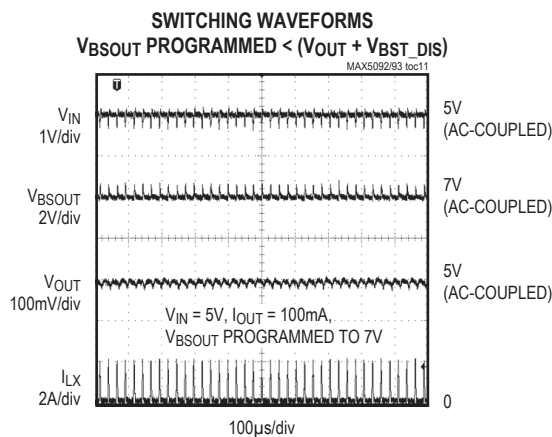
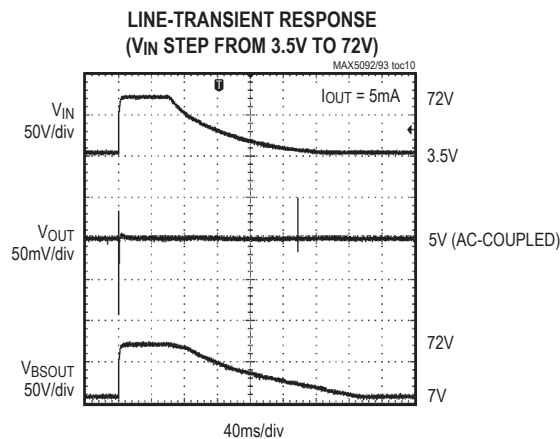
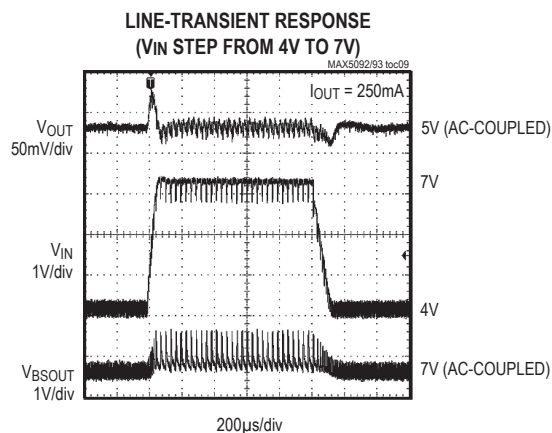
Typical Operating Characteristics

($V_{IN} = V_{EN} = 14V$, $C_{IN} = 47\mu F$, $C_{BSOUT} = 22\mu F$, $C_{OUT} = 10\mu F$, $C_{VL} = 1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.) (See Figures 4–7 as applicable.)



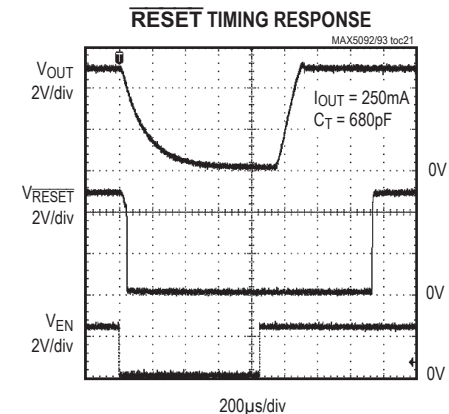
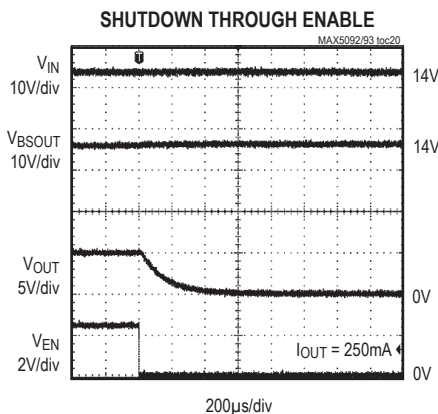
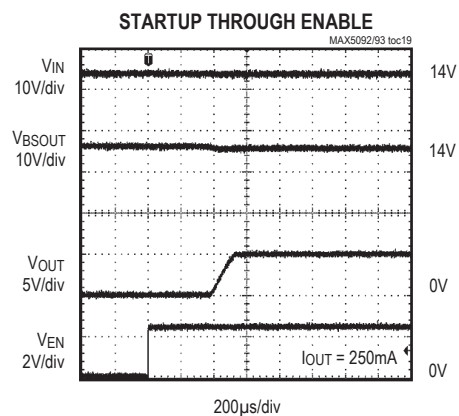
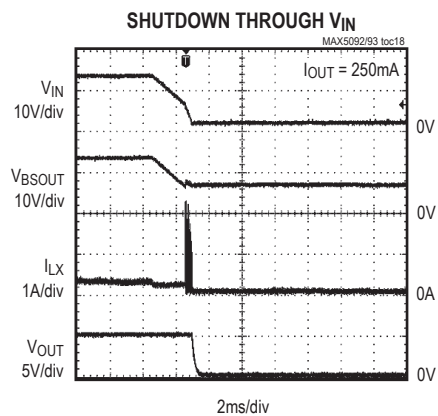
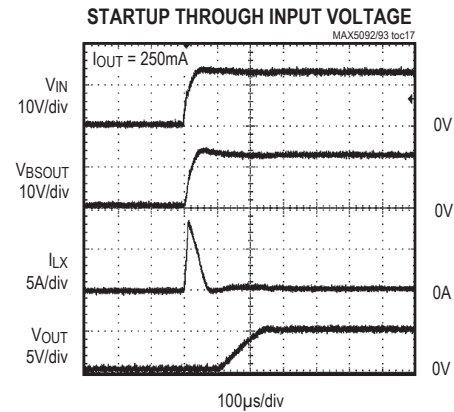
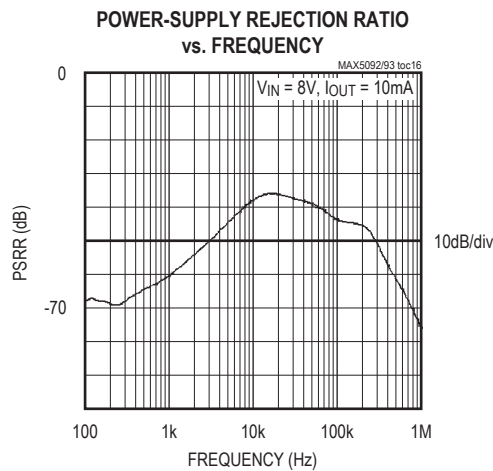
Typical Operating Characteristics (continued)

($V_{IN} = V_{EN} = 14V$, $C_{IN} = 47\mu F$, $C_{BSOUT} = 22\mu F$, $C_{OUT} = 10\mu F$, $C_{VL} = 1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.) (See Figures 4–7 as applicable.)



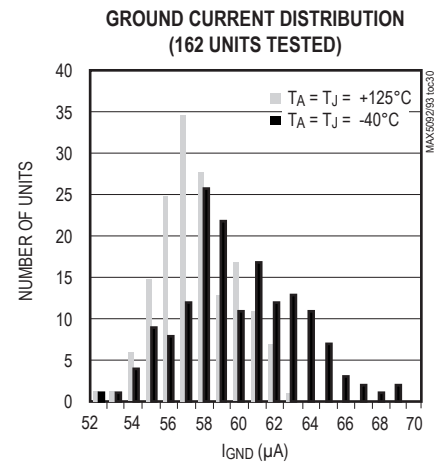
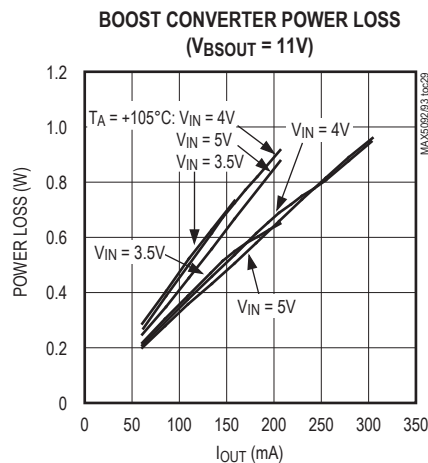
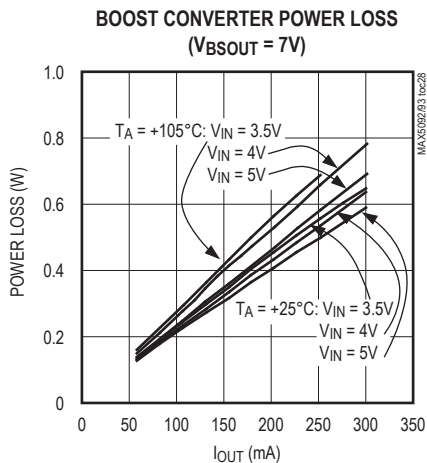
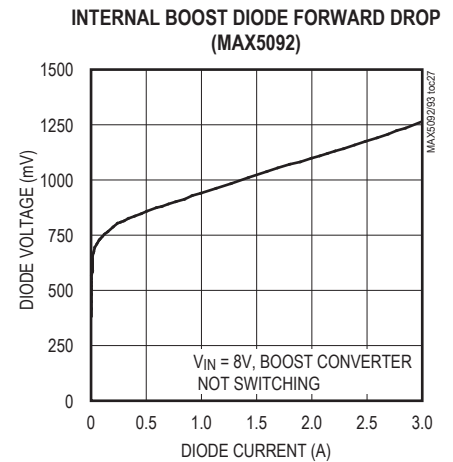
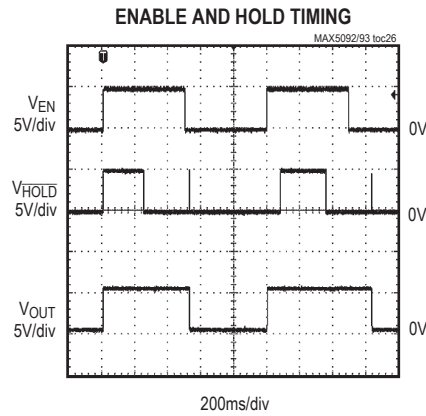
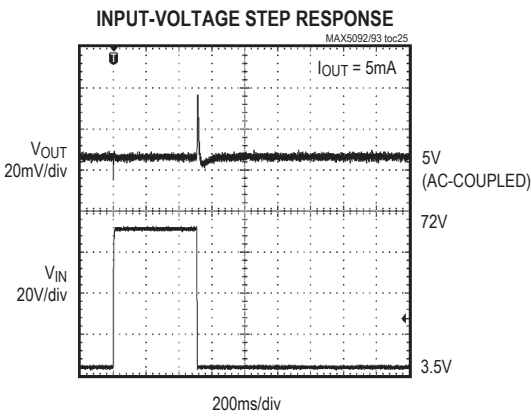
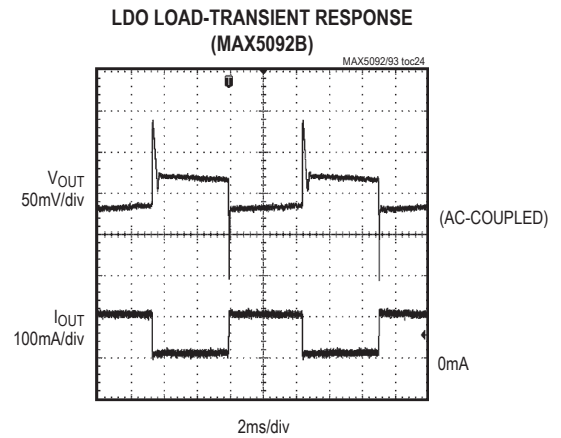
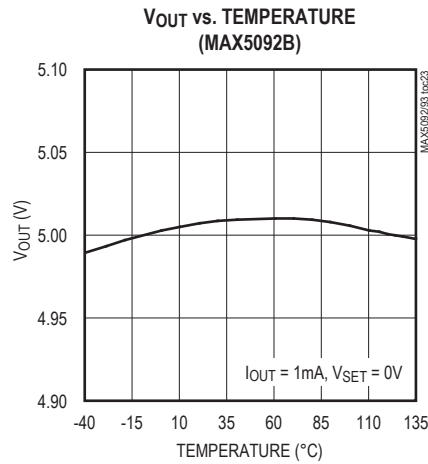
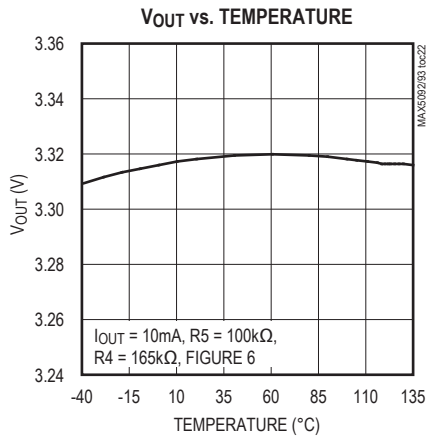
Typical Operating Characteristics (continued)

($V_{IN} = V_{EN} = 14V$, $C_{IN} = 47\mu F$, $C_{BSOUT} = 22\mu F$, $C_{OUT} = 10\mu F$, $C_{VL} = 1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.) (See Figures 4–7 as applicable.)



Typical Operating Characteristics (continued)

($V_{IN} = V_{EN} = 14V$, $C_{IN} = 47\mu F$, $C_{BSOUT} = 22\mu F$, $C_{OUT} = 10\mu F$, $C_{VL} = 1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.) (See Figures 4–7 as applicable.)



Pin Description

PIN	NAME	FUNCTION
1	IN	Input Supply Voltage. Bypass IN to the power ground plane with a 47 μ F (low-ESR) aluminum electrolytic capacitor in parallel with a 1 μ F ceramic capacitor placed as close to the IC as possible.
2	EN	Enable Input. Drive EN high to turn on the IC. Drive EN low to disable the IC. Connect EN directly to IN for always-on operation.
3	SGND	Signal Ground. Connect SGND to the signal ground plane and the exposed paddle. Connect the power ground and signal ground plane together at the negative terminal of the input capacitor(s).
4	$\overline{\text{HOLD}}$	Output Hold. When $\overline{\text{HOLD}}$ is forced low, the regulator stores the on-state of the output, allowing the regulator to remain enabled even if EN is pulled low. To shut down the regulator, release $\overline{\text{HOLD}}$ after EN is pulled low. If $\overline{\text{HOLD}}$ is unused, either connect $\overline{\text{HOLD}}$ to OUT or leave unconnected. $\overline{\text{HOLD}}$ is internally connected to OUT through a 4 μ A pullup current.
5	PGND_LDO	LDO Power Ground. Connect PGND_LDO to the power ground plane. Connect the PGND_LDO ground and signal ground plane together.
6	SET	Feedback Input for the LDO. Connect SET directly to SGND to set the output voltage of the LDO to the preset voltage of 3.3V (MAX5092A/MAX5093A) or 5V (MAX5092B/MAX5093B). Connect SET to the center tap of a resistor-divider connected between the LDO output and SGND to set the output voltage. V_{SET} regulates to 1.24V when using an adjustable output.
7	OUT_SENSE	LDO Regulator Output Sense. Connect OUT_SENSE to OUT at the output capacitor near the load.
8	OUT	LDO Regulator Output. Bypass OUT to the power ground plane with a 10 μ F ceramic capacitor. V_{OUT} regulates to a preset voltage of 3.3V (MAX5092A/MAX5093A) or 5V (MAX5092B/MAX5093B), or is adjustable from 1.5V to 9V (MAX5092_) or 1.5V to 10V (MAX5093_).
9	BSOUT	Boost Regulator Output Voltage. Bypass BSOUT to the PGND_BST ground plane with a 22 μ F (low-ESR) aluminum electrolytic capacitor in parallel with a 1 μ F ceramic capacitor placed as close to the IC as possible. Connect BSFB directly to SGND to regulate the BOOST output to a fixed voltage of 7V for $V_{\text{IN}} \leq 7\text{V}$. V_{BSOUT} follows V_{IN} for $V_{\text{BSOUT}} - V_{\text{OUT}} > 2.5\text{V}$ (typ). V_{BSOUT} is programmable up to 11V (MAX5092_) or 12V (MAX5093_) by connecting BSFB to the center tap of an external resistor-divider connected between the BOOST output and PGND_BST.
10, 11	LX	Inductor Connection to the Drain of the Internal Power MOSFET. Connect LX to the switched side of the inductor. Connect pins 10 and 11 together as close to the device as possible. For the MAX5093, also connect LX to the anode of the external Schottky diode.
12	PGND_BST	Boost Regulator Power Ground. Connect PGND_BST to the power ground plane. Connect the PGND_BST ground plane and the signal ground plane together at the negative terminal of the input capacitor(s).
13	BSFB	Feedback Input for the Boost Regulator. Connect BSFB directly to SGND to set the boost regulator output voltage to 7V. Connect BSFB to the center tap of an external resistor-divider connected between BSOUT and SGND to set the output voltage. V_{BSFB} regulates to 1.24V when using an adjustable output.
14	VL	Internal Regulator Output for IC Supply. Bypass VL to SGND with a 1 μ F/6.3V ceramic capacitor placed as close to the IC as possible. V_{VL} regulates to 5.5V with $V_{\text{BSOUT}} \geq 5.5\text{V}$.
15	CT	$\overline{\text{RESET}}$ Timeout Programming Input. Connect a capacitor from CT to SGND to set the $\overline{\text{RESET}}$ timeout period. See the <i>CT Capacitor Selection</i> section.
16	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ Output. $\overline{\text{RESET}}$ is an open-drain output that goes high impedance when V_{OUT} exceeds 92% of the output voltage threshold after a programmed time delay. $\overline{\text{RESET}}$ pulls low immediately once V_{OUT} drops below 90% of the regulated LDO output voltage.
—	EP	Exposed Paddle. Connect to the signal ground plane (SGND). Connect to a large-signal ground plane for increased thermal performance.

Functional Diagrams

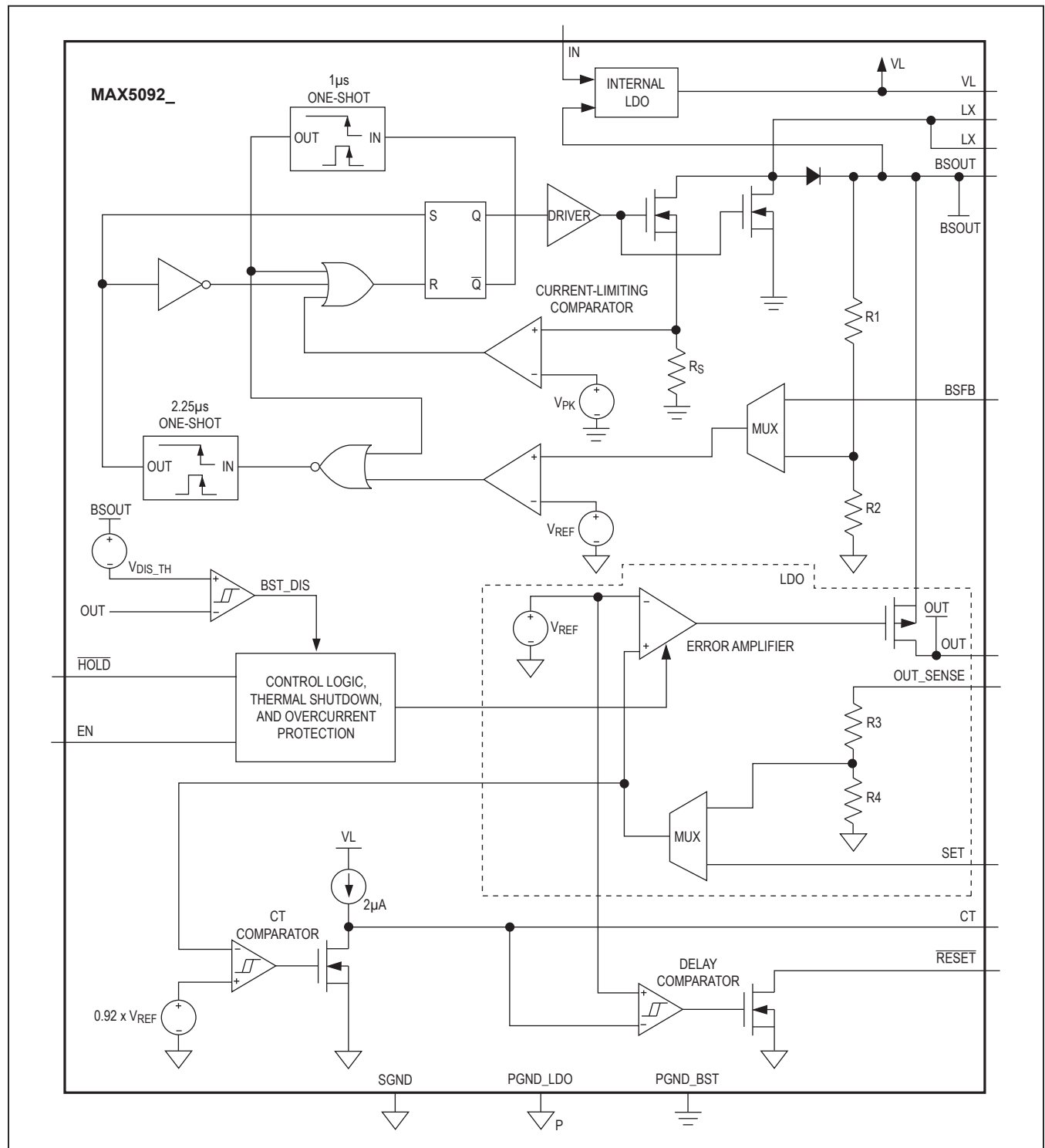


Figure 1. MAX5092_ Functional Diagram

Functional Diagrams (continued)

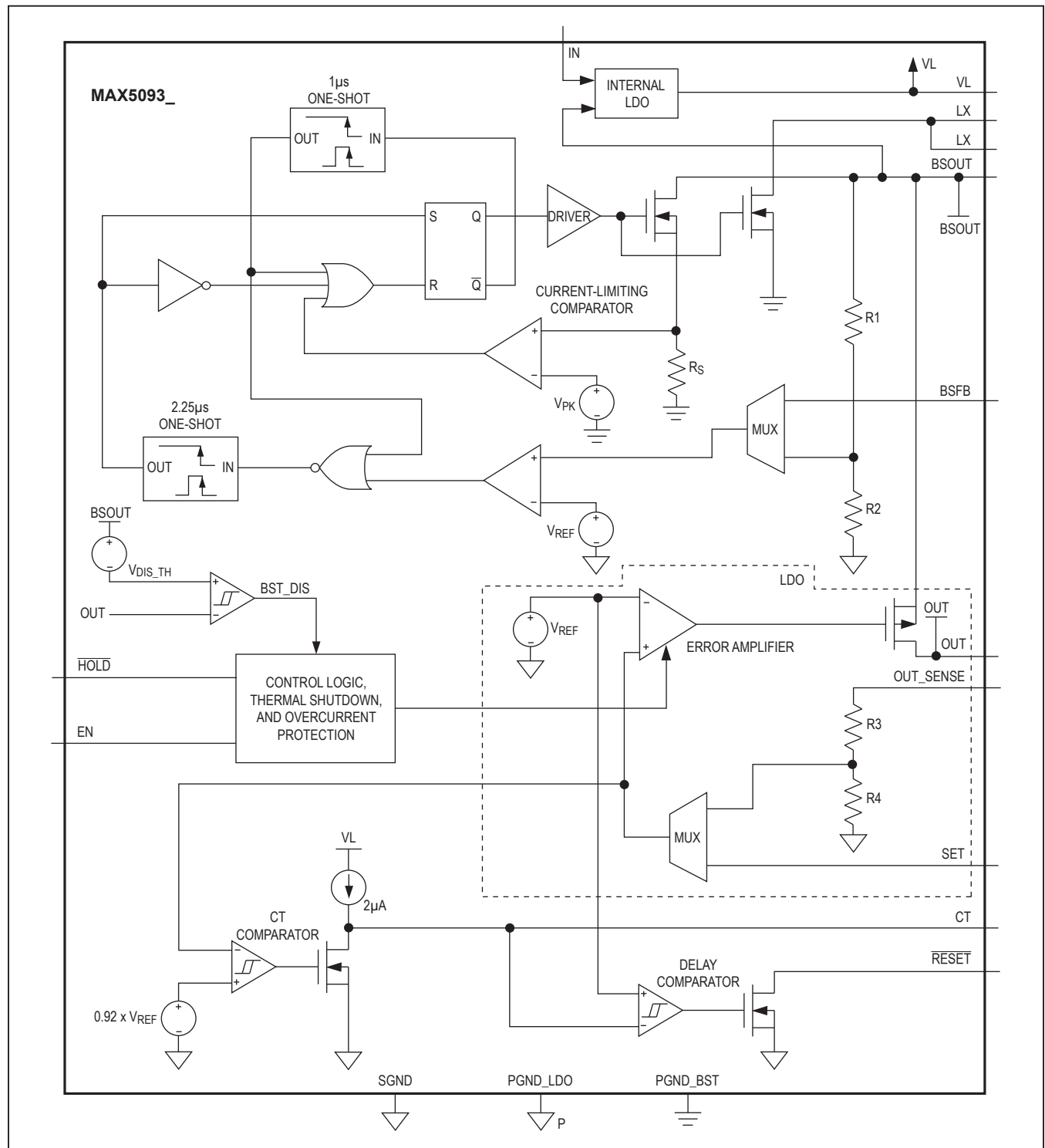


Figure 2. MAX5093_ Functional Diagram

Detailed Description

The MAX5092A/MAX5092B/MAX5093A/MAX5093B include a step-up, switch-mode DC-DC converter and a linear regulator to provide step-up/-down voltage conversion over a wide range of input voltages. This combination of an LDO and a boost converter offers the advantage of using a single off-the-shelf inductor in place of the multiple-winding custom magnetics needed in typical SEPIC or transformer-based flyback topologies. The boost preregulator is completely turned off during normal operation ($V_{IN} = 14V$), reduces quiescent current to 65 μA (typ), and makes the devices suitable for always-on power supplies.

The devices have an internal UVLO threshold of 3.8V (max, V_{IN} rising) that must be exceeded before the device is enabled. When V_{IN} is above V_{UVLO} , the internal boost converter starts switching and regulates V_{BSOUT} to the programmed boost output voltage. The low quiescent-current LDO steps down V_{BSOUT} to the programmed LDO output voltage. The LDO output is preset to 3.3V (MAX5092A/MAX5093A) or 5V (MAX5092B/MAX5093B). Both output voltages can be adjusted by using external resistor-dividers.

If ($V_{BSOUT} - V_{OUT}$) rises above 2.5V (typ), the boost converter is disabled, forcing V_{BSOUT} to follow V_{IN} . If $V_{BSOUT} - V_{OUT}$ falls below 2V (typ), the boost converter starts switching and regulates V_{BSOUT} to the programmed voltage. The boost converter regulates V_{BSOUT} for V_{IN} down to 3.5V, providing uninterrupted operation during low cold-crank voltages even if the programmed LDO output voltage is greater than V_{IN} (but less than 9V). The boost converter turn-on response time is less than 10 μs , making cold-crank input glitches transparent to the system even at full load.

The boost-converter output is followed by a high PSRR, low-quiescent-current LDO. The LDO rejects the switching noise present at BSOUT and provides a clean, regulated output voltage. The linear regulator uses an internal p-channel MOSFET pass element. Additional features include a power-on-reset function with an externally adjustable timeout, an enable (EN) input, and a hold (HOLD) regulator control input.

Boost Converter

The switch-mode converter uses a minimum off-time, maximum on-time pulse frequency modulation (PFM) control scheme. The internal MOSFET turns on whenever V_{BSOUT} falls below the regulation point determined by V_{BSFB} (see the *Setting the Boost Output Voltage* (V_{BSOUT}) section). The MOSFET turns off when the

inductor current reaches the peak current limit (2.5A typ) or after 2.25 μs maximum on-time, whichever occurs first. The MOSFET is held off for at least 1 μs after the turn-on phase. A new switching cycle initiates once V_{BSOUT} falls below the threshold. In this control scheme, switching frequency and output ripple are functions of load current and input voltage. No frequency compensation is needed in the PFM control scheme.

The output of the boost converter is preset to 7V and is adjustable by using external resistors. See the *Setting the Boost Output Voltage* V_{BSOUT} section.

If V_{BSOUT} is programmed greater than ($V_{OUT} + V_{BST_DIS}$), larger ripple is observed on BSOUT. The reason is as V_{BSOUT} rises above $V_{OUT} + V_{BST_DIS}$, the boost converter is disabled, causing V_{BSOUT} to fall. As V_{BSOUT} falls to $V_{OUT} + V_{BST_EN}$, the boost converter turns back on, and V_{BSOUT} rises. For the lowest V_{BSOUT} ripple, program V_{BSOUT} within the boost disable threshold. See the *Typical Operating Characteristics* for the Switching Waveforms.

Due to the integrated blocking diode in the MAX5092_, V_{BSOUT} is limited to 11V. Use the MAX5093_ for higher boost output voltages (or to reduce the power dissipation in to the package). The MAX5093_ requires an external diode for the boost converter. Select the external diode according to the *Schottky Diode Selection* (MAX5093_) section.

Linear Regulator

The MAX5092_/MAX5093_ contain an internal p-channel MOSFET used as the pass transistor for the LDO. The output of the boost regulator is connected to the source of the p-MOSFET. The LDO starts up 200 μs after the boost regulator starts up. The LDO supplies up to 250mA with a typical dropout voltage of 0.9V. The maximum LDO output current is determined by the package power-dissipation limit as well as the internal current limit. The LDO is designed to be a low-quiescent-current type. During normal operation when the battery voltage is > 9V, the MAX5092_/MAX5093_ consume only 75 μA (max) at +85°C and 100 μA load.

The output voltage of the LDO is set using the SET input. Connect SET to SGND to use the factory-preset output voltage. Connect SET to the center of an external resistor-divider connected from OUT to SGND to program a different output voltage. See the *Setting the LDO Output Voltage* (V_{OUT}) section.

Internal Regulator (VL)

An internal regulator (VL) is used to supply all internal low-voltage blocks. Bypass VL to SGND with a 1µF ceramic capacitor placed as close to the IC as possible. V_{VL} regulates to 5.5V when V_{BSOUT} is above 5.5V. V_{VL} tracks the voltage at BSOUT when V_{BSOUT} is below 5.5V.

Power-On-Reset Output ($\overline{\text{RESET}}$)

The MAX5092_/MAX5093_ contain an open-drain output ($\overline{\text{RESET}}$) that indicates when the LDO output (V_{OUT}) is out of regulation. If the output of the LDO falls below 90% of the nominal output voltage, $\overline{\text{RESET}}$ pulls low after a short delay. Once the output rises above 92% of the nominal output voltage, $\overline{\text{RESET}}$ goes high impedance after the programmed reset timeout period. Connect a 100kΩ pullup resistor from OUT to $\overline{\text{RESET}}$. See the *CT Capacitor Selection* section for details on setting the RESET timeout period.

Enable and Hold Inputs

The MAX5092_/MAX5093_ utilize two logic inputs, EN (active-high) and $\overline{\text{HOLD}}$ (active low), to implement a self-holding circuit with no additional components. For example, an ignition switch drives EN high and the regulator turns on. If $\overline{\text{HOLD}}$ is then driven low, the regulator remains on even if EN goes low. As long as $\overline{\text{HOLD}}$ is forced low and remains low after initial regulator power-up, the regulator remains on. From this state, release $\overline{\text{HOLD}}$ (an internal current source connects $\overline{\text{HOLD}}$ to OUT), or connect $\overline{\text{HOLD}}$ to OUT to turn the regulator off. Drive EN low and $\overline{\text{HOLD}}$ high to place the IC into shutdown mode. Shutdown mode reduces supply current to 5µA. Figure 3 shows the timing diagram for the enable and hold functions. Table 1 shows the state of the regulator output with respect to the voltage level at EN and $\overline{\text{HOLD}}$ with reference to Figure 3. Connect $\overline{\text{HOLD}}$ to OUT or leave unconnected to disable the hold feature and use EN as a standard on/off control input.

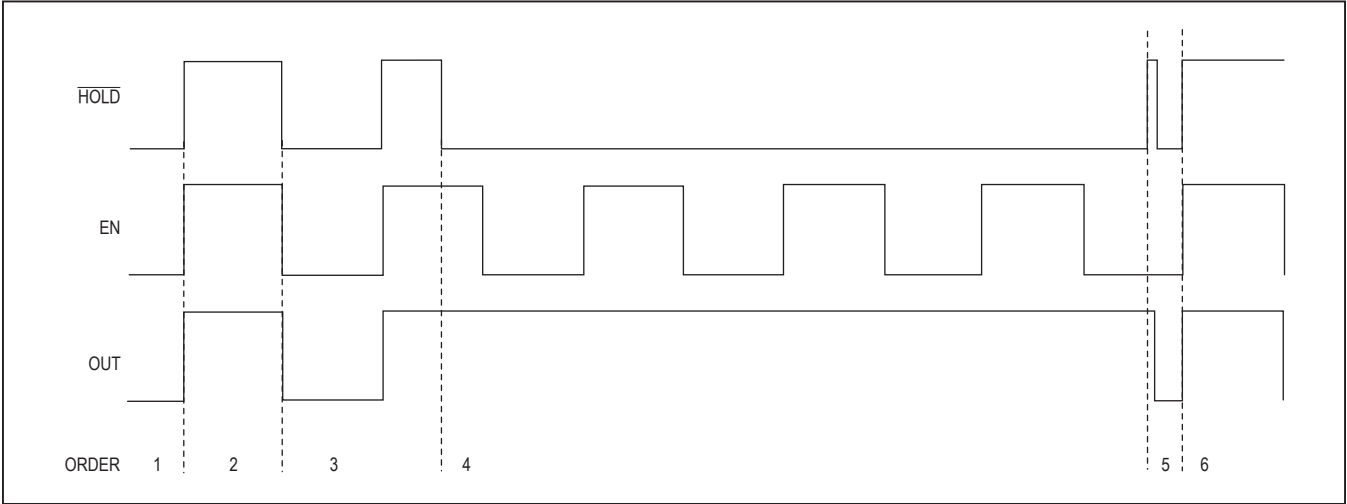


Figure 3. Enable and Hold Timing Diagram

Table 1. Truth Table for Enable and Hold Timing Diagram

ORDER	EN	$\overline{\text{HOLD}}$	OUT	COMMENTS
1	Low	X	Off	Initial State. EN has a 500nA pulldown to GND. $\overline{\text{HOLD}}$ has an internal current source to OUT. $\overline{\text{HOLD}}$ follows OUT.
2	High	Released	On	Regulator output is active when EN is pulled high. $\overline{\text{HOLD}}$ is in release state, and it follows OUT.
3	Low	Released	Off	$\overline{\text{HOLD}}$ is in release state. OUT follows EN.
4	High	Low	On	$\overline{\text{HOLD}}$ is pulled low externally after OUT turns on. The regulator output is forced on regardless of the state of EN. A self-holding state.
5	Low	Released	Off	$\overline{\text{HOLD}}$ is released after EN is pulled low. Output turns off.
5	High	X	On	Regulator enabled. Normal turn-on behavior. Regulator follows EN and $\overline{\text{HOLD}}$ follows OUT.

The schematic diagram illustrates the MAX5092B circuit. The input section (pins 1, 10, 11) includes an input voltage range of 4V to 72V, a 4.7μH inductor (L1), and two capacitors (C1* = 47μF, C2* = 1μF) connected to pins 1 and 11. The output section (pins 14, 9, 12, 13, 4, 7, 8, 5, 6) features a 1μF capacitor (C6) on pin 14, a 7V reference on pin 9, a 1μF capacitor (C3*) and a 22μF capacitor (C4*) on pins 12 and 13, a μP signal on pin 4, an output sense signal on pin 7, an output voltage of 5V at 250mA** on pin 8, a 10μF capacitor (C7) on pin 5, and a power ground (PGND) on pin 6. The control section (pins 16, 2, 3, 15) includes a 100kΩ resistor (R1) connected to pins 16 and 2, an ON/OFF control signal on pin 2, a signal ground (SGND) on pin 3, and a 0.22μF capacitor (C5) on pin 15. The MAX5092B chip (U1) is shown with its internal components and connections.

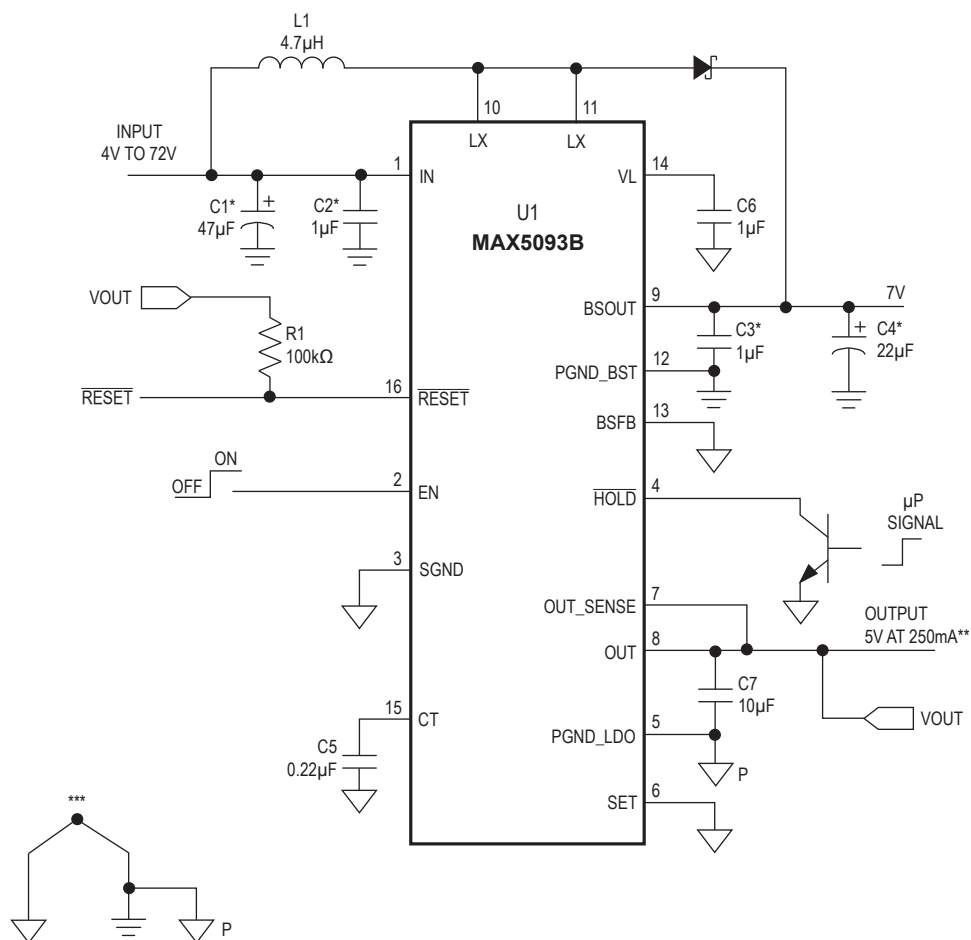
***THESE CAPACITORS MUST BE RATED AT THE HIGHEST V_{IN} VOLTAGE.

**OUTPUT CURRENT IS LIMITED BY THE TOTAL POWER-DISSIPATION CAPABILITY OF THE PACKAGE.

***SEE *PCB LAYOUT GUIDELINES* SECTION.

Figure 4. MAX5092B Typical Application Circuit with Factory Preprogrammed LDO and Boost Output Voltages

Applications Information Diagrams (continued)



*THESE CAPACITORS MUST BE RATED AT THE HIGHEST V_{IN} VOLTAGE.

**OUTPUT CURRENT IS LIMITED BY THE TOTAL POWER-DISSIPATION CAPABILITY OF THE PACKAGE.

***SEE PCB LAYOUT GUIDELINES SECTION.

Figure 5. MAX5093B Typical Application Circuit with Factory Preprogrammed Boost and LDO Output Voltages

The schematic diagram illustrates the MAX5092A circuit configuration. The input stage features an IN pin connected to a 4V TO 72V source through a 4.7μH inductor (L1) and a 47μF capacitor (C1*). A 1μF capacitor (C2*) is connected between the IN pin and ground. The control stage includes an EN pin connected to an ON/OFF switch, a RESET pin connected to a 100kΩ resistor (R3) and a RESET signal, and a CT pin connected to a 0.22μF capacitor (C5). The output stage consists of a VL pin connected to a 5.5V source through a 1μF capacitor (C6), a BSOUT pin connected to a 5.3V source through a 1μF capacitor (C3*), a PGND_BST pin connected to ground, a BSFB pin connected to a 1.65MΩ resistor (R1) and a 499kΩ resistor (R2), a HOLD pin connected to a μP SIGNAL, an OUT_SENSE pin connected to a VOUT node, an OUT pin connected to a 3.3V** output through a 10μF capacitor (C7), a PGND_LDO pin connected to ground, and a SET pin connected to ground. A note at the bottom states: ***SEE PCB LAYOUT GUIDELINES SECTION.

Figure 6. MAX592A Typical Application Circuit with User-Programmed LDO and Boost Output Voltages

***THESE CAPACITORS MUST BE RATED AT THE HIGHEST V_{IN} VOLTAGE.

**OUTPUT CURRENT IS LIMITED BY THE TOTAL OUTPUT POWER AND THE DISSIPATION CAPABILITY OF THE PACKAGE.

***SEE PCB LAYOUT GUIDELINES SECTION.

Figure 7. MAX593A Typical Application Circuit with User-Programmable Boost Output Voltage and LDO Output Voltage

Design Guidelines

Input Capacitor (C_{IN}) and Boost Capacitor (C_{BSOUT}) Selection

The input current waveform of the boost converter is continuous, and usually does not demand high capacitance at its input. However, the MAX5092/MAX5093 boost converter is designed to fully turn on as soon as the input drops below a certain voltage in order to ride out cold-crank droops. This operation demands low input source impedance for proper operation. If the source (battery) is located far from the IC, high-capacity, low-ESR capacitors are recommended for C_{IN} . The worst-case peak capacitor current could be as high as 3A. Use a 47 μ F, 100m Ω low-ESR capacitor placed as close as possible to the input of the device. Note that the aluminum electrolytic capacitor ESR increases significantly at cold temperatures. In the cold temperature case, choose an electrolyte capacitor with ESR lower than 40m Ω or connect a low-ESR ceramic capacitor (10 μ F) in parallel with the electrolytic capacitor.

The boost converter output (BSOUT) is fed to the input of the internal 250mA LDO. The boost-converter output current waveform is discontinuous and requires high-capacity, low-ESR capacitors at BSOUT to ensure low V_{BSOUT} ripple. During the on-time of the internal MOSFET, the BSOUT capacitor supplies 250mA current to the LDO input. During the off-time, the inductor dumps current into the output capacitor while supplying the output load current. The internal 250mA LDO is designed with high PSRR; however, high-frequency spikes may not be rejected by the LDO. Thus, high-value, low-ESR electrolytic capacitors are recommended for C_{BSOUT} . Peak-to-peak V_{BSOUT} ripple depends on the ESR of the electrolyte capacitor. Use the following equation to calculate the required ESR (ESR_{BSOUT}) of the BSOUT capacitor:

$$ESR_{BSOUT} = \frac{\Delta V_{ESRBS}}{I_{LIM} - I_{OUT}}$$

where ΔV_{ESRBS} is 75% of total peak-to-peak ripple at BSOUT, I_{LIM} is the internal switch current limit (3A max), and I_{OUT} is the LDO output current. Use a 100m Ω or lower ESR electrolytic capacitor. Make sure the ESR at cold temperatures does not cause excessive ripple voltage. Alternately, use a 10 μ F ceramic capacitor in parallel with the electrolyte capacitor.

During the switch on-time, the BSOUT capacitor discharges while supplying I_{OUT} . The ripple caused by the capacitor discharge (ΔV_{CBS}) is estimated by using the following equation:

$$\Delta V_{CBS} = \frac{I_{OUT} \times 2.7 \times 10^{-6}}{C_{BSOUT}}$$

where I_{OUT} is the LDO output current and C_{BSOUT} is the BSOUT capacitance.

Inductor Selection

The control scheme of the MAX5092/MAX5093 permits flexibility in choosing an inductor value. Smaller inductance values typically offer smaller physical size for a given series resistance, allowing the smallest overall circuit dimensions. Circuits using larger inductance may provide higher efficiency and exhibit less ripple, but also may reduce the maximum output current. This occurs when the inductance is sufficiently large to prevent the LX current limit (I_{LIM}) from being reached before the maximum on-time (t_{ON-MAX}) expires.

For maximum output current, choose the inductor value so that the controller reaches the current limit before the maximum on-time is reached:

$$L \leq \frac{V_{IN} \times t_{ON-MAX}}{I_{LIM}}$$

where t_{ON-MAX} is typically 2.25 μ s, and the current limit (I_{LIM}) is a maximum of 3A (see the *Electrical Characteristics*). Choose an inductor with the maximum saturation current (I_{SAT}) greater than 3A.

Setting the Boost Output Voltage (V_{BSOUT})

The MAX5092_/MAX5093_ feature Dual Mode™ operation for the internal boost converter output voltage. These devices operate in a preset output-voltage mode or an adjustable output-voltage mode. In preset mode, internal trimmed feedback resistors set V_{BSOUT} to a fixed 7V. Select the preset mode by directly connecting BSFB to SGND (Figures 4 and 5). Ensure a low-impedance path between BSFB and SGND to limit the transient at BSFB to below 100mV. In adjustable mode, connect BSFB to the center tap of an external resistor-divider connected between BSOUT and SGND to program V_{BSOUT} (Figures 6 and 7). Program ($V_{BSOUT} < V_{OUT} + V_{BST_DIS}$) for lower V_{BSOUT} ripple. Note that the current drawn by the resistor-divider at BSOUT adds to the quiescent current and the shutdown current of the IC. Use the resistor-divider only if V_{BSOUT} is required to be significantly different than 7V. Select 499kΩ or lower resistance value for the bottom resistor (R2) of the divider connected to SGND. The top resistor (R1) value is calculated as:

$$R1 = R2 \times \left(\frac{V_{BSOUT}}{V_{BSFB}} - 1 \right)$$

where V_{BSFB} is the regulation voltage at BSFB (1.24V typ) and V_{BSOUT} is the desired output voltage for BSOUT.

Setting the LDO Output Voltage (V_{OUT})

The LDO output voltage is also Dual Mode (preset and adjustable). Preset mode is selected by connecting SET to SGND (Figures 4 and 5). In preset mode, V_{OUT} regulates to 3.3V (MAX5092A/MAX5093A) or 5V (MAX5092B/MAX5093B) by internal trimmed feedback resistors. Adjustable mode is selected by connecting SET to the center tap of an external resistor-divider connected between OUT and SGND (Figures 6 and 7). Note that the current drawn by the resistor-divider at OUT adds to the quiescent current of the LDO. Use the resistor-divider only if V_{OUT} is required to be significantly different than the preset voltage. Select 100kΩ or lower value for the bottom resistor (R5) of the divider connected to SGND. The top resistor (R4) value is calculated as:

$$R4 = R5 \times \left(\frac{V_{OUT}}{V_{SET}} - 1 \right)$$

where V_{SET} is the regulation voltage at SET (1.24V typ) and V_{OUT} is the desired output voltage for the LDO output.

Schottky Diode Selection (MAX5093_)

The MAX5093_ requires an external diode connected between LX and BSOUT (Figures 5 and 7). Proper selection of an external diode can offer a lower forward-voltage drop and a higher reverse-voltage handling capability. Since the high switching frequency of the IC demands a high-speed rectifier, Schottky diodes are recommended for most applications because of their fast recovery time and low forward-voltage drop. Ensure that the diode's peak current rating is greater than or equal to the peak current limit of internal boost converter MOSFET. A diode average forward current rating of at least 1A is recommended. Additionally, the diode reverse breakdown voltage must be greater than the worst-case load-dump-condition voltage.

CT Capacitor Selection

The MAX5092_/MAX5093_ contain an open-drain power-on-reset output (RESET) that indicates when the LDO output voltage (V_{OUT}) is out of regulation. When V_{OUT} rises above 92% of the nominal output voltage, RESET goes high impedance after a user-programmable time delay. This time duration is programmable by a capacitor (C_{CT}) from CT to SGND (Figures 4–7). For a chosen RESET active timeout period (t_{DELAY}), calculate the required capacitor value as:

$$C_{CT} = \frac{2 \times 10^{-6} \times t_{DELAY}}{1.24}$$

When V_{OUT} drops below 90% of the LDO output regulation voltage, a 5mA pulldown current from CT to SGND discharges C_{CT} . The time required to discharge CT determines the delay necessary to pull RESET low. This delay provides glitch immunity to the RESET function. The glitch immunity delay is directly proportional to the CT capacitor and is approximately 70μs for a 0.1μF capacitor at CT.

Dual Mode is a trademark of Maxim Integrated Products, Inc.

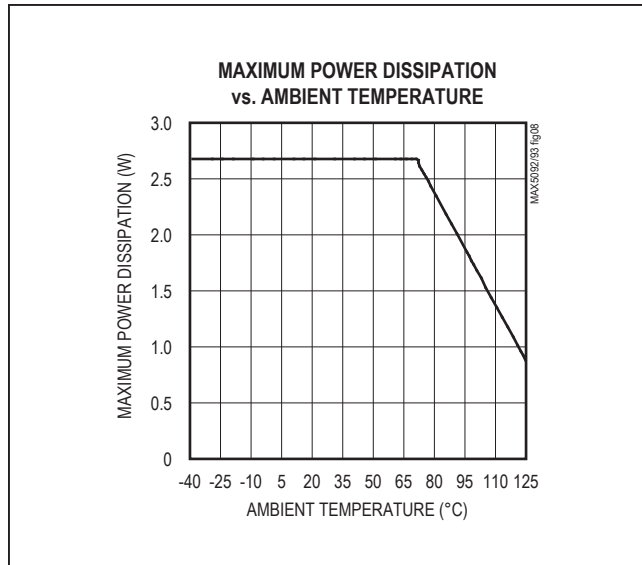


Figure 8. MAX5092/MAX5093 Package Power Dissipation

Maximum Output Current (I_{OUT_MAX})

The MAX5092/MAX5093 high input voltage (+72V max) provides up to 250mA of current from OUT. Package power-dissipation limits the amount of output current available for a given input/output voltage and ambient temperature. Figure 8 depicts the maximum power-dissipation curve for the devices. The graph assumes that the exposed metal pad of the IC package is soldered to the PCB copper according to the JEDEC 51 standard (multilayer board). Use Figure 8 to determine the allowable package dissipation for a given ambient temperature. Alternately, use the following formula to calculate the allowable package dissipation (P_{DISS}) in watts:

For $T_A \leq +70^\circ\text{C}$:

$$P_{DISS} = 2.67$$

For $+70^\circ\text{C} < T_A \leq +125^\circ\text{C}$:

$$P_{DISS} = 2.67 - (0.0333 \times (T_A - 70))$$

where $+70^\circ\text{C} < T_A \leq +125^\circ\text{C}$ and $0.0333\text{W}/^\circ\text{C}$ is the package thermal derating. After determining the allowable package dissipation, calculate the maximum output current (I_{OUT_MAX}) using the following formula:

$$I_{OUT_MAX} = \frac{P_{DISS} - P_{LOSS(BST)}}{V_{IN} - V_{OUT}}$$

where P_{DISS} is the allowable package power dissipation and $P_{LOSS(BST)}$ is the boost converter power loss.

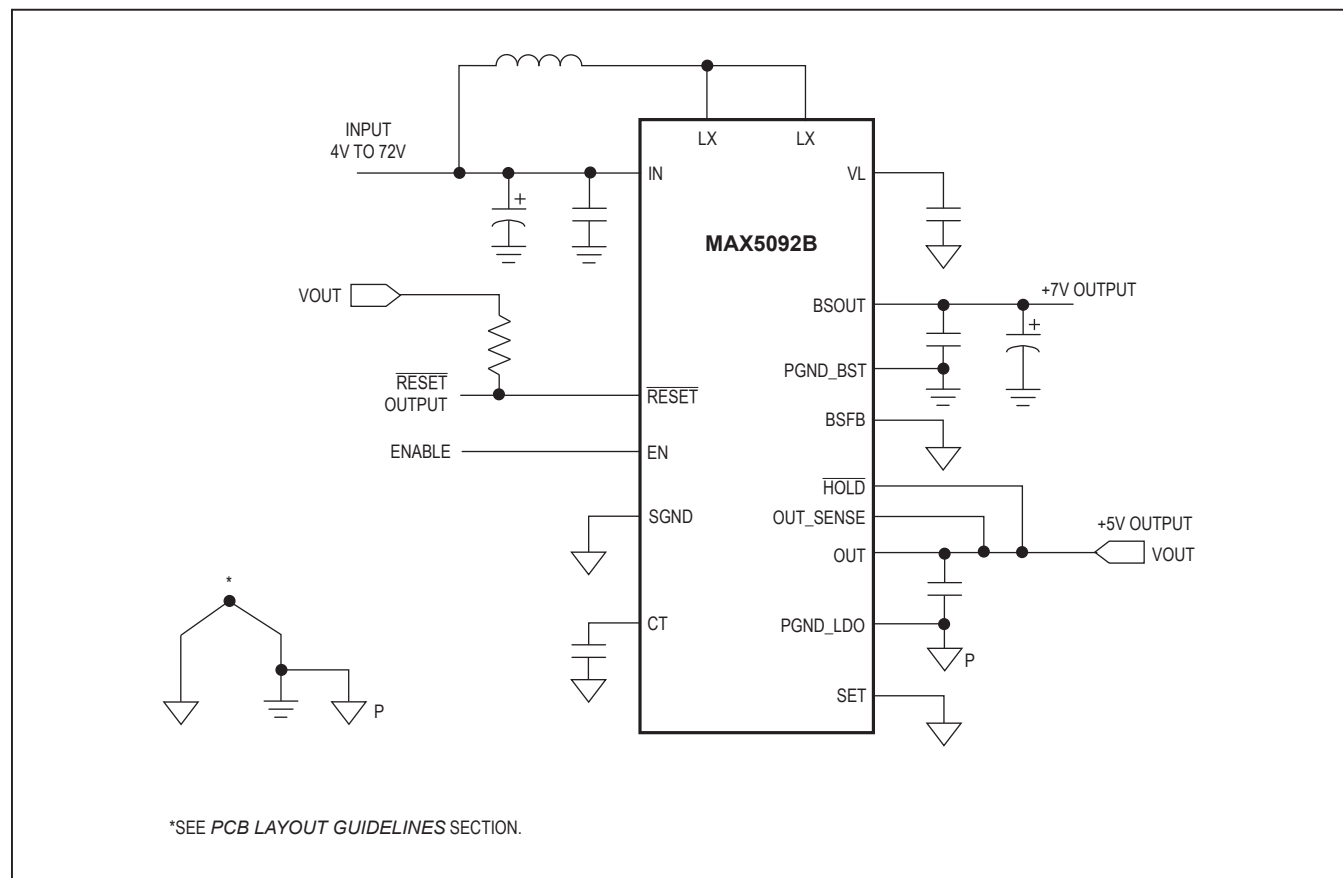
P_{DISS} includes the losses in the boost converter operation and the LDO itself. The boost converter loss $P_{LOSS(BST)}$, depends on V_{IN} , V_{BSOUT} , and I_{OUT} . See the Boost Converter Power Loss graphs in the *Typical Operating Characteristics* to estimate the losses at a given V_{IN} and V_{BSOUT} at room temperature. At a higher ambient temperature of $+105^\circ\text{C}$, $P_{LOSS(BST)}$ increases by up to 20% due to higher R_{DS-ON} and switching losses of the internal boost converter MOSFET. (Note: I_{OUT_MAX} must be less than 250mA).

PCB Layout Guidelines

Good PCB layout and routing are required in high-frequency switching power supplies to achieve proper regulation and stability. It is strongly recommended that the evaluation kit PCB layouts be followed as closely as possible. Refer to the MAX5092 EV kit for an example layout. Follow these guidelines for good PCB layout:

- 1) For SGND, use a large copper plane under the IC and solder it to the exposed paddle. To effectively use this copper area as a heat exchanger between the PCB and ambient, expose this copper area on the top and bottom side of the PCB. Do not make a direct connection from the EP copper plane to pin 3 (SGND) underneath the IC so as to minimize ground bounce.
- 2) Isolate the power components and high-current path from the sensitive analog circuit.
- 3) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- 4) Connect the return terminals of input capacitors and boost output capacitors to the PGND_BST power ground plane. Connect the power ground (PGND_BST) and signal ground (SGND) planes together at the negative terminal of the input capacitors. Do not connect them anywhere else. Connect PGND_LDO ground plane to SGND ground plane at a single point.
- 5) Ensure that the feedback connections are short and direct. Ensure a low-impedance path between BSFB and SGND to limit the transient at BSFB to 100mV.
- 6) Route high-speed switching nodes away from the sensitive analog areas. Use the internal PCB layer for SGND as an EMI shield to keep radiated noise away from the IC, feedback dividers, and bypass capacitors.

Typical Operating Circuit



Selector Guide

PART	PRESET LDO OUTPUT (V)	ADJUSTABLE LDO OUTPUT	PRESET BSOUT OUTPUT (V)	ADJUSTABLE BSOUT OUTPUT	BOOST DIODE
MAX5092AATE+	3.3	Yes	7	Yes	Internal
MAX5092BATE+	5	Yes	7	Yes	Internal
MAX5093AATE+	3.3	Yes	7	Yes	External
MAX5093BATE+	5	Yes	7	Yes	External

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1655+3	21-0140	90-0073

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/06	Initial release	—
1	1/08	Updated <i>Ordering Information</i> and <i>Electrical Characteristics</i> table, added two <i>Typical Operating Characteristics</i> graphs, updated <i>Functional Diagrams</i> and <i>Applications Information Diagrams</i> , added boost converter details	1–12, 14–17, 19, 22, 23
2	10/14	Removed automotive references from the <i>General Description</i> , <i>Applications</i> , <i>Detailed Description</i> , and <i>Enable and Hold Inputs</i> sections	1, 12, 13

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