Quad, High-Speed HDMI/DVI 2:1 Digital Video Switch

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{DD} .....-0.3V to +4V
SEL (Note 1) .....-0.3V to (V_{DD} + 0.3V)
COM_, NC_, NO_ .....-0.3V to (V_{DD} + 0.3V)
Continuous Current Through Any Switch .....±120mA
Peak Current Through Any Switches
(Pulsed at 1ms, 10% duty cycle).....±240mA

Continuous Power Dissipation (T_A = +70°C)
42-Pin Thin QFN-EP (derate 35.7mW/°C above +70°C).....2857.1mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Signal exceeding V_{DD} or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3.0V to +3.6V, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}			3.0		3.6	V
Quiescent Supply Current	I_{DD}	+3V ≤ V_{DD} ≤ +3.6V; SEL = 0V or V_{DD}			600	1100	µA
ANALOG SWITCH							
On-Resistance (Note 3)	R_{ON}	V_{DD} = +3V, 0V ≤ $V_{COM\_}$ ≤ V_{DD}, $I_{COM\_}$ = -40mA	T_A = +25°C		8	11	Ω
			T_A = T_{MIN} to T_{MAX}			15	
		V_{DD} = +3V, $I_{COM\_}$ = -40mA, 0 ≤ $V_{COM\_}$ ≤ 1.5V	T_A = +25°C		8	11	
			T_A = T_{MIN} to T_{MAX}			15	
On-Resistance Matching (Notes 3, 4)	ΔR_{ON}	V_{DD} = +3V, 1.5V ≤ $V_{COM\_}$ ≤ V_{DD}, $I_{COM\_}$ = -40mA	T_A = +25°C		0.28	0.40	Ω
			T_A = T_{MIN} to T_{MAX}			0.8	
		V_{DD} = +3V, 0 ≤ $V_{COM\_}$ ≤ 1.5V, $I_{COM\_}$= -40mA	T_A = +25°C		0.28	0.40	
			T_A = T_{MIN} to T_{MAX}			0.8	
On-Resistance Flatness (Note 3)	$R_{FLAT(ON)}$	V_{DD} = +3V, $I_{COM\_}$ = -40mA, 1.5V < $V_{COM\_}$ < V_{DD}	T_A = +25°C		0.02	0.60	Ω
			T_A = T_{MIN} to T_{MAX}			1	
		V_{DD} = +3V, $I_{COM\_}$ = -40mA, 0 ≤ $V_{COM\_}$ ≤ 1.5V	T_A = +25°C		0.02	0.60	
			T_A = T_{MIN} to T_{MAX}			1	
Leakage Current	I_L	V_{DD} = +3.6V, $V_{COM\_}$ = +0.3V, +3.3V, $V_{NC\_}$ or $V_{NO\_}$ = +3.3V, 0.3V		-1		+1	µA
SWITCH DYNAMIC							
Off-Capacitance	C_{OFF}	f = 1MHz, $V_{COM\_}$ = $V_{NC\_}$ or $V_{NO\_}$			1.5		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3.0V to +3.6V, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
On-Capacitance	C_{ON}	f = 1MHz, $V_{COM\_}$ = $V_{NC\_}$ or $V_{NO\_}$		2.5		pF
Propagation Delay	t_{PD1}, t_{PD2}	R_S = R_L = 50Ω (Figure 2)		100		ps
Output Skew Between Ports	t_{SKEW1}	Skew between any two ports, R_S = R_L = 50Ω (Figure 3)		20		ps
Skew Between Same Ports	t_{SKEW2}	R_S = R_L = 50Ω, skew between any two ports (Figure 3)		20		ps
SWITCH AC PERFORMANCE						
On-Channel -3dB Bandwidth	BW	R_S = R_L = 50Ω (Figure 4)		2.6		GHz
Insertion Loss	I_{LOS}	R_S = R_L = 50Ω, f = 50MHz (Figure 4)		0.6		dB
Off-Isolation	V_{ISO}	R_S = R_L = 50Ω, single-ended, f = 50MHz (Figure 4)		-58		dB
Crosstalk	V_{CT1}	Crosstalk between any two switches, R_S = R_L = 50Ω, f = 50MHz (Figure 4)		-49		dB
LOGIC INPUTS (SEL)						
Input-Low Voltage	V_{IL}	V_{DD} = +3.0V			0.8	V
Input-High Voltage	V_{IH}	V_{DD} = +3.6V	2.0			V
Input-Voltage Hysteresis	V_{HYST}			100		mV
Input Leakage Current	I_{LEAK}	V_{DD} = +3.6V, $V_{COM\_}$ or $V_{NC\_}$ or $V_{NO\_}$ = 0V	-1		+1	µA

Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Device is production tested at T_A = +25°C.

Note 3: Negative current is going into COM_ and out of NO_ or NC_.

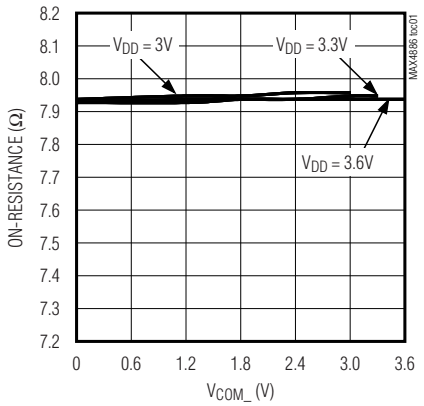
Note 4: Guaranteed by design.

Quad, High-Speed HDMI/DVI 2:1 Digital Video Switch

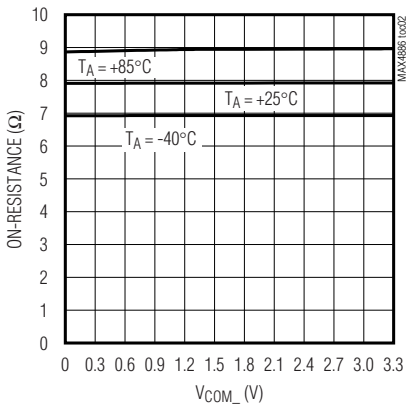
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

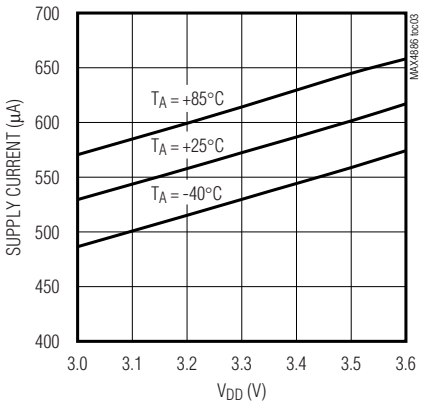
ON-RESISTANCE vs. $V_{COM\_}$



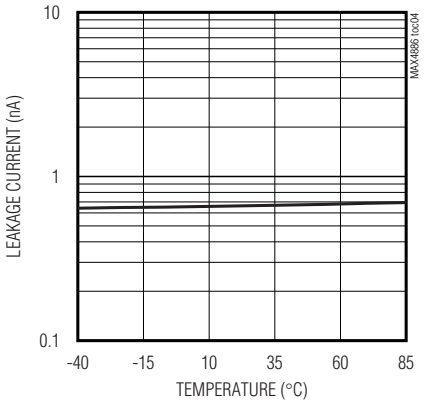
ON-RESISTANCE vs. TEMPERATURE



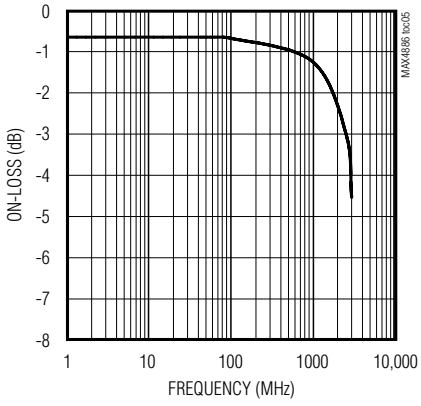
SUPPLY CURRENT vs. SUPPLY VOLTAGE



LEAKAGE CURRENT vs. TEMPERATURE



FREQUENCY RESPONSE

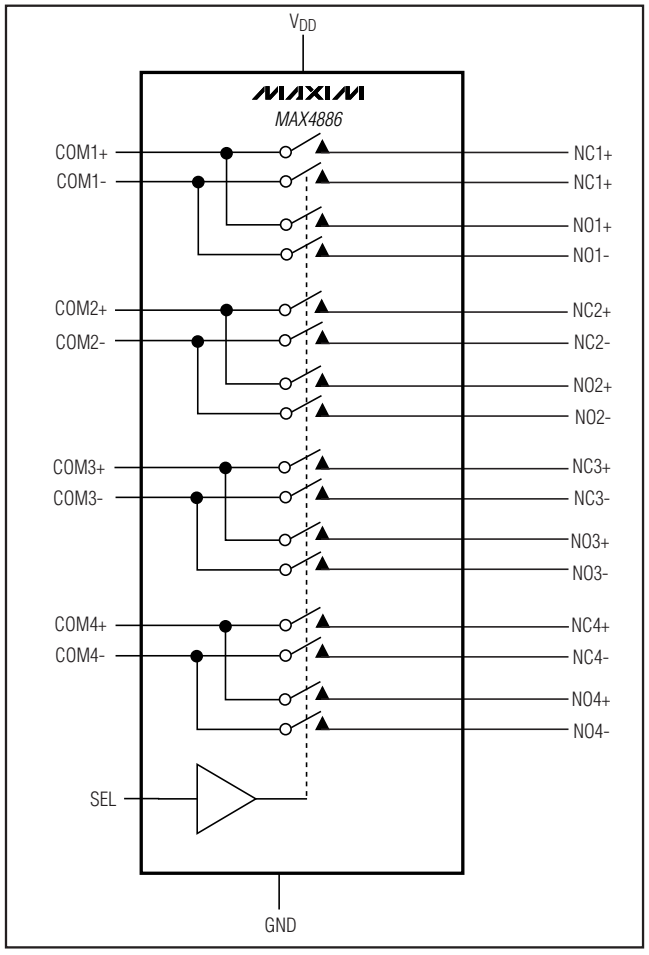


Pin Description

PIN	NAME	FUNCTION
1, 4, 10, 14, 17, 19, 21, 39, 41	GND	Ground
5, 8, 13, 18, 20, 30, 40, 42	V_{DD}	Power-Supply Voltage Input. Bypass V_{DD} to GND with a 0.1µF or larger ceramic capacitor.
2	COM1+	Data Signal Inputs/Outputs
3	COM1-	Data Signal Inputs/Outputs
6	COM2+	Data Signal Inputs/Outputs
7	COM2-	Data Signal Inputs/Outputs
9	SEL	Select Input. Logic input for switch connection (see Table 1).
11	COM3+	Data Signal Inputs/Outputs
12	COM3-	Data Signal Inputs/Outputs
15	COM4+	Data Signal Inputs/Outputs
16	COM4-	Data Signal Inputs/Outputs
22	NO4-	Differential Pair. Data Signal Inputs/Outputs.
23	NO4+	Differential Pair. Data Signal Inputs/Outputs.
24	NO3-	Differential Pair. Data Signal Inputs/Outputs.
25	NO3+	Differential Pair. Data Signal Inputs/Outputs.
26	NC4-	Differential Pair. Data Signal Inputs/Outputs.
27	NC4+	Differential Pair. Data Signal Inputs/Outputs.
28	NC3-	Differential Pair. Data Signal Inputs/Outputs.
29	NC3+	Differential Pair. Data Signal Inputs/Outputs.
31	NO2-	Differential Pair. Data Signal Inputs/Outputs.
32	NO2+	Differential Pair. Data Signal Inputs/Outputs.
33	NO1-	Differential Pair. Data Signal Inputs/Outputs.
34	NO1+	Differential Pair. Data Signal Inputs/Outputs.
35	NC2-	Differential Pair. Data Signal Inputs/Outputs.
36	NC2+	Differential Pair. Data Signal Inputs/Outputs.
37	NC1-	Differential Pair. Data Signal Inputs/Outputs.
38	NC1+	Differential Pair. Data Signal Inputs/Outputs.
EP	EP	Exposed Paddle. Connect EP to GND.

Quad, High-Speed HDMI/DVI 2:1 Digital Video Switch

Functional Diagram



Detailed Description

The MAX4886 high-speed analog switch is ideal for HDMI/DVI switching applications, permitting 2:1 or 1:2 switching. The MAX4886 contains four differential pairs for HDMI or DVI switching. The MAX4886 connects either one monitor to one of two digital video signals or one HDMI/DVI output to one of two connectors or loads.

The MAX4886 differential switches are based on an nFET architecture with an internal charge pump for gate overdrive. This advanced architecture results in an extremely low capacitance and on-resistance needed for an excellent returns loss.

The MAX4886 features an 8Ω (typ) on-resistance and 2.5pF on-capacitance switches for routing RGB and CLK video signals.

Table 1. Switch Truth Table

SEL	FUNCTION
0	COM_ to NC_
1	COM_ to NO_

The MAX4886 switches are identical, and any of the switches can be used to route RGB and CLK video signals.

The device will also be useful in other high-speed switching applications such as LVDS and LVPECL.

Analog-Signal Levels

Signal inputs over the full voltage range (0V to V_{DD}) are passed through the switch with minimal change in on-resistance (see the *Typical Operating Characteristics* section). The switches are bidirectional. Therefore, COM_, NC_, and NO_ can be either inputs or outputs.

Logic Inputs (SEL)

The MAX4886 has a logic input that controls the switch on/off function. Use SEL to switch COM_ to NO_ or COM_ to NC_. Table 1 and the *Functional Diagram* illustrate the MAX4886 Truth Table.

Applications Information

Power-Supply Bypassing and Sequencing

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence V_{DD} on first, followed by the switch inputs and the logic inputs. Bypass at least one V_{DD} input to ground with a 0.1µF capacitor as close to the device as possible. Use the smallest physical size possible for optimal performance.

It is also recommended to bypass more than one V_{DD} input. A good strategy is to bypass one V_{DD} input with a 0.1µF capacitor and at least a second V_{DD} input with a 1nF to 10nF capacitor. (Use 0603 or smaller physical size ceramic capacitor).

PC Board (PCB) Layout

High-speed switches such as the MAX4886 require proper PCB layout for optimum performance. Ensure that impedance-controlled PCB traces for high-speed signals are matched in length, and as short as possible. Connect the MAX4886 exposed paddle to a solid ground plane.

Timing Circuits/Timing Diagrams

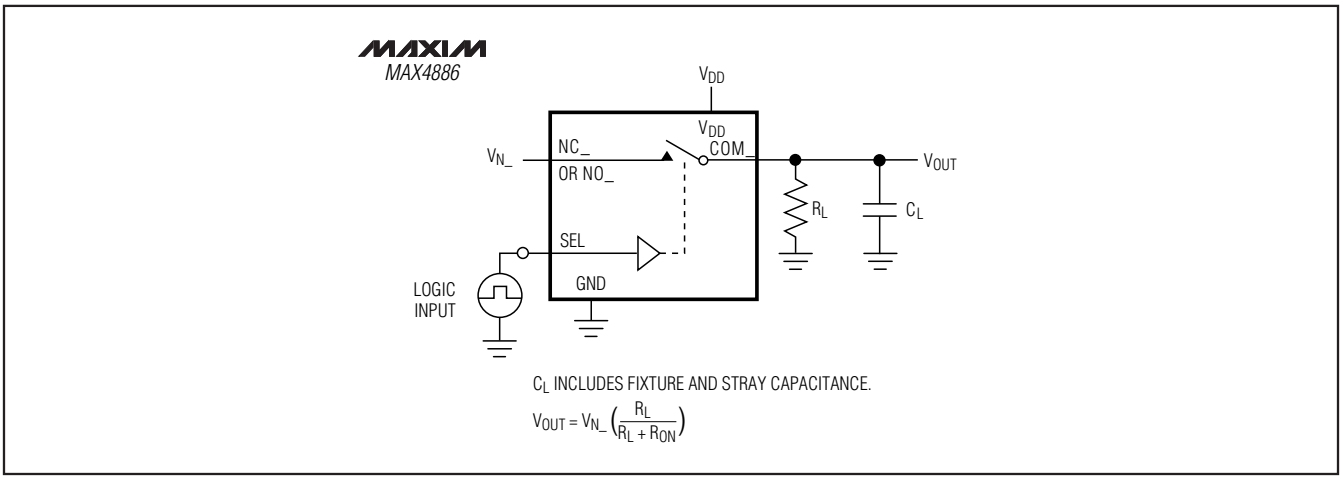


Figure 1. Switching Time

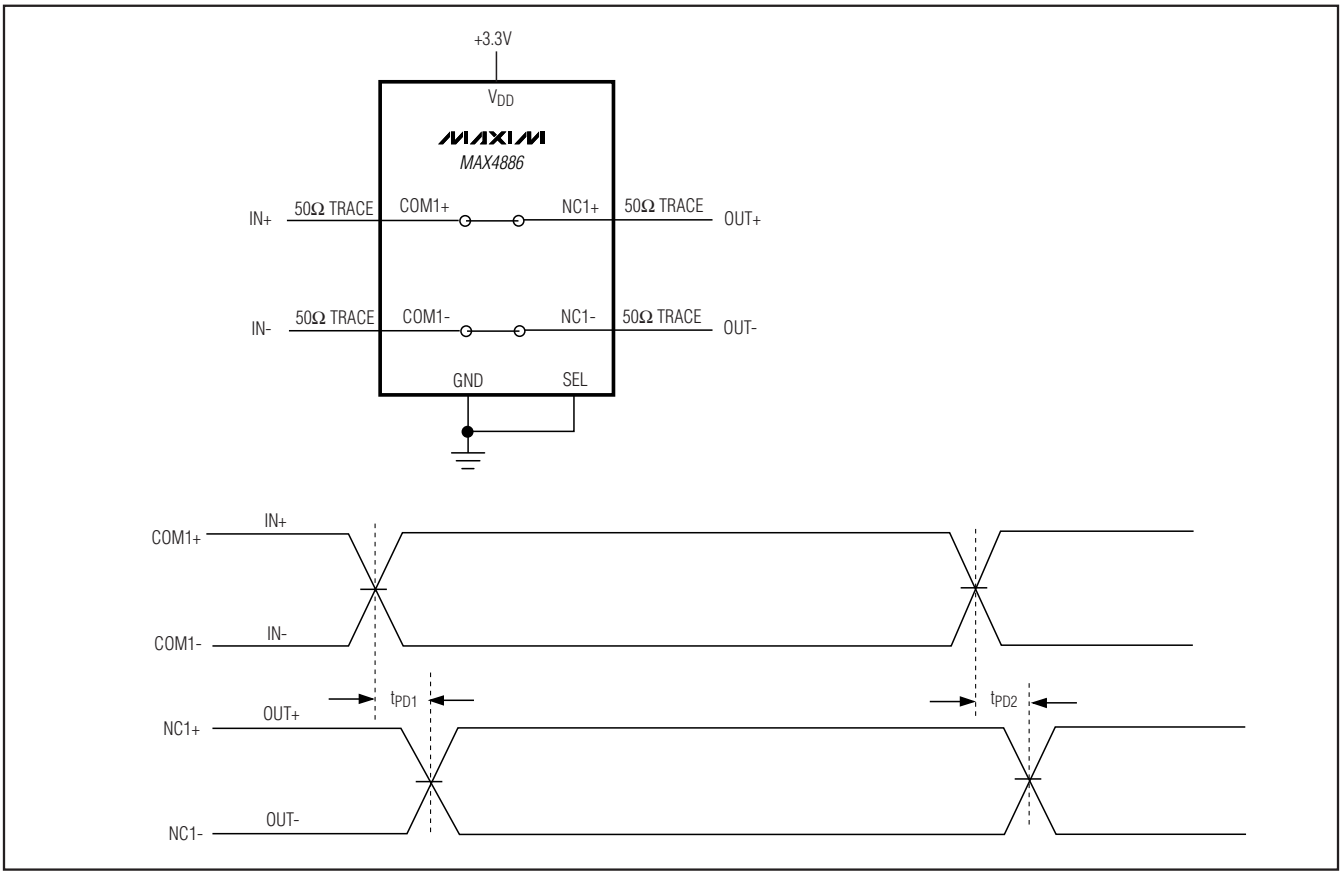


Figure 2. Propagation Delay

Quad, High-Speed HDMI/DVI 2:1 Digital Video Switch

Timing Circuits/Timing Diagrams (continued)

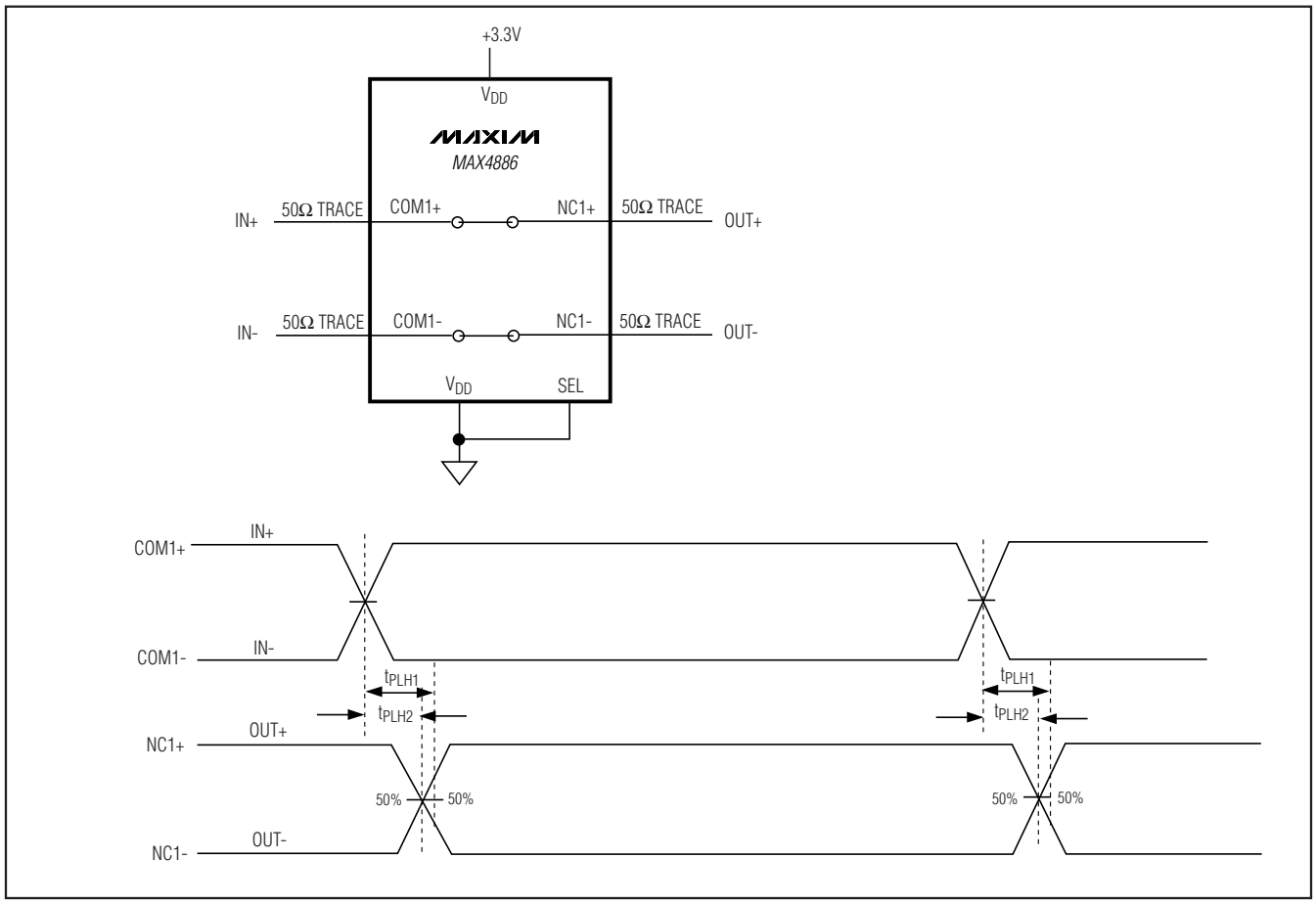


Figure 3. Skew Measurements

Additional Applications Information

In a typical application (see Figure 5), the MAX4886 and MAX4929 are used to route the TMDS signals and low-frequency signals between two HDMI inputs.

In another application (see Figure 6), the MAX4886 is used in a notebook to route high-frequency DVI port on the computer or to the connector on the docking station. The MAX4886 routes four differential signals (RGB and CLK) either to the DVI connector or to the docking station port. The switch is inherently bilateral and may be used as a 2:1 or 1:2 mux without penalties.

Chip Information

PROCESS: BiCMOS

Connect exposed paddle to GND.

Timing Circuits/Timing Diagrams (continued)

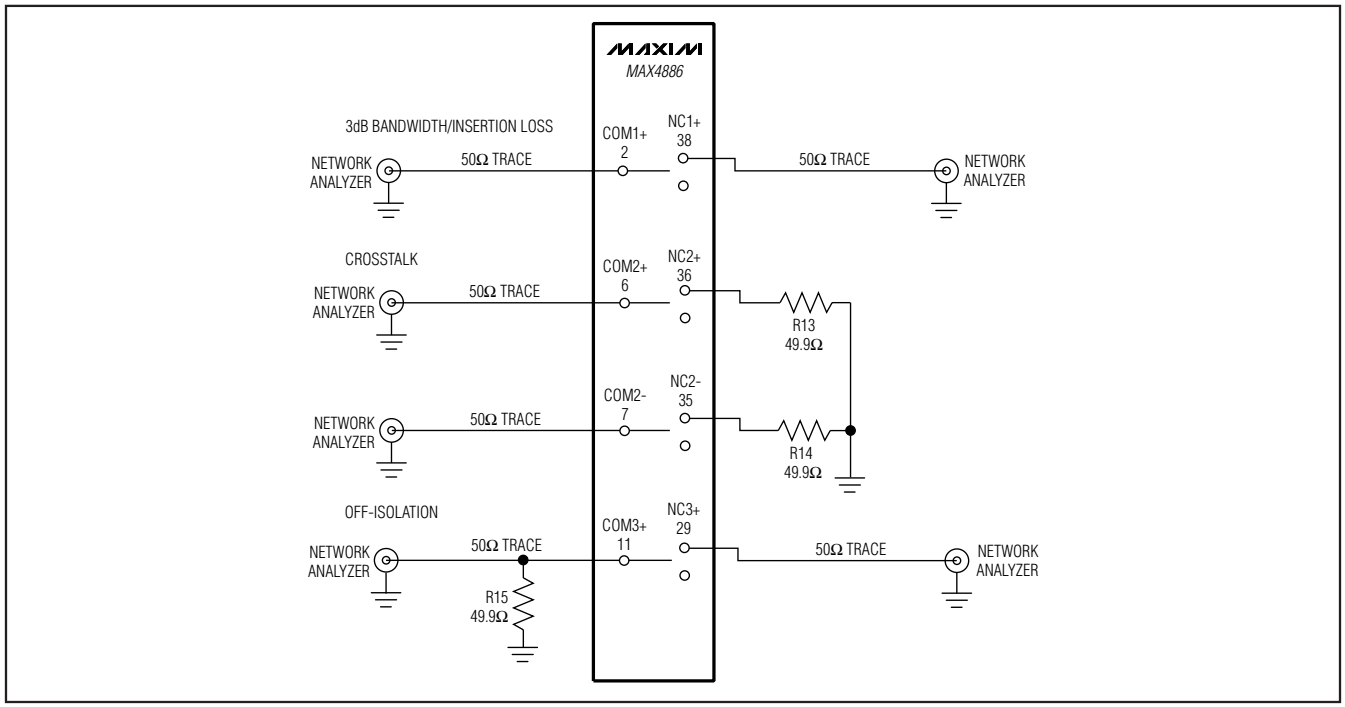


Figure 4. On-Loss, Off-Isolation, and Crosstalk

Typical Application Diagrams

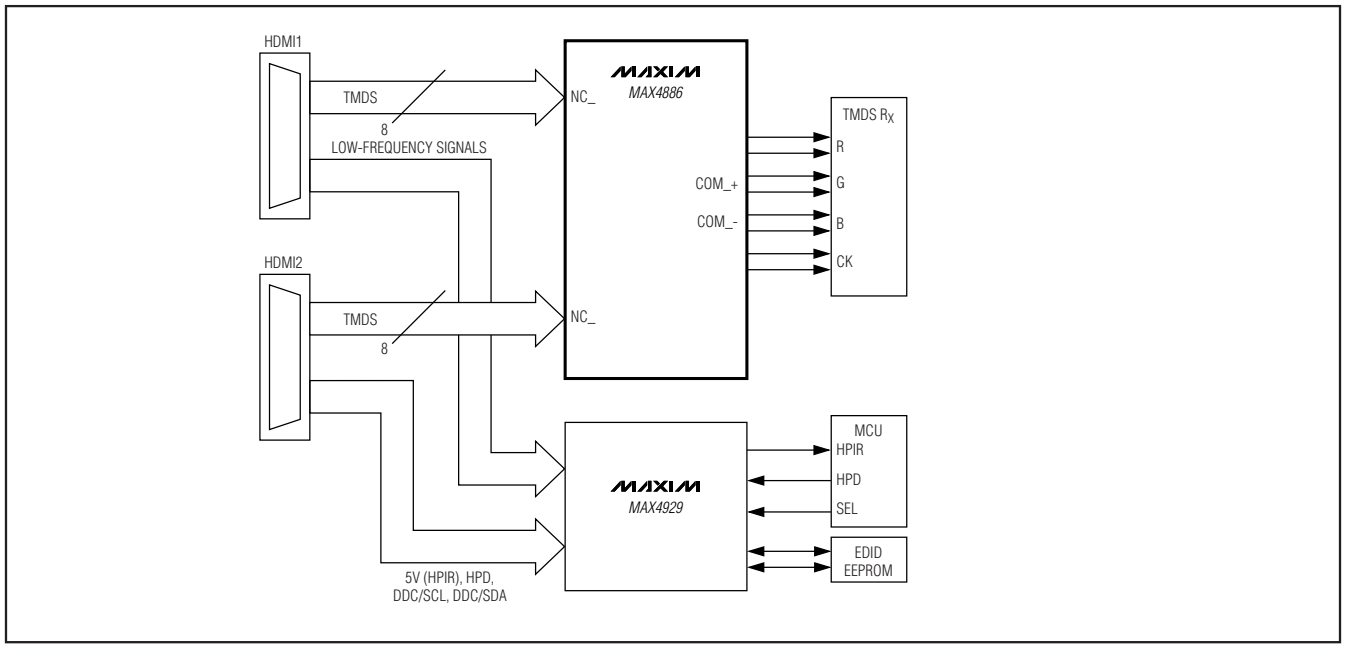


Figure 5. TV/Monitor Application

Quad, High-Speed HDMI/DVI 2:1 Digital Video Switch

Typical Application Diagrams (continued)

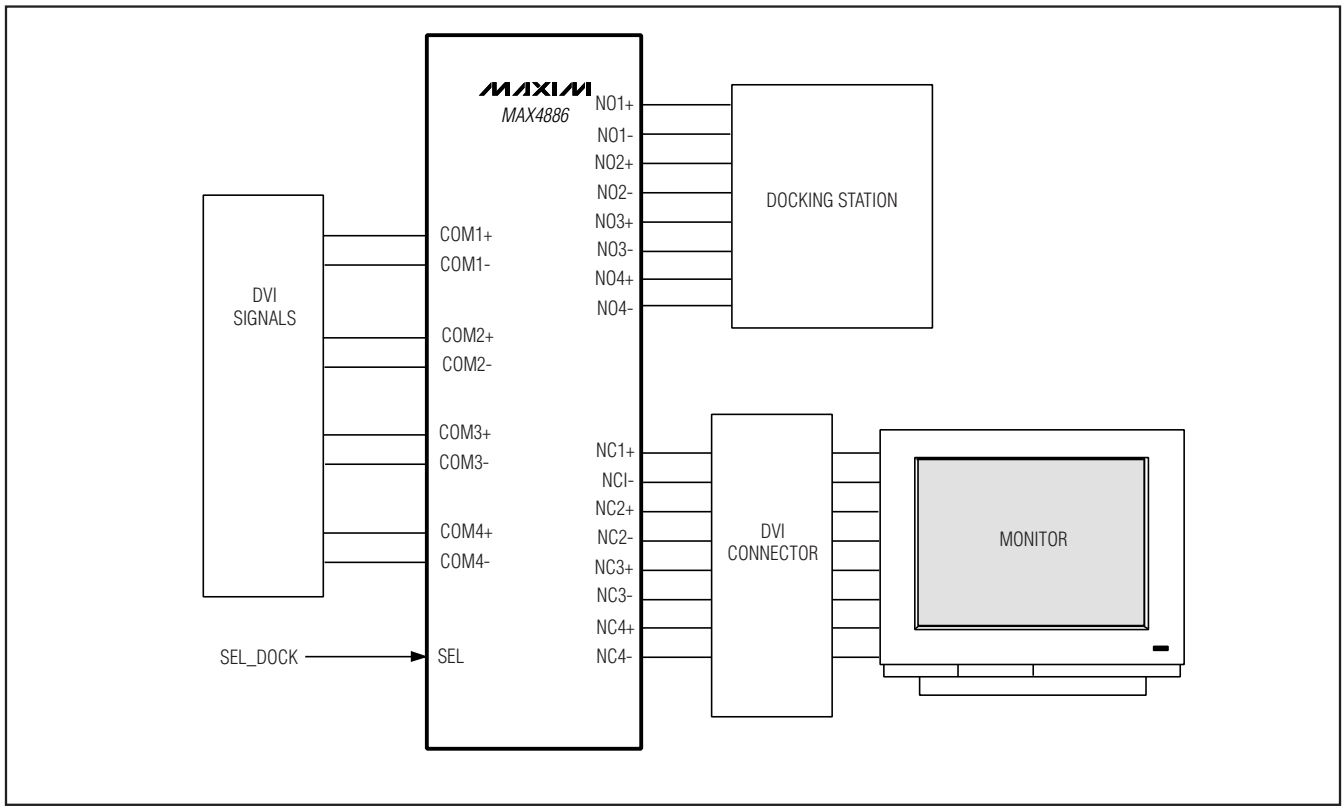
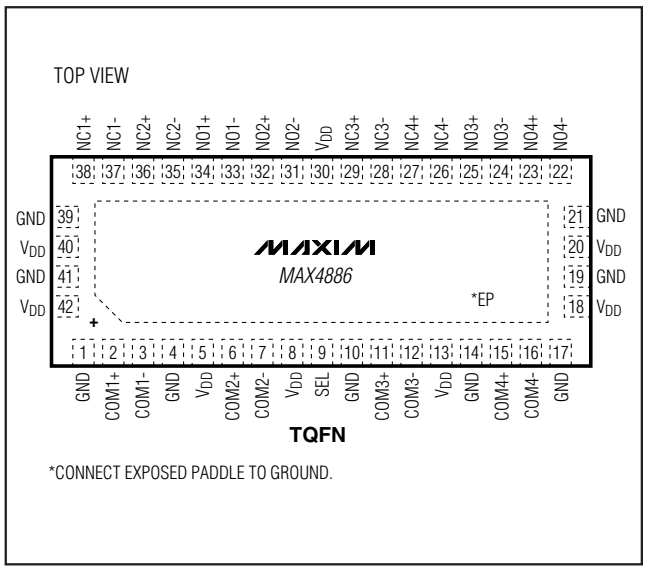


Figure 6. Notebook Application

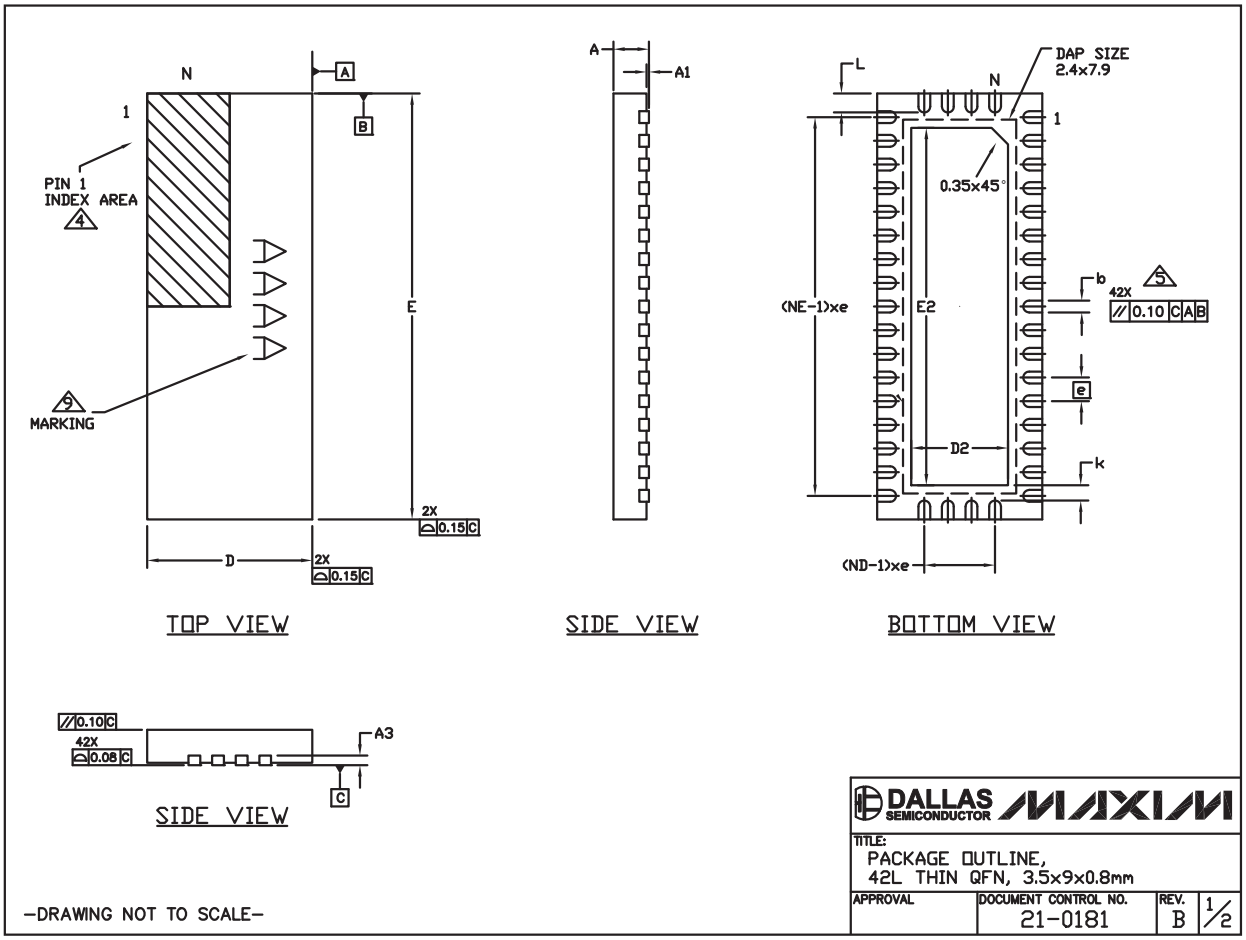
Pin Configuration



Quad, High-Speed HDMI/DVI 2:1 Digital Video Switch

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Quad, High-Speed HDMI/DVI 2:1 Digital Video Switch

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS				
REF.	MIN.	NOM.	MAX.	NOTE
A	0.70	0.75	0.80	
A1	0	-	0.05	
A3	0.20 REF.			
b	0.20	0.25	0.30	
D	3.40	3.50	3.60	
E	8.90	9.00	9.10	
e	0.50 BSC.			
k	0.25	-	-	
L	0.35	0.40	0.45	ALL PINS
N	42			
ND	4			
NE	17			

	EXPOSED PAD VARIATIONS					
	D2			E2		
PKG. CODE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T423590-1	1.95	2.05	2.15	7.45	7.55	7.65
T423590M-1	1.95	2.05	2.15	7.45	7.55	7.65

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
8. WARPAGE SHALL NOT EXCEED 0.10mm.
9. MARKING IS FOR PACKAGE ORIENTATION PURPOSE ONLY.
10. LEAD CENTERLINES TO BE AT DEFINED BY DIMESION e ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 42L THIN QFN, 3.5x9x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0181	B	2/2