

Absolute Maximum Ratings

Supply Voltage (V_{DD} to V_{SS})	6V	8-Pin μMAX® (derate 4.8mW/°C above +70°C)	387.8mW
All Other Pins	($V_{SS} - 0.3V$) to ($V_{DD} + 0.3V$)	10-Pin μMAX (derate 8.8mW/°C above +70°C)	707.3mW
Output Short-Circuit Duration to V_{DD} or V_{SS} (Note 1)	10s	10-Bump UCSP (derate 5.6mW/°C above +70°C)	448.7mW
Continuous Power Dissipation (Multilayer, $T_A = +70^\circ\text{C}$)		14-Pin SO (derate 11.9mW/°C above +70°C)	952.4mW
5-Pin SC70 (derate 3.1mW/°C above +70°C)	247mW	14-Pin TSSOP (derate 10mW/°C above +70°C)	796.8mW
5-Pin SOT23 (derate 3.9mW/°C above +70°C)	313mW	Operating Temperature Range	-40°C to +125°C
6-Pin SC70 (derate 3.1mW/°C above +70°C)	245mW	Junction Temperature	+150°C
6-Pin SOT23 (derate 13.4mW/°C above +70°C)	1072mW	Storage Temperature Range	-65°C to +150°C
6-Pin Thin μDFN (derate 2.1mW/°C above +70°C)	170.2mW	Lead Temperature	
6-Bump UCSP (derate 3.9mW/°C above +70°C)	308.3mW	(excluding 6 and 10 UCSP, soldering, 10s)	+300°C
8-Pin SOT23 (derate 5.1mW/°C above +70°C)	408.2mW	Soldering Temperature (reflow)	+260°C

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Note 1: Package power dissipation should also be observed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

($V_{DD} = 2.7V$, $V_{SS} = 0V$, $V_{CM} = V_{DD}/2$, $V_{OUT} = (V_{DD}/2)$, $R_L = \infty$ connected to ($V_{DD}/2$), $V_{SHDN} = V_{DD}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{DD}	Inferred from PSRR test	2.7		5.5	V
Input Offset Voltage	V_{OS}			0.85	±6	mV
Input Bias Current (Note 4)	I_B	$V_{CM} = V_{SS}$ to V_{DD}			1	pA
Input Offset Current	I_{OS}	$V_{CM} = V_{SS}$ to V_{DD}		1		pA
Input Resistance	R_{IN}			1000		MΩ
Common-Mode Input Voltage Range	V_{CM}	Inferred from CMRR test	V_{SS}		V_{DD}	V
Common-Mode Rejection Ratio	CMRR	$V_{SS} < V_{CM} < V_{DD}$	52	70		dB
Power-Supply Rejection Ratio	PSRR	$V_{DD} = 2.7V$ to $5.5V$	73	85		dB
Shutdown Output Impedance	R_{OUT}	$V_{SHDN} = 0V$ (Note 3)		10		Ω
Output Voltage in Shutdown	$V_{OUT(SHDN)}$	$V_{SHDN} = 0V$, $R_L = 200\Omega$ (Note 3)		68		mV
Large-Signal Voltage Gain	A_{VOL}	$V_{SS} + 0.20V < V_{OUT} < V_{DD} - 0.20V$	$R_L = 100k\Omega$	100		dB
			$R_L = 2k\Omega$	85	98	
			$R_L = 200\Omega$	74	80	
Output Voltage Swing	V_{OUT}	$R_L = 32\Omega$	$V_{DD} - V_{OH}$	400	500	mV
			$V_{OL} - V_{SS}$	360	500	
		$R_L = 200\Omega$	$V_{DD} - V_{OH}$	80	120	
			$V_{OL} - V_{SS}$	70	120	
		$R_L = 2k\Omega$	$V_{DD} - V_{OH}$	8	14	
			$V_{OL} - V_{SS}$	7	14	

DC Electrical Characteristics (continued)

($V_{DD} = 2.7V$, $V_{SS} = 0V$, $V_{CM} = V_{DD}/2$, $V_{OUT} = (V_{DD}/2)$, $R_L = \infty$ connected to $(V_{DD}/2)$, $V_{SHDN} = V_{DD}$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Source/Sink Current	I _{OUT}	V _{DD} = 2.7V, V _{IN} = ±100mV			70		mA	
		V _{DD} = 5V, V _{IN} = ±100mV			200			
Output Voltage		I _L = 10mA	V _{DD} = 2.7V	V _{DD} - V _{OH}	128	200	mV	
				V _{OL} - V _{SS}	112	175		
		I _L = 30mA	V _{DD} = 5V	V _{DD} - V _{OH}	240	320		
				V _{OL} - V _{SS}	224	300		
Quiescent Supply Current (per Amplifier)	I _{DD}	V _{DD} = 5.5V, V _{CM} = V _{DD} /2			1.2	2.3	mA	
		V _{DD} = 2.7V, V _{CM} = V _{DD} /2			1.1	2.0		
Shutdown Supply Current (per Amplifier) (Note 3)	I _{DD} (SHDN)	V _{SHDN} = 0V, R _L = ∞		V _{DD} = 5.5V	0.5	1	μA	
				V _{DD} = 2.7V	0.1	1		
SHDN Logic Threshold (Note 3)	V _{IL}	Shutdown mode				0.8	V	
	V _{IH}	Normal mode				V _{DD} x 0.57		
SHDN Input Bias Current		V _{SS} < V _{SHDN} < V _{DD} (Note 3)			50		pA	

DC Electrical Characteristics

($V_{DD} = 2.7V$, $V_{SS} = 0V$, $V_{CM} = V_{DD}/2$, $V_{OUT} = (V_{DD}/2)$, $R_L = \infty$ connected to $(V_{DD}/2)$, $V_{SHDN} = V_{DD}$, $T_A = -40$ to $+125^\circ C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{DD}	Inferred from PSRR test	2.7		5.5	V
Input Offset Voltage	V_{OS}				±8	mV
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$			±3		μV/°C
Input Bias Current (Note 4)	I_B	$T_A = -40^\circ C$ to $+85^\circ C$			17	pA
		$T_A = -40^\circ C$ to $+125^\circ C$			550	
Common-Mode Input Voltage Range	V_{CM}	Inferred from CMRR test	V_{SS}		V_{DD}	V
Common-Mode Rejection Ratio	CMRR	$V_{SS} < V_{CM} < V_{DD}$	46			dB
Power-Supply Rejection Ratio	PSRR	$V_{DD} = 2.7V$ to $5.5V$	70			dB
Output Voltage in Shutdown	$V_{OUT(SHDN)}$	$V_{SHDN} = 0V$, $R_L = 200\Omega$ (Note 3)			150	mV
Large-Signal Voltage Gain	A_{VOL}	$V_{SS} + 0.20V$ $< V_{DD} - 0.20V$	$R_L = 2k\Omega$	76		dB
			$R_L = 200\Omega$	67		
Output Voltage Swing	V_{OUT}	$R_L = 32\Omega$ $T_A = +85^\circ C$	$V_{DD} - V_{OH}$		650	mV
			$V_{OL} - V_{SS}$		650	
		$R_L = 200\Omega$	$V_{DD} - V_{OH}$		150	
			$V_{OL} - V_{SS}$		150	
		$R_L = 2k\Omega$	$V_{DD} - V_{OH}$		20	
			$V_{OL} - V_{SS}$		20	

DC Electrical Characteristics

($V_{DD} = 2.7V$, $V_{SS} = 0V$, $V_{CM} = V_{DD}/2$, $V_{OUT} = (V_{DD}/2)$, $R_L = \infty$ connected to $(V_{DD}/2)$, $V_{SHDN} = V_{DD}$, $T_A = -40$ to $+125^\circ C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Voltage		$I_L = 10\text{mA}$	$V_{DD} = 2.7\text{V}$	$V_{DD} - V_{OH}$			250	mV
				$V_{OL} - V_{SS}$			230	
		$I_L = 30\text{mA}$ $T_A = -40^\circ\text{C}$ to $+85^\circ$	$V_{DD} = 5\text{V}$	$V_{DD} - V_{OH}$			400	
				$V_{OL} - V_{SS}$			370	
Quiescent Supply Current (per Amplifier)	I_{DD}	$V_{DD} = 5.5\text{V}, V_{CM} = V_{DD}/2$					2.8	mA
		$V_{DD} = 2.7\text{V}, V_{CM} = V_{DD}/2$					2.5	
Shutdown Supply Current (per Amplifier) (Note 3)	$I_{DD}(\text{SHDN})$	$V_{\text{SHDN}} < 0\text{V}, R_L = \infty$		$V_{DD} = 5.5\text{V}$			2.0	μA
				$V_{DD} = 2.7\text{V}$			2.0	
SHDN Logic Threshold (Note 3)	V_{IL}	Shutdown mode					0.8	V
	V_{IH}	Normal mode			$V_{DD} \times 0.61$			

AC Electrical Characteristics

($V_{DD} = 2.7V$, $V_{SS} = 0V$, $V_{CM} = V_{DD}/2$, $V_{OUT} = (V_{DD}/2)$, $R_L = \infty$ connected to $(V_{DD}/2)$, $V_{SHDN} = V_{DD}$, $T_A = +125^\circ C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	GBWP	$V_{CM} = V_{DD}/2$		10		MHz
Full-Power Bandwidth	FPBW	$V_{OUT} = 2V_{P-P}$, $V_{DD} = 5V$		0.8		MHz
Slew Rate	SR			10		V/μs
Phase Margin	PM			70		Degrees
Gain Margin	GM			15		dB
Total Harmonic Distortion Plus Noise	THD+N	$f = 10kHz$, $V_{OUT} = 2V_{P-P}$, $A_{VCL} = 1V/V$		0.0005		%
Input Capacitance	C_{IN}			8		pF
Voltage-Noise Density	e_n	$f = 1kHz$		15		$nV/\sqrt{Hz}$
		$f = 10kHz$		12		
Channel-to-Channel Isolation		$f = 1kHz$, $R_L = 100k\Omega$		125		dB
Capacitive-Load Stability		$A_{VCL} = 1V/V$, no sustained oscillations		780		pF
Shutdown Time	t_{SHDN}	(Note 3)		1		μs
Enable Time from Shutdown	t_{ENABLE}	(Note 3)		6		μs
Power-Up Time	t_{ON}			5		μs

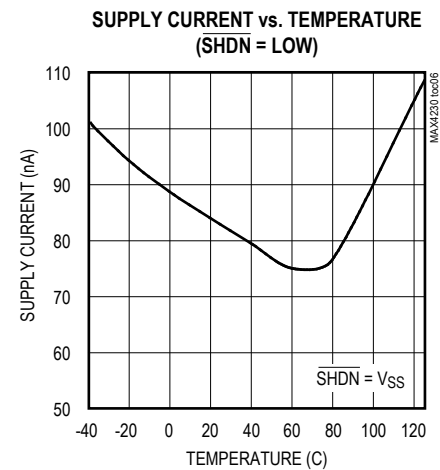
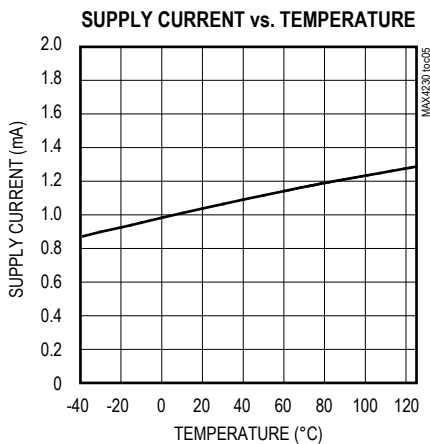
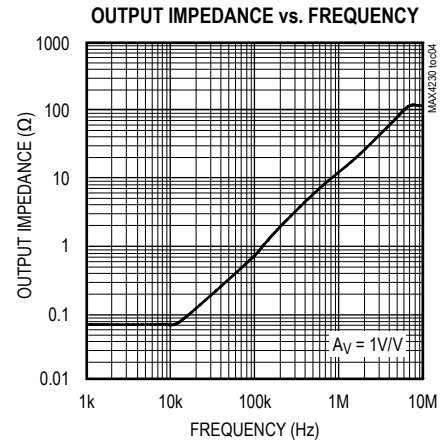
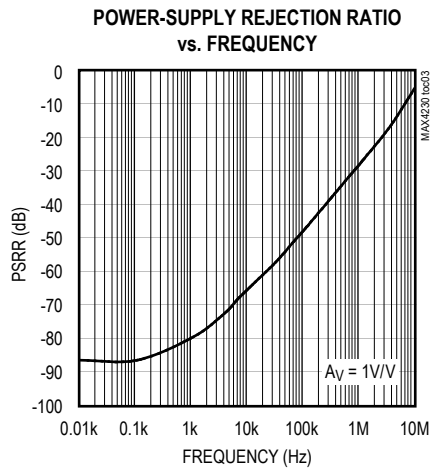
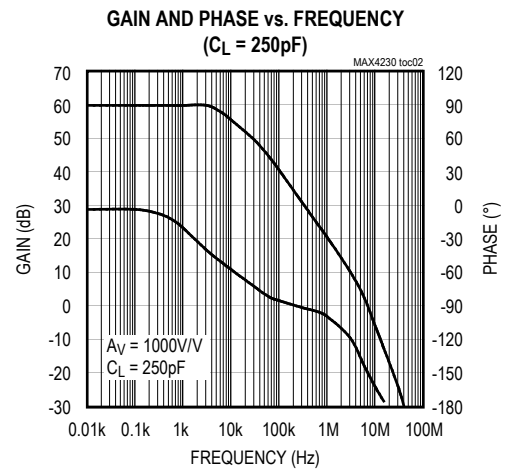
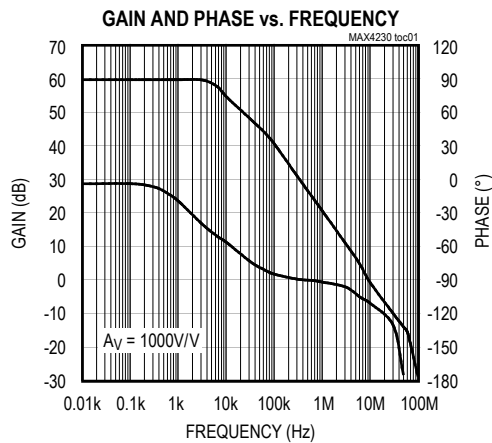
Note 2: All units 100% tested at $+25^\circ C$. All temperature limits are guaranteed by design.

Note 3: SHDN logic parameters are for the MAX4231/MAX4233 only.

Note 4: Guaranteed by design.

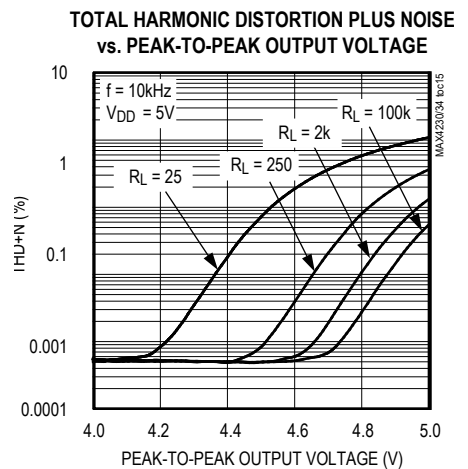
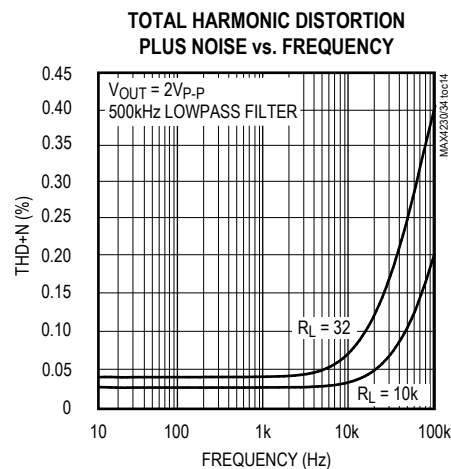
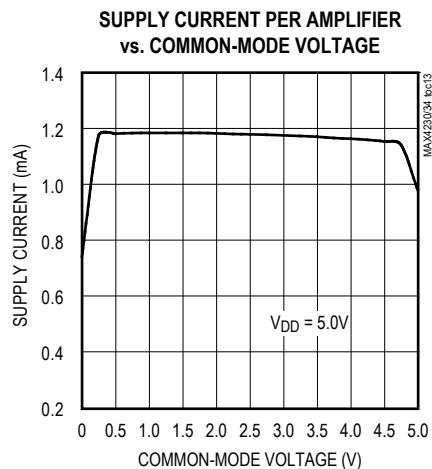
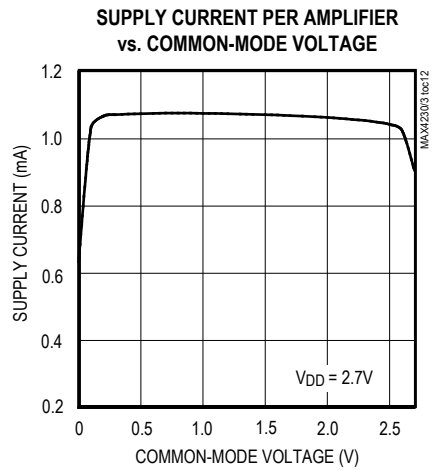
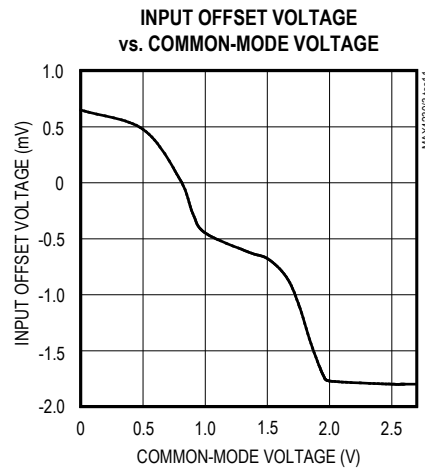
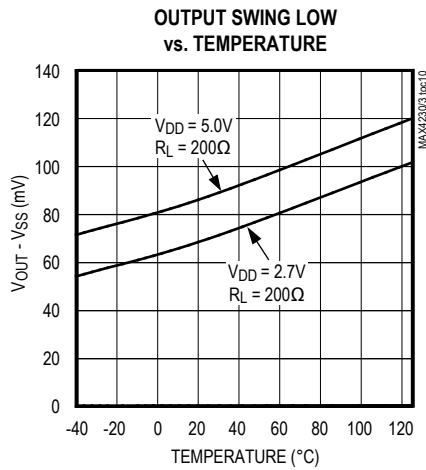
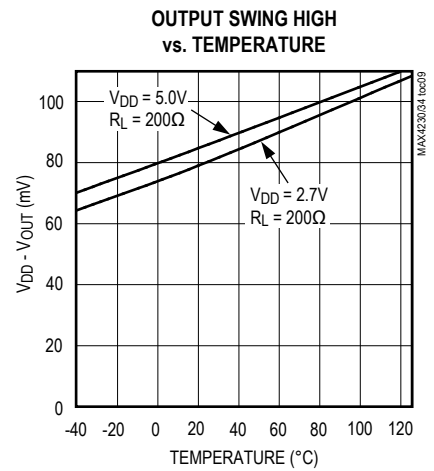
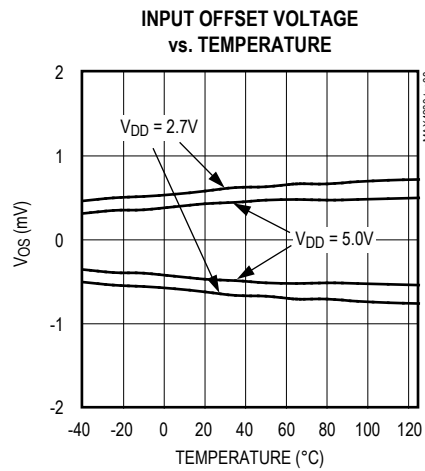
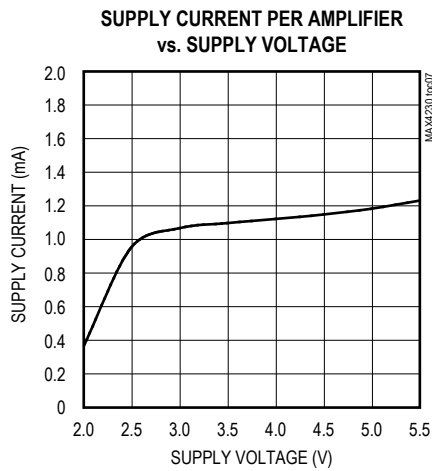
Typical Operating Characteristics

($V_{DD} = 2.7V$, $V_{SS} = 0V$, $V_{CM} = V_{DD}/2$, $V_{OUT} = V_{DD}/2$, $R_L = \infty$, connected to $V_{DD}/2$, $\overline{V_{SHDN}} = V_{DD}$, $T_A = +25^\circ C$, unless otherwise noted.)



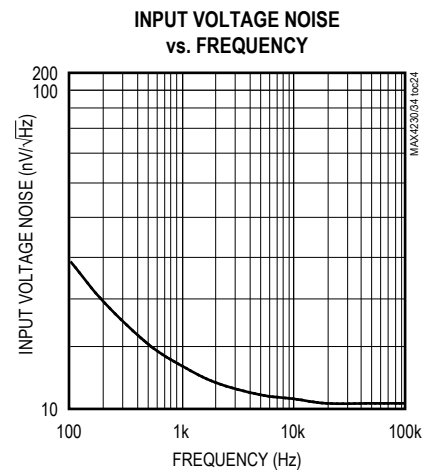
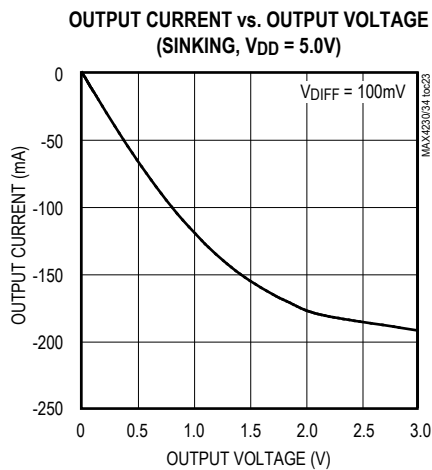
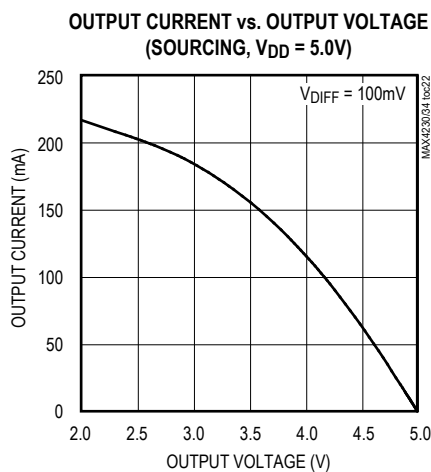
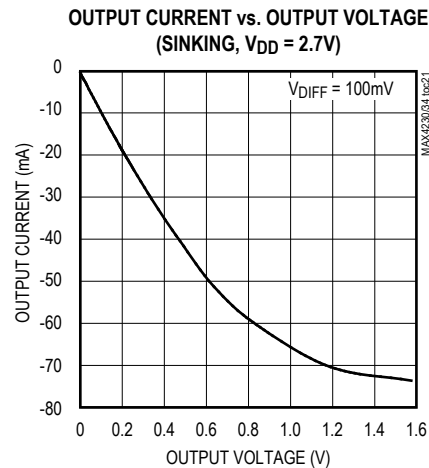
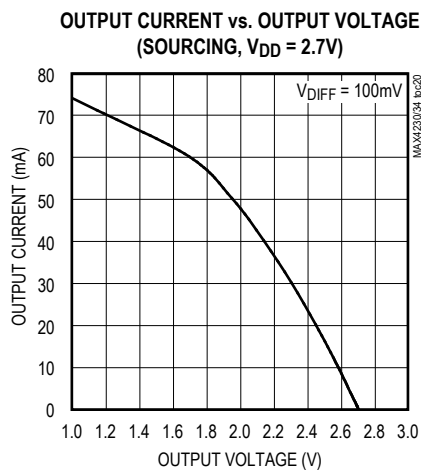
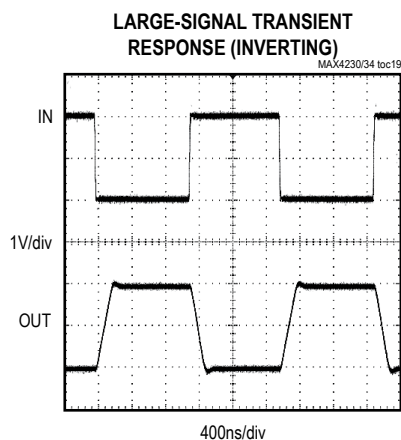
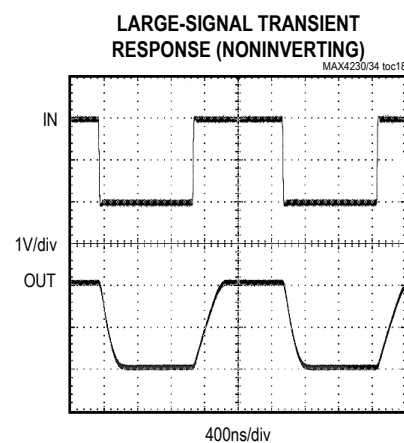
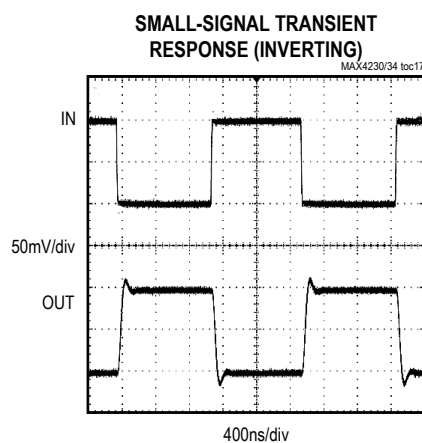
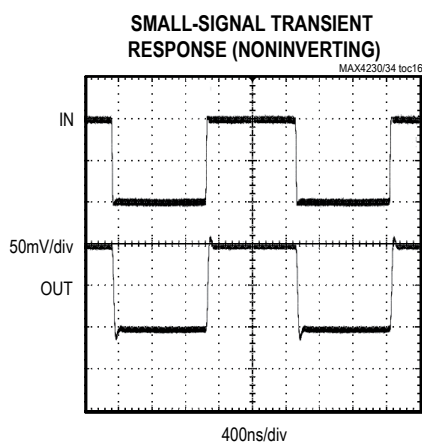
Typical Operating Characteristics (continued)

($V_{DD} = 2.7V$, $V_{SS} = 0V$, $V_{CM} = V_{DD}/2$, $V_{OUT} = V_{DD}/2$, $R_L = \infty$, connected to $V_{DD}/2$, $V_{SHDN} = V_{DD}$, $T_A = +25^\circ C$, unless otherwise noted.)



Typical Operating Characteristics (continued)

($V_{DD} = 2.7V$, $V_{SS} = 0V$, $V_{CM} = V_{DD}/2$, $V_{OUT} = V_{DD}/2$, $R_L = \infty$, connected to $V_{DD}/2$, $V_{SHDN} = V_{DD}$, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

PIN					BUMP		NAME	FUNCTION
MAX4230 SOT23/ SC70	MAX4231 SOT23/ SC70/Thin μDFN	MAX4232 SOT23/ μMAX	MAX4233 μMAX	MAX4234 TSSOP/SO	MAX4231 UCSP	MAX4233 UCSP		
1	1	—	—	—	B1	—	IN+	Noninverting Input
2	2	4	4	11	A1	B4	VSS	Negative Supply Input. Connect to ground for single- supply operation.
3	3	—	—	—	B2	—	IN-	Inverting Input
4	4	—	—	—	A2	—	OUT	Amplifier Output
5	6	8	10	4	A3	B1	VDD	Positive Supply Input
—	5	—	5, 6	—	B3	C4, A4	$\overline{\text{SHDN}}$, SHDN1, SHDN2	Shutdown Control. Tie to high for normal operation.
—	—	3	3	3	—	C3	IN1+	Noninverting Input to Amplifier 1
—	—	2	2	2	—	C2	IN1-	Inverting Input to Amplifier 1
—	—	1	1	1	—	C1	OUT1	Amplifier 1 Output
—	—	5	7	5	—	A3	IN2+	Noninverting Input to Amplifier 2
—	—	6	8	6	—	A2	IN2-	Inverting Input to Amplifier 2
—	—	7	9	7	—	A1	OUT2	Amplifier 2 Output
—	—	—	—	10, 12	—	—	IN3+, N4+	Noninverting Input to Amplifiers 3
—	—	—	—	9, 13	—	—	IN3-, IN4-	Inverting Input to Amplifiers 3 and
—	—	—	—	8, 14	—	—	OUT3, OUT4	Amplifiers 3 and 4 Outputs

Detailed Description

Rail-to-Rail Input Stage

The MAX4230–MAX4234 CMOS operational amplifiers have parallel-connected n- and p-channel differential input stages that combine to accept a common-mode range extending to both supply rails. The n-channel stage is active for common-mode input voltages typically greater than ($V_{SS} + 1.2V$), and the p-channel stage is active for common-mode input voltages typically less than ($V_{DD} - 1.2V$).

Applications Information

Package Power Dissipation

Warning: Due to the high output current drive, this op amp can exceed the absolute maximum power-dissipation rating. As a general rule, as long as the peak current is less than or equal to 40mA, the maximum

package power dissipation is not exceeded for any of the package types offered. There are some exceptions to this rule, however. The absolute maximum power-dissipation rating of each package should always be verified using the following equations. The equation below gives an approximation of the package power dissipation:

$$P_{IC(DISS)} \cong V_{RMS} I_{RMS} \cos\theta$$

where:

V_{RMS} = RMS voltage from V_{DD} to V_{OUT} when sourcing current and RMS voltage from V_{OUT} to V_{SS} when sinking current.

I_{RMS} = RMS current flowing out of or into the op amp and the load.

θ = phase difference between the voltage and the current. For resistive loads, $\cos\theta = 1$.

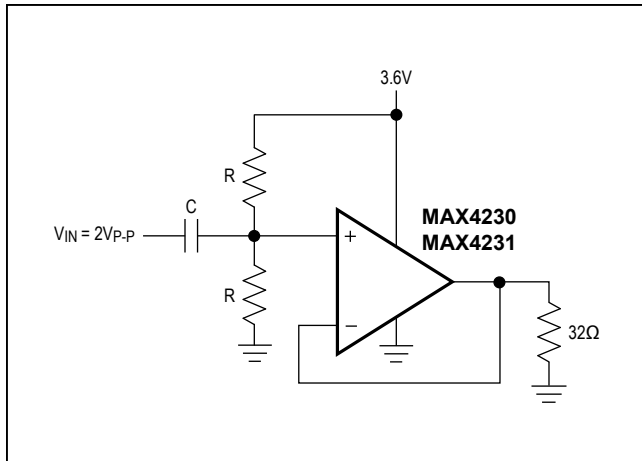


Figure 1. MAX4230/MAX4231 Used in Single-Supply Operation Circuit Example

For example, the circuit in [Figure 1](#) has a package power dissipation of 196mW:

$$\begin{aligned} V_{RMS} &\cong (V_{DD} - V_{DC}) + \frac{V_{PEAK}}{\sqrt{2}} \\ &= 3.6V - 1.8V + \frac{1.0V}{\sqrt{2}} = 2.507V_{RMS} \\ I_{RMS} &\cong I_{DC} + \frac{I_{PEAK}}{\sqrt{2}} = \frac{1.8V}{32\Omega} + \frac{1.0V / 32\Omega}{\sqrt{2}} \\ &= 78.4mA_{RMS} \end{aligned}$$

where:

V_{DC} = the DC component of the output voltage.

I_{DC} = the DC component of the output current.

V_{PEAK} = the highest positive excursion of the AC component of the output voltage.

I_{PEAK} = the highest positive excursion of the AC component of the output current.

Therefore:

$$\begin{aligned} P_{IC(DISS)} &= V_{RMS} I_{RMS} \cos \theta \\ &= 196mW \end{aligned}$$

Adding a coupling capacitor improves the package power dissipation because there is no DC current to the load, as shown in [Figure 2](#):

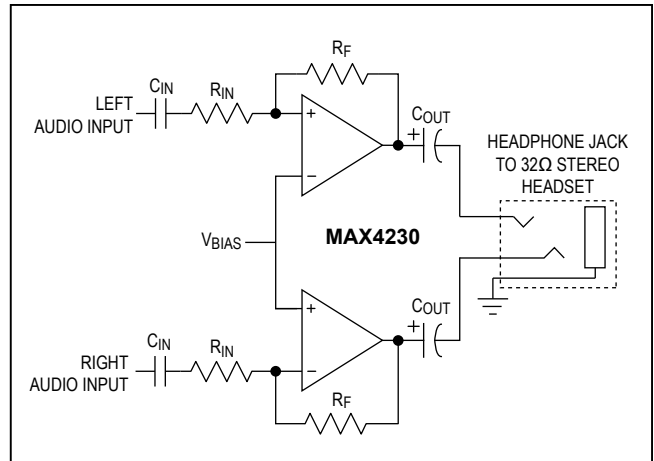


Figure 2. Circuit Example: Adding a Coupling Capacitor Greatly Reduces Power Dissipation of its Package

$$\begin{aligned} V_{RMS} &\cong \frac{V_{PEAK}}{\sqrt{2}} \\ &= \frac{1.0V}{\sqrt{2}} = 0.707V_{RMS} \\ I_{RMS} &\cong I_{DC} + \frac{I_{PEAK}}{\sqrt{2}} = 0A + \frac{1.0V / 32\Omega}{\sqrt{2}} \\ &= 22.1mA_{RMS} \end{aligned}$$

Therefore:

$$\begin{aligned} P_{IC(DISS)} &= V_{RMS} I_{RMS} \cos \theta \\ &= 15.6mW \end{aligned}$$

If the configuration in [Figure 1](#) were used with all four of the MAX4234 amplifiers, the absolute maximum power dissipation rating of this package would be exceeded (see the [Absolute Maximum Ratings](#) section).

60mW Single-Supply Stereo Headphone Driver

Two MAX4230/MAX4231s can be used as a single-supply, stereo headphone driver. The circuit shown in [Figure 2](#) can deliver 60mW per channel with 1% distortion from a single 5V supply.

The input capacitor (C_{IN}), in conjunction with R_{IN} , forms a highpass filter that removes the DC bias from the incoming signal. The -3dB point of the highpass filter is given by

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

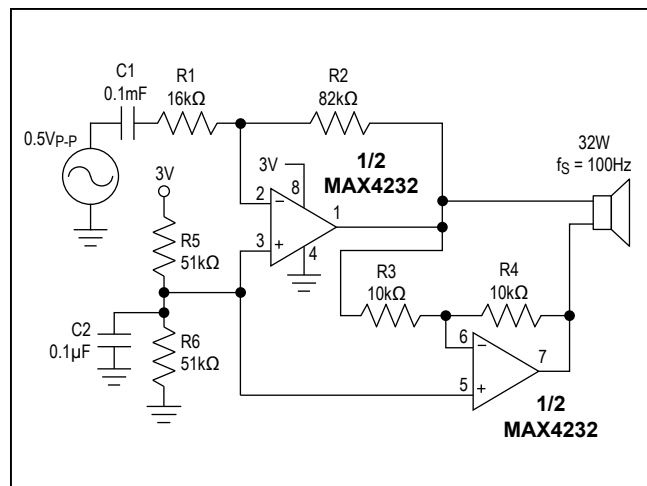


Figure 3. Dual MAX4230/MAX4231 Bridge Amplifier for 200mW at 3V

Choose gain-setting resistors R_{IN} and R_F according to the amount of desired gain, keeping in mind the maximum output amplitude. The output coupling capacitor, C_{OUT} , blocks the DC component of the amplifier output, preventing DC current flowing to the load. The output capacitor and the load impedance form a highpass filter with the -3dB point determined by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{OUT}}$$

For a 32Ω load, a 100μF aluminum electrolytic capacitor gives a low-frequency pole at 50Hz.

Bridge Amplifier

The circuit shown in Figure 3 uses a dual MAX4230 to implement a 3V, 200mW amplifier suitable for use in size-constrained applications. This configuration eliminates the need for the large coupling capacitor required by the single op-amp speaker driver when single-supply operation is necessary. Voltage gain is set to 10V/V; however, it can be changed by adjusting the 82kΩ resistor value.

Rail-to-Rail Input Stage

The MAX4230–MAX4234 CMOS op amps have parallel connected n- and p-channel differential input stages that combine to accept a common-mode range extending to both supply rails. The n-channel stage is active for common-mode input voltages typically greater than ($V_{SS} + 1.2V$), and the p-channel stage is active for common-mode input voltages typically less than ($V_{DD} - 1.2V$).

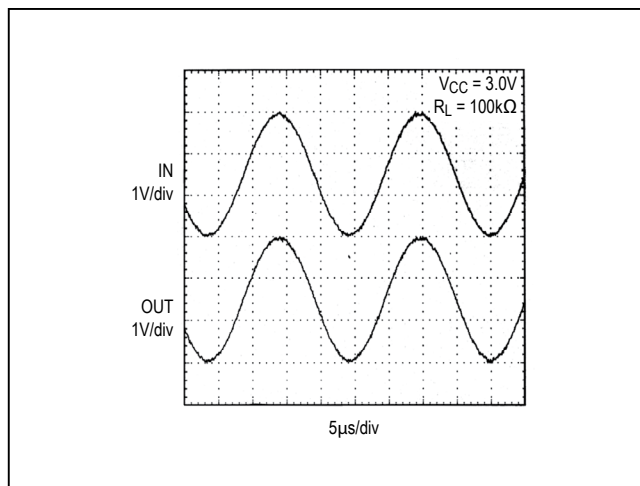


Figure 4. Rail-to-Rail Input/Output Range

Rail-to-Rail Output Stage

The minimum output is within millivolts of ground for single-supply operation, where the load is referenced to ground (V_{SS}). Figure 4 shows the input voltage range and the output voltage swing of a MAX4230 connected as a voltage follower. The maximum output voltage swing is load dependent; however, it is guaranteed to be within 500mV of the positive rail ($V_{DD} = 2.7V$) even with maximum load (32Ω to ground).

Observe the [Absolute Maximum Ratings](#) for power dissipation and output short-circuit duration (10s, max) because the output current can exceed 200mA (see the [Typical Operating Characteristics](#).)

Input Capacitance

One consequence of the parallel-connected differential input stages for rail-to-rail operation is a relatively large input capacitance C_{IN} (5pF typ). This introduces a pole at frequency $(2\pi R' C_{IN})^{-1}$, where R' is the parallel combination of the gain-setting resistors for the inverting or noninverting amplifier configuration (Figure 5). If the pole frequency is less than or comparable to the unity-gain bandwidth (10MHz), the phase margin is reduced, and the amplifier exhibits degraded AC performance through either ringing in the step response or sustained oscillations. The pole frequency is 10MHz when $R' = 2k\Omega$. To maximize stability, $R' \ll 2k\Omega$ is recommended.

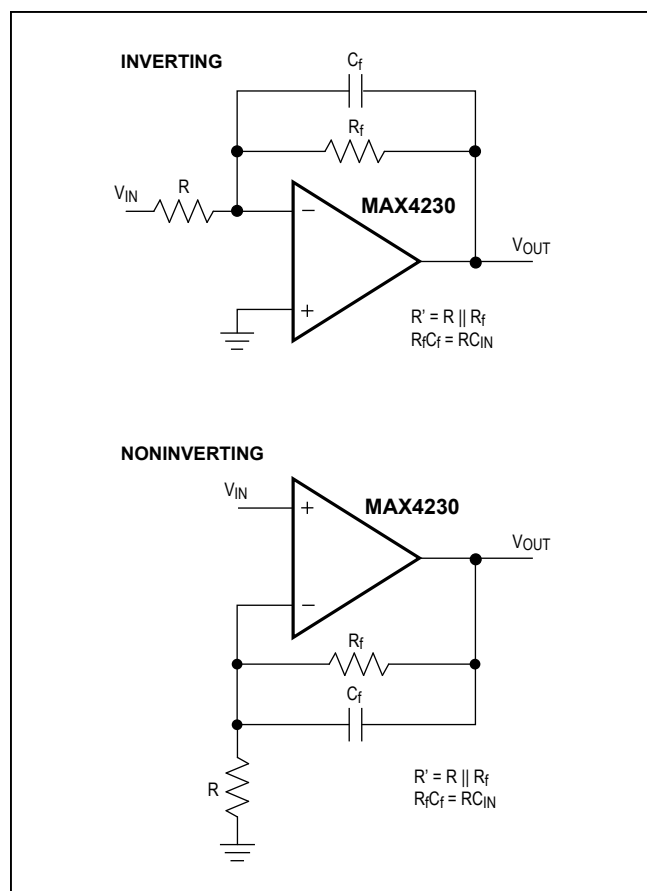


Figure 5. Inverting and Noninverting Amplifiers with Feedback Compensation

To improve step response when $R' > 2k\Omega$, connect small capacitor C_f between the inverting input and output. Choose C_f as follows:

$$C_f = 8(R/R_f) \text{ [pF]}$$

where R_f is the feedback resistor and R is the gain-setting resistor (Figure 5).

Driving Capacitive Loads

The MAX4230–MAX4234 have a high tolerance for capacitive loads. They are stable with capacitive loads up to 780pF. Figure 6 is a graph of the stable operating region for various capacitive loads vs. resistive loads. Figures 7 and 8 show the transient response with excessive capacitive loads (1500pF), with and without the addition of an isolation resistor in series with the output. Figure 9 shows a typical noninverting capacitive-load-driving circuit in the unity-gain configuration.

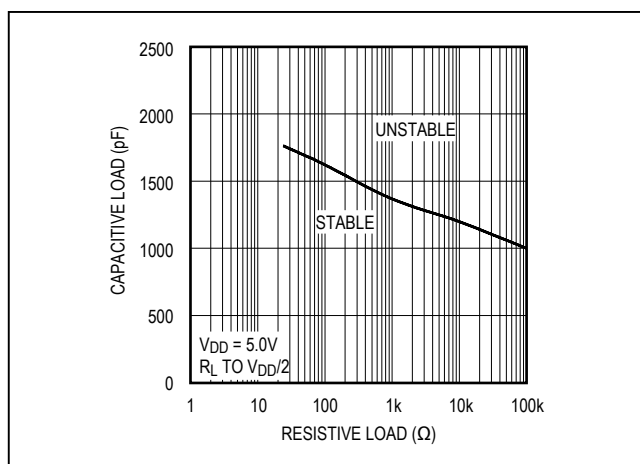


Figure 6. Capacitive-Load Stability

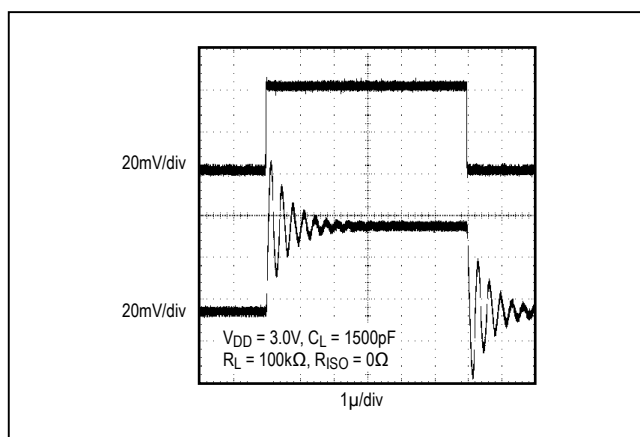


Figure 7. Small-Signal Transient Response with Excessive Capacitive Load

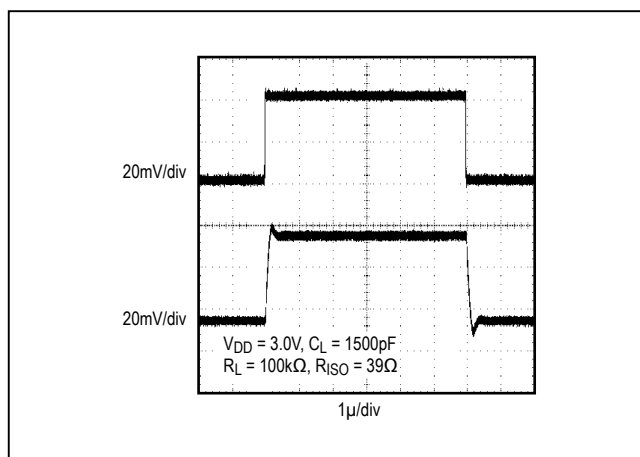


Figure 8. Small-Signal Transient Response with Excessive Capacitive Load with Isolation Resistor

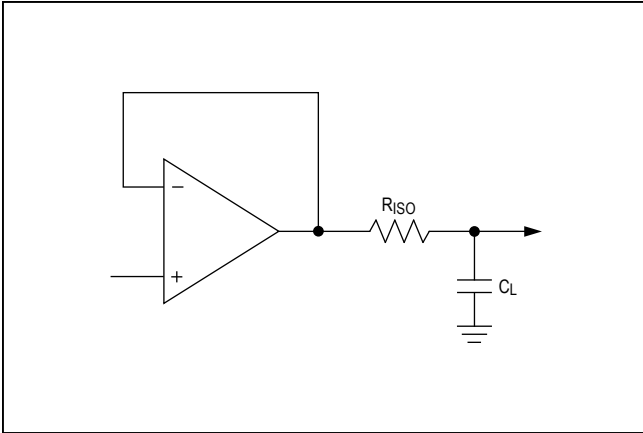


Figure 9. Capacitive-Load-Driving Circuit

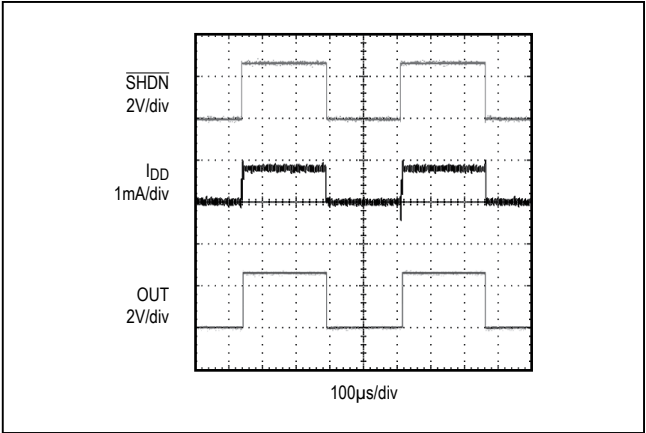


Figure 11. Shutdown Enable/Disable Supply Current

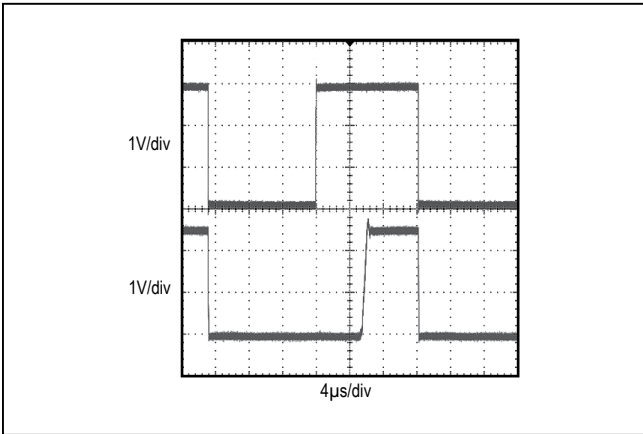


Figure 10. Shutdown Output Voltage Enable/Disable

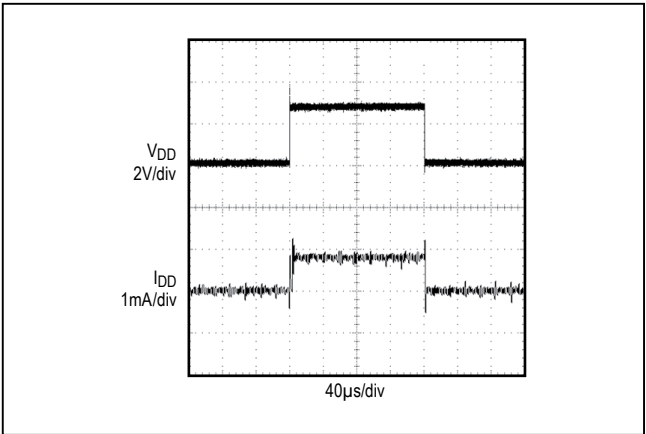


Figure 12. Power-Up/Down Supply Current

The resistor improves the circuit's phase margin by isolating the load capacitor from the op amp's output.

Power-Up and Shutdown Modes

The MAX4231/MAX4233 have a shutdown option. When the shutdown pin (SHDN) is pulled low, supply current drops to 0.5 μ A per amplifier ($V_{DD} = 2.7V$), the amplifiers are disabled, and their outputs are driven to V_{SS} . Since the outputs are actively driven to V_{SS} in shutdown, any pullup resistor on the output causes a current drain from the supply. Pulling SHDN high enables the amplifier. In the dual MAX4233, the two amplifiers shut down independently. [Figure 10](#) shows the MAX4231's output voltage to a shutdown pulse. The MAX4231–MAX4234 typically settle within 5 μ s after power-up. Figures 11 and 12 show I_{DD} to a shutdown plus and voltage power-up cycle.

Selector Guide

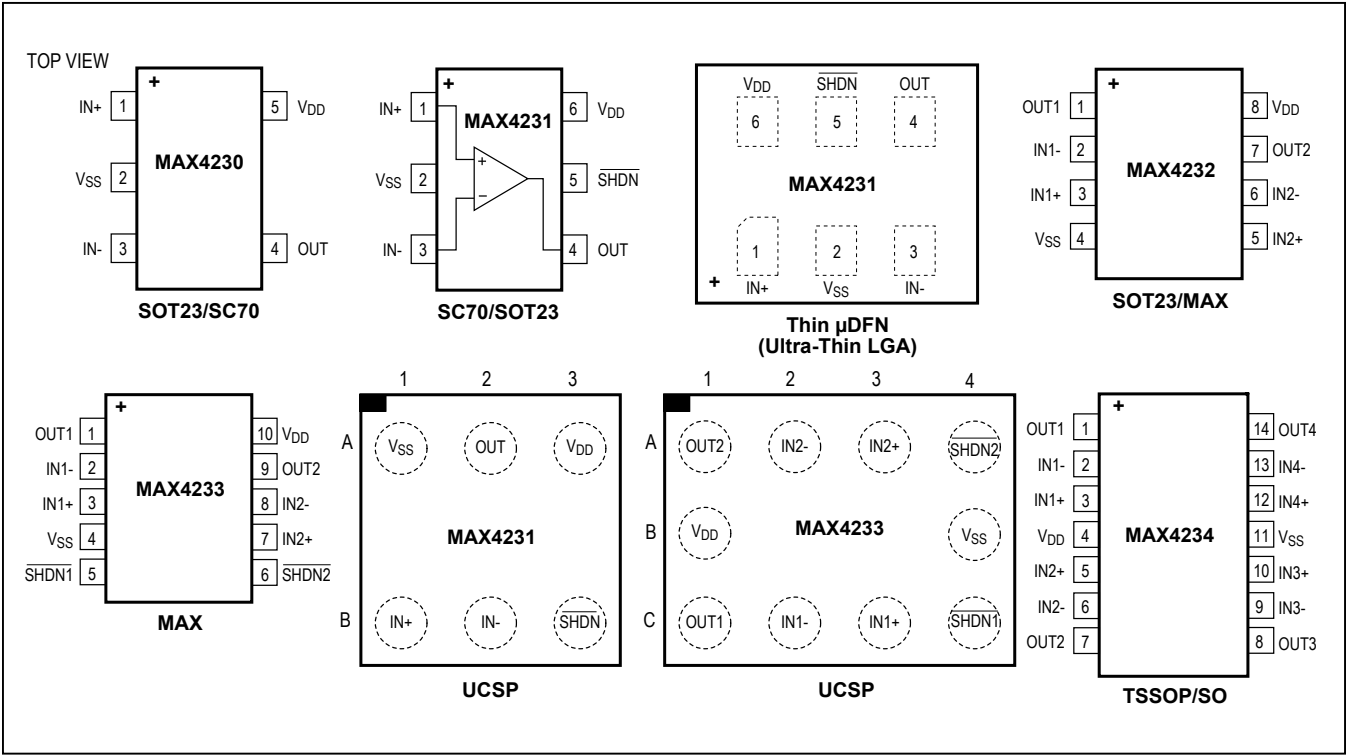
PART	AMPS PER PACKAGE	SHUTDOWN MODE
MAX4230	Single	—
MAX4231	Single	Yes
MAX4232	Dual	—
MAX4233	Dual	Yes
MAX4234	Quad	—

When exiting shutdown, there is a 6 μ s delay before the amplifier's output becomes active ([Figure 10](#)).

MAX4230–MAX4234

High-Output-Drive, 10MHz, 10V/μs,
Rail-to-Rail I/O Op Amps with Shutdown in SC70

Pin/Bump Configurations



Power Supplies and Layout

The MAX4230–MAX4234 can operate from a single 2.7V to 5.5V supply, or from dual ±1.35V to ±2.5V supplies. or single-supply operation, bypass the power supply with a 0.1μF ceramic capacitor. For dual-supply operation, bypass each supply to ground. Good layout improves performance by decreasing the amount of stray capacitance at the op amps' inputs and outputs. Decrease stray capacitance by placing external components close to the op amps' pins, minimizing trace and lead lengths.

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4232AKA+T	-40°C to +125°C	8 SOT23	AAKW
MAX4232AKA/V+T	-40°C to +125°C	8 SOT23	AEQW
MAX4232AUA+T	-40°C to +125°C	8 μMAX	—
MAX4233AUB+T	-40°C to +125°C	10 μMAX	—
MAX4233ABC+T	-40°C to +125°C	10 UCSP	ABF
MAX4234AUD	-40°C to +125°C	14 TSSOP	—
MAX4234AUD/V+T	-40°C to +125°C	14 TSSOP	+YWD
MAX4234ASD	-40°C to +125°C	14 SO	—

+Denotes a lead-free(Pb)/RoHS-compliant package.
T = Tape and reel.
/V denotes an automotive-qualified part.
*EP = Exposed pad.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN NO.
5 SC70	X5+1	21-0076	90-0188
6 SC70	X6SN+1	21-0077	90-0189
5 SOT23	U5+1	21-0057	90-0174
6 SOT23	U6SN+1	21-0058	90-0175
8 μMAX	U8+1	21-0036	90-0092
8 SOT23	K8+5	21-0078	90-0176
10 μMAX	U10+2	21-0061	90-0330
10 UCSP	B12+4	21-0104	—
6 UCSP	R61A1+1	21-0228	—
6 Thin μDFN (Ultra-Thin LGA)	Y61A1+1	21-0190	90-0233
14 TSSOP	U14+1	21-0066	90-0113
14 SO	S14+1	21-0041	90-0112

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
7	7/08	Added 6-pin μDFN package for the MAX4231	1, 2, 8, 13
8	10/08	Corrected top mark for MAX4321, 6 SOT23 package; changed MAX4320 and 4321 to lead-free packages	1
9	10/08	Added shutdown pin limits	3, 4
10	12/08	Added automotive part number	13
11	9/09	Corrected top mark designation and pin configuration, and added UCSP package	1, 2, 8, 13
12	1/10	Updated <i>Absolute Maximum Ratings</i> section	2
13	1/11	Added 10 μMAX to <i>Package Information</i> section	14
14	10/11	Updated <i>Electrical Characteristics</i> table with specs for bias current at various temperatures	1–4
15	3/12	Updated thermal data in the <i>Absolute Maximum Ratings</i>	2
16	6/12	Added automotive part number for MAX4230	1
17	12/13	Updated t _{ENABLE} specification in the <i>AC Electrical Characteristics</i>	6
18	10/14	Corrected μDFN references and added ultra-thin LGA reference to <i>Ordering Information</i> , <i>Pin Configurations</i> , and <i>Package Information</i>	1, 13, 14
19	1/15	Updated <i>General Description</i> , <i>Applications</i> , and <i>Benefits and Features</i> sections	1
20	11/16	Updated TOC22 in <i>Typical Operating Characteristics</i> section	7
21	2/18	Updated <i>Benefits and Features</i> section and <i>Ordering Information</i> table	1, 13
22	7/20	Updated <i>DC Electrical Characteristics</i> table	2
23	5/21	Updated <i>Ordering Information</i> table	13

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