## **ABSOLUTE MAXIMUM RATINGS**

DCIN, CSSP, CSSN, HSD to GND	0.3V to +30V	CS to BATT Current	
CSSP to CSSN	0.6V to +0.6V	PGND to GND	0.3V to +0.3V
BST to GND	0.3V to +36V	VL Source Current	50mA
BST to LX	0.3V to +6V	Continuous Power Dissipation ( $T_A = +70^{\circ}C$ )	
LX to PGND0.0	6V to (V <sub>HSD</sub> + 0.3V)	28-Pin SSOP (derate 9.5mW/°C above +70°	
VL, SHDN, ISETIN, ISETOUT, REF, VADJ, CI	ELL, TIMER1,	Operating Temperature Range	40°C to +85°C
TIMER2, CCI, CCS, CCV, THM to GND	0.3V to +6V	Junction Temperature	+150°C
FASTCHG, FULLCHG, FAULT to GND	0.3V to +30V	Storage Temperature	65°C to +150°C
BATT, CS to GND	0.3V to +20V	Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## **ELECTRICAL CHARACTERISTICS**

(Circuit of Figure 1,  $V_{DCIN} = V_{HSD} = V_{CSSP} = V_{CSSN} = 18V$ ,  $V_{\overline{SHDN}} = V_{VL}$ ,  $V_{CELL} = GND$ ,  $V_{BATT} = V_{CS} = 4.2V$ ,  $V_{VADJ} = V_{REF} / 2$ ,  $V_{ISETIN} = V_{ISETOUT} = V_{REF}$ ,  $R_{THM} = 10k\Omega$ ,  $T_A = 0^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
SUPPLY AND REFERENCE		-	r			
DCIN Input Voltage Range			6		28	V
DCIN Quiescent Supply Current		6V < V <sub>DCIN</sub> < 28V		5	7	mA
DCIN to BATT Dropout Threshold, DCIN Falling		Falling edge	0.075	0.125	0.175	V
DCIN to BATT Dropout Threshold, DCIN Rising		Rising edge	0.20	0.30	0.40	V
VL Output Voltage		$6V < V_{DCIN} < 28V$	5.10	5.40	5.70	V
VL Output Load Regulation		$I_{VL} = 0$ to 15mA		44	65	mV
REF Output Voltage	VREF	$6V < V_{DCIN} < 28V$	4.179	4.20	4.221	V
REF Line Regulation		$6V < V_{DCIN} < 28V$		2	6	mV
REF Load Regulation		I <sub>REF</sub> = 0 to 1mA		6	14	mV
SWITCHING REGULATOR						
PWM Oscillator Frequency	fosc	Nondropout fosc	270	300	330	kHz
LX Maximum Duty Cycle		In-dropout, fosc / 4	97	98		%
CSSN/CSSP Off-State Leakage		$V_{CSSN} = V_{CSSP} = V_{DCIN} = 28V, V_{\overline{SHDN}} = GND$		2	10	μA
HSD Off-State Leakage		$V_{LX} = PGND, V_{HSD} = V_{DCIN} = 28V, V_{\overline{SHDN}} = GND$		0.1	10	μA
LX Off-State Leakage		$V_{LX} = V_{HSD} = V_{DCIN} = 28V, V_{\overline{SHDN}} = GND$		0.1	10	μA
HSD to LX On-Resistance		$V_{BST} = V_{LX} + 4.5V$		260	450	mΩ
LX to PGND On-Resistance		See PWM Controller section		1	2	Ω
CS to BATT Current-Sensing Resistance	R <sub>CS</sub>	Internal resistor between CS and BATT, 1.5A RMS operating		110	170	mΩ
		V <del>SHDN</del> = GND, VBATT = 19V		0.1	5	μA
BATT, CS Input Current		CELL = REF, V <sub>BATT</sub> = 15V, any charging state		280	540	μA
		V <sub>BATT</sub> = 18V, done state		150	270	μA

## **ELECTRICAL CHARACTERISTICS (continued)**

(Circuit of Figure 1,  $V_{DCIN} = V_{HSD} = V_{CSSP} = V_{CSSN} = 18V$ ,  $V_{\overline{SHDN}} = V_{VL}$ ,  $V_{CELL} = GND$ ,  $V_{BATT} = V_{CS} = 4.2V$ ,  $V_{VADJ} = V_{REF} / 2$ ,  $V_{ISETIN} = V_{ISETOUT} = V_{REF}$ ,  $R_{THM} = 10k\Omega$ ,  $T_A = 0^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CS to BATT Hard Current Limit		Instantaneous peak current limit	2.4	2.7	3.0	Α
BATT, CS Input Voltage Range			0		19	V
VOLTAGE LIMIT ACCURACY	1					
Battery Regulation Voltage	VBATTR	CELL = float, GND, VL, or REF	4.167	4.2	4.233	V/cell
Absolute Voltage Accuracy		Not including VADJ resistor tolerances	-0.8		0.8	%
Absolute voltage Accuracy		With 1% VADJ resistors	-1		1	/0
BATT Regulation Voltage		V <sub>ADJ</sub> = GND	3.948	3.979	4.010	V/cel
Adjustment Range		V <sub>ADJ</sub> = REF	4.386	4.421	4.453	V/CEI
ERROR AMPLIFIERS						
CCV Amplifier Transconductance		$V_{CCV} = 2V$	0.4	0.7	1.0	mS × cells
CCV Amplifier Maximum Output Current		V <sub>CCV</sub> = 2V	±50			μA
BATT Full-Scale Charge Current			1.35	1.5	1.65	Α
BATT 1/10-Scale Charge Current (Note 1)		VISETOUT = V <sub>REF</sub> / 10	100	150	200	mA
BATT Charge Current in Prequalification State		V <sub>BATT</sub> < 2.4V per cell	100	150	200	mA
CCI Battery Current Sense Gain		$V_{CCI} = 2V$	60	130	240	μA/A
CCI Amplifier Maximum Output Current		V <sub>CCI</sub> = 2V	±100			μA
CSSP to CSSN Full-Scale Current-Sense Voltage			90	100	115	mV
CSSP to CSSN 1/10-Scale Current-Sense Voltage		VISETIN = VREF / 10	5	10	15	mV
CCS Amplifier Transconductance		V <sub>CCS</sub> = 2V	1.0	2.0	3.0	mS
CCS Amplifier Maximum Output Current		V <sub>CCS</sub> = 2V	±100			μA
CCI, CCS Clamp Voltage with Respect to CCV			25		200	mV
CCV Clamp Voltage with Respect to CCI, CCS			25		200	mV
STATE MACHINE	1	r	1			
THM Trip Threshold Voltage	VTRT	THM low-temp or high-temp current	1.386	1.40	1.414	V
THM Low-Temp Current	ITLTC	VTHM = 1.4V	46.2	49	51.5	μA
THM High-Temp Current	Ітнтс	V <sub>THM</sub> = 1.4V	344	353	362	μA
THM COLD Threshold Resistance (Note 2)		Combines THM low-temp current and THM threshold, VTRT / ITLTC	26.92	28.70	30.59	kΩ
THM HOT Threshold Resistance		Combines THM high-temp current and THM	3.819	3.964	4.115	kΩ

M/X/W

## **ELECTRICAL CHARACTERISTICS (continued)**

(Circuit of Figure 1,  $V_{DCIN} = V_{HSD} = V_{CSSP} = V_{CSSN} = 18V$ ,  $V_{\overline{SHDN}} = V_{VL}$ ,  $V_{CELL} = GND$ ,  $V_{BATT} = V_{CS} = 4.2V$ ,  $V_{VADJ} = V_{REF} / 2$ ,  $V_{ISETIN} = V_{ISETOUT} = V_{REF}$ ,  $R_{THM} = 10k\Omega$ ,  $T_A = 0^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
BATT Undervoltage Threshold (Note 3)			2.4	2.5	2.6	V/cell
BATT Overvoltage Threshold (Note 4)			4.55	4.67	4.8	V/cell
FULLCHG BATT Current Termination Threshold (Note 5)			250	330	400	mA
BATT Recharge Voltage Threshold (Note 6)			94	95	96	% of VBATTR x cell
TIMER1 and TIMER2 Oscillation Frequency			2.1	2.33	2.6	kHz
Prequalification Timer			6.25	7.5	8.75	min
Fast-Charge Timer			81	90	100	min
Full-Charge Timer			81	90	100	min
Top-Off Timer			40.5	45	49.8	min
Temperature Measurement Frequency			0.98	1.12	1.32	Hz
CONTROL INPUTS/OUTPUTS	1		I.			
SHDN Input Voltage High	VIH		1.4			V
SHDN Input Voltage Low	VIL				0.6	V
VADJ, ISETIN, ISETOUT Input Voltage Range			0		VREF	V
VADJ, ISETIN, ISETOUT Input Bias Current		VVADJ, VISETIN, VISETOUT = 0 or 4.2V	-50		50	nA
SHDN Input Bias Current		$V\overline{SHDN} = 0 \text{ or } V_{VL}$	-1		1	μA
CELL Input Bias Current		VCELL = 0 or VVL	-5		5	μA
ISETOUT Shutdown Threshold Voltage (Note 3)			150	220	300	mV
		For 1 cell	0		0.5	
		For 2 cells (floating)	1.5		2.5	
CELL Input Voltage		For 3 cells	V <sub>REF</sub> - 0.3	VF	REF + 0.3	V
		For 4 cells	VvL - 0.4		Vvl	

## **ELECTRICAL CHARACTERISTICS (continued)**

(Circuit of Figure 1,  $V_{DCIN} = V_{HSD} = V_{CSSP} = V_{CSSN} = 18V$ ,  $V_{\overline{SHDN}} = V_{VL}$ ,  $V_{CELL} = GND$ ,  $V_{BATT} = V_{CS} = 4.2V$ ,  $V_{VADJ} = V_{REF} / 2$ ,  $V_{ISETIN} = V_{ISETOUT} = V_{REF}$ ,  $R_{THM} = 10k\Omega$ ,  $T_A = 0^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
FASTCHG, FULLCHG, FAULT Output Low Voltage	V <sub>OL</sub>	I <sub>SINK</sub> = 5mA			0.5	V
FASTCHG, FULLCHG, FAULT Output High Leakage		$V_{FASTCHG}$ , $V_{FULLCHG}$ , $V_{FAULT} = 28V$ , $V_{SHDN} = GND$			1	μA

## **ELECTRICAL CHARACTERISTICS**

(Circuit of Figure 1,  $V_{DCIN} = V_{HSD} = V_{CSSP} = V_{CSSN} = 18V$ ,  $V_{\overline{SHDN}} = V_{VL}$ ,  $V_{CELL} = GND$ ,  $V_{BATT} = V_{CS} = 4.2V$ ,  $V_{VADJ} = V_{REF} / 2$ ,  $V_{ISETIN} = V_{ISETOUT} = V_{REF}$ ,  $R_{THM} = 10k\Omega$ ,  $T_{A} = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted.) (Note 7)

SUPPLY AND REFERENCE         DCIN Input Voltage Range         VL Output Voltage         REF Output Voltage         REF Output Voltage         REF Line Regulation         6V < VDCIN < 28V         SWITCHING REGULATOR         PWM Oscillator Frequency       fOSC         Nondropout fOSC         HSD to LX On-Resistance       VBST = VLX + 4.5V         LX to PGND On-Resistance       Instantaneous peak current limit         BATT, CS Input Voltage Range       Instantaneous peak current limit         Absolute Voltage Accuracy       Not including VADJ resistor tolerances         With 1% VADJ resistors       With 1% VADJ resistors         BATT Regulation Voltage       CELL = float, GND, VL, or REF         BATT full-Scale Charge Current       VSETOUT = VREF / 10         BATT Charge Current in Prequalification State       VBATT < 2.4V per cell	6 5.1 4.166 260 2.2 0 -0.8 -1	28 5.7 4.242 6 340 450 2 3.2 19 0.8 1	V           V           V           MV           kHz           mΩ           Ω           A           V           %
VL Output Voltage6VVDCIN < 28VREF Output Voltage6V < VDCIN < 28V	5.1 4.166 260 	5.7 4.242 6 340 450 2 3.2 19 0.8	V           V           mV           kHz           mΩ           Ω           A           V
REF Output Voltage6V < VDCIN < 28VREF Line Regulation6V < VDCIN < 28V	4.166 260 2.2 	4.242 6 340 450 2 3.2 19 0.8	V           mV           kHz           mΩ           Ω           A           V
REF Line Regulation6V < VDCIN < 28VSWITCHING REGULATORPWM Oscillator FrequencyfoscNondropout foscHSD to LX On-ResistanceVBST = VLX + 4.5VLX to PGND On-ResistanceCS to BATT Hard Current LimitInstantaneous peak current limitBATT, CS Input Voltage RangeACCURACY AND ERROR AMPLIFIERSAbsolute Voltage AccuracyNot including VADJ resistor tolerancesBATT Regulation VoltageCELL = float, GND, VL, or REFBATT Full-Scale Charge CurrentVSETOUT = VREF / 10BATT Charge Current in Prequalification StateVBATT < 2.4V per cell	260 2.2 0 -0.8	6 340 450 2 3.2 19 0.8	mV kHz mΩ Ω A V
SWITCHING REGULATOR         PWM Oscillator Frequency       fOSC       Nondropout fOSC         HSD to LX On-Resistance       VBST = VLX + 4.5V         LX to PGND On-Resistance       Instantaneous peak current limit         BATT, CS Input Voltage Range       Instantaneous peak current limit         ACCURACY AND ERROR AMPLIFIERS       Not including VADJ resistor tolerances         Absolute Voltage Accuracy       With 1% VADJ resistors         BATT Regulation Voltage       CELL = float, GND, VL, or REF         BATT Full-Scale Charge       VSETOUT = VREF / 10         BATT Charge Current in Prequalification State       VBATT < 2.4V per cell	2.2 0 -0.8	340 450 2 3.2 19 0.8	kHz mΩ Ω A V
PWM Oscillator FrequencyfOSCNondropout fOSCHSD to LX On-ResistanceVBST = VLX + 4.5VLX to PGND On-ResistanceInstantaneous peak current limitCS to BATT Hard Current LimitInstantaneous peak current limitBATT, CS Input Voltage RangeAccuracy AND ERROR AMPLIFIERSAbsolute Voltage AccuracyNot including VADJ resistor tolerancesBATT Regulation VoltageCELL = float, GND, VL, or REFBATT Full-Scale Charge CurrentVSETOUT = VREF / 10BATT Charge Current in Prequalification StateVBATT < 2.4V per cell	2.2 0 -0.8	450 2 3.2 19 0.8	mΩ Ω A V
HSD to LX On-ResistanceVBST = VLX + 4.5VLX to PGND On-ResistanceInstantaneous peak current limitCS to BATT Hard Current LimitInstantaneous peak current limitBATT, CS Input Voltage RangeACCURACY AND ERROR AMPLIFIERSAbsolute Voltage AccuracyNot including VADJ resistor tolerancesBATT Regulation VoltageCELL = float, GND, VL, or REFBATT Full-Scale Charge CurrentVSETOUT = VREF / 10BATT Charge Current in Prequalification StateVBATT < 2.4V per cell	2.2 0 -0.8	450 2 3.2 19 0.8	mΩ Ω Α V
LX to PGND On-Resistance       Instantaneous peak current limit         CS to BATT Hard Current Limit       Instantaneous peak current limit         BATT, CS Input Voltage Range       Accuracy AND ERROR AMPLIFIERS         Absolute Voltage Accuracy       Not including VADJ resistor tolerances         BATT Regulation Voltage       CELL = float, GND, VL, or REF         BATT Full-Scale Charge Current       VSETOUT = VREF / 10         BATT Charge Current in Prequalification State       VBATT < 2.4V per cell	-0.8	2 3.2 19 0.8	Ω A V
CS to BATT Hard Current Limit       Instantaneous peak current limit         BATT, CS Input Voltage Range       Instantaneous peak current limit         ACCURACY AND ERROR AMPLIFIERS       Not including VADJ resistor tolerances         Absolute Voltage Accuracy       With 1% VADJ resistors         BATT Regulation Voltage       CELL = float, GND, VL, or REF         BATT Full-Scale Charge Current       VSETOUT = VREF / 10         BATT Charge Current in Prequalification State       VBATT < 2.4V per cell	-0.8	3.2 19 0.8	A V
BATT, CS Input Voltage Range       Not including VADJ resistor tolerances         Absolute Voltage Accuracy       Not including VADJ resistor tolerances         BATT Regulation Voltage       CELL = float, GND, VL, or REF         BATT Full-Scale Charge Current       VSETOUT = VREF / 10         BATT Charge Current in Prequalification State       VBATT < 2.4V per cell	-0.8	19 0.8	V
ACCURACY AND ERROR AMPLIFIERS         Absolute Voltage Accuracy       Not including VADJ resistor tolerances         BATT Regulation Voltage       CELL = float, GND, VL, or REF         BATT Full-Scale Charge Current       BATT 1/10-Scale Charge         BATT Not including VADJ resistors       VSETOUT = VREF / 10         BATT Charge Current in Prequalification State       VBATT < 2.4V per cell	-0.8	0.8	
Absolute Voltage Accuracy       Not including VADJ resistor tolerances         BATT Regulation Voltage       CELL = float, GND, VL, or REF         BATT Full-Scale Charge Current       BATT 1/10-Scale Charge         BATT 1/10-Scale Charge       VSETOUT = VREF / 10         BATT Charge Current in Prequalification State       VBATT < 2.4V per cell	0.0		%
Absolute Voltage Accuracy     With 1% VADJ resistors       BATT Regulation Voltage     CELL = float, GND, VL, or REF       BATT Full-Scale Charge Current     BATT 1/10-Scale Charge       Current (Note 1)     VSETOUT = VREF / 10       BATT Charge Current in Prequalification State     VBATT < 2.4V per cell	0.0		%
With 1% VADJ resistorsBATT Regulation VoltageCELL = float, GND, VL, or REFBATT Full-Scale Charge CurrentBATT 1/10-Scale Charge Current (Note 1)VSETOUT = VREF / 10BATT Charge Current in Prequalification StateVBATT < 2.4V per cell	-1	- 1	- 70
BATT Full-Scale Charge Current         BATT 1/10-Scale Charge Current (Note 1)         VSETOUT = VREF / 10         BATT Charge Current in Prequalification State		I	
BATT 1/10-Scale Charge Current (Note 1)     VSETOUT = VREF / 10       BATT Charge Current in Prequalification State     VBATT < 2.4V per cell	4.158	4.242	V/cell
Current (Note 1)     VSETOUT = VREF / 10       BATT Charge Current in     VBATT < 2.4V per cell	1.3	1.7	A
Prequalification State VBATT < 2.4V per cell	100	200	mA
	100	200	mA
CSSP to CSSN Full-Scale Current-Sense Voltage	85	115	mV
CSSP to CSSN 1/10-Scale Current-Sense Voltage VSETIN = VREF / 10	5	15	mV
STATE MACHINE			
THM Trip Threshold Voltage V <sub>TRT</sub> THM low-temp or high-temp current	1.386	1.414	V
THM Low-Temp Current ITLTC VTHM = 1.4V	1.500		μA

<b>ELECTRICAL CHARACTERISTICS (</b>	continued)
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(Circuit of Figure 1,  $V_{DCIN} = V_{HSD} = V_{CSSP} = V_{CSSN} = 18V$ ,  $V_{\overline{SHDN}} = V_{VL}$ ,  $V_{CELL} = GND$ ,  $V_{BATT} = V_{CS} = 4.2V$ ,  $V_{VADJ} = V_{REF} / 2$ ,  $V_{ISETIN} = V_{ISETOUT} = V_{REF}$ ,  $R_{THM} = 10k\Omega$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
BATT Undervoltage Threshold (Note 3)			2.4		2.6	V/cell
BATT Overvoltage Threshold (Note 4)			4.55		4.8	V/cell
FULLCHG BATT Current Termination Threshold (Note 5)			250		400	mA
Temperature Measurement Frequency			0.93		1.37	Hz
CONTROL INPUTS/OUTPUTS						
SHDN Input Voltage High	VIH		1.4			V
SHDN Input Voltage Low	VIL				0.6	V

**Note 1:** When  $V_{ISETOUT} = 0$ , battery charger turns off.

Note 2: See Thermistor section.

Note 3: Below this threshold, charger reverts to a prequalification mode with IBATT reduced to 10% of full scale.

Note 4: Above this threshold, charger is disabled.

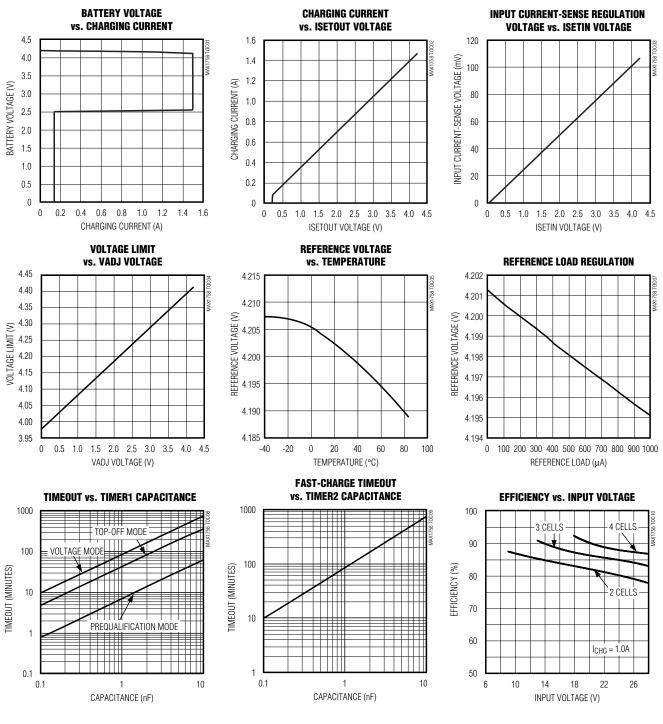
Note 5: After full-charge state is complete and peak inductor current falls below this threshold, FULLCHG output switches high. Battery charging continues until top-off timeout occurs. See Table 1.

Note 6: After charging is complete, when BATT voltage falls below this threshold, a new charging cycle is initiated.

Note 7: Specifications to -40°C are guaranteed by design, not production tested.

## **Typical Operating Characteristics**

(Circuit of Figure 1,  $V_{DCIN} = 18V$ ,  $V_{\overline{SHDN}} = V_{VL}$ ,  $V_{CELL} = GND$ ,  $V_{VADJ} = V_{REF}/2$ ,  $V_{ISETIN} = V_{ISETOUT} = V_{REF}$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.)



**MAX1758** 

## **Pin Description**

PIN	NAME	FUNCTION				
PIN	NAME					
1	VL	Chip Power Supply. Output of the 5.4V linear regulator from DCIN. Bypass VL to GND with 2.2 $\mu$ F or larger ceramic capacitor.				
2	ISETIN Input Current Limit Adjust. Use a voltage-divider to set the voltage between 0 and V <sub>REF</sub> . See <i>Input Regulator</i> section.					
3	ISETOUT	Battery Charging Current Adjust. Use a voltage-divider to set the voltage between 0 and V <sub>REF</sub> . See <i>Charging Current Regulator</i> section.				
4	THM Thermistor Input. Connect a thermistor from THM to GND to set qualification temperature range. If unus connect a 10k $\Omega$ resistor from THM to GND. See <i>Thermistor</i> section.					
5	REF	4.2V Reference Voltage Output. Bypass REF to GND with 1µF or larger ceramic capacitor.				
6	GND	Analog Ground				
7	7     VADJ     Voltage Adjustment. Use a voltage-divider to set the voltage between 0 and VREF to adjust the batter ulation voltage by ±5%. See Battery Regulation Voltage section.					
8	BATT	Battery Voltage-Sense Input and Current-Sense Negative Input				
9, 10	HSD	High-Side Drain. This is the drain of the internal high-side FET. See Figure 3.				
11	CELL	Cell-Count Programming Input. Connect CELL to GND, REF, or VL to set 1, 3, or 4 cells, or leave uncon- nected to set 2 cells.				
12	TIMER1	Timer1 Adjustment. Connect a capacitor from TIMER1 to GND to set the prequalification, full-charge, and top-off times. See <i>Timers</i> section.				
13	TIMER2	Timer2 Adjustment. Connect a capacitor from TIMER2 to GND to set the fast-charge time. See <i>Timers</i> section.				
14	FAULT	Charge Fault Indicator. Open-drain output pulls low when charging terminates abnormally. See Table 1.				
15	FASTCHG	Fast-Charge Indicator. Open-drain output pulls low when charging with constant current.				
16	FULLCHG	Full-Charge Indicator. Open-drain output pulls low when charging with constant voltage in full-charge state.				
17	SHDN	Shutdown Input. Drive SHDN low to disable charging. Connect SHDN to VL for normal operation.				
18	PGND	Power Ground. Current from the low-side power MOSFET switch source flows through PGND.				
19, 20	LX	Power Inductor Switching Node and High-Side Power MOSFET Source				
21	CS	Battery Current-Sense Positive Input. Connects to internal 0.1 $\Omega$ resistor between BATT and CS.				
22	BST	High-Side MOSFET Gate Drive Bias. Connect a $0.1\mu$ F capacitor from BST to LX.				
23	CCS	Charger Source Current Regulation Loop Compensation Point. See Compensation section.				
24	CCI	Battery Charge Current Regulation Loop Compensation Point. See Compensation section.				
25	CCV	Voltage Regulation Loop Compensation Point. See Compensation section.				
26	CSSN	Source Current-Sense Negative Input. See Input Current Regulator section.				
27	CSSP	Source Current-Sense Positive Input. See Input Current Regulator section.				
28	DCIN	Power-Supply Input. DCIN is the input supply for the VL regulator. Bypass DCIN to GND with a 0.1µF or greater capacitor. See <i>Detailed Description</i> .				

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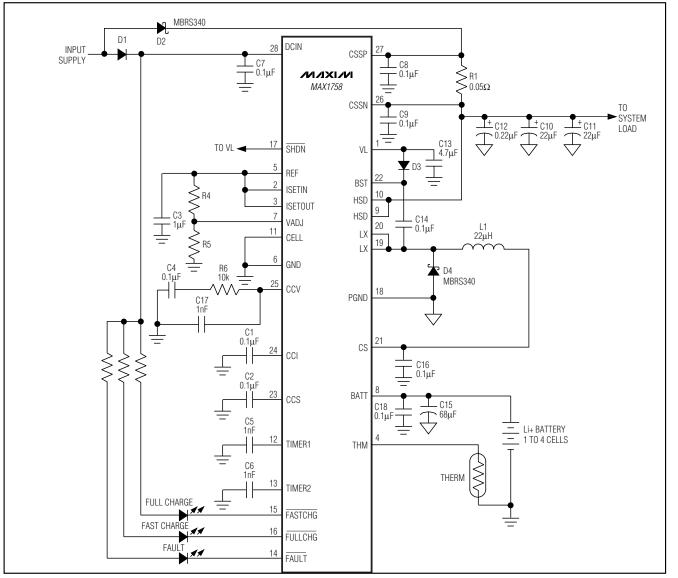


Figure 1. Typical Application Circuit

### **Detailed Description**

The MAX1758 includes all of the functions necessary to charge 1, 2, 3, or 4 Li+ battery cells in series. It includes a step-down DC-DC converter that controls charging voltage and current. It also includes input source current limiting, battery temperature monitoring, battery undervoltage precharging, battery fault indication, and a state machine with timers for charge termination.

The DC-DC converter uses an internal power MOSFET switch to convert the input voltage to the charging current or voltage. Figure 1 shows the typical application circuit. Figure 2 shows a typical charging sequence and Figure 3 shows the functional diagram. The charging current is set by the voltage at ISETOUT. The battery voltage is measured at the BATT pin. The battery regulation voltage limit is set to 4.2V per cell and can be adjusted  $\pm$ 5% by changing the voltage at the VADJ pin. By limiting the adjust range, the voltage limit accuracy is better than 1% while using 1% setting resistors.

**MAX1758** 

## Table 1. Charging State Table

STATE	ENTRY CONDITIONS	STATE CONDITIONS
Reset	From initial power-on or from done state if battery voltage < recharge volt- age threshold or $V_{DCIN}$ - $V_{BATT}$ < dropout threshold or $V_{BATT}$ > battery overvoltage threshold	Timers reset, charging current = 0, $\overline{FASTCHG}$ = high, $\overline{FULLCHG}$ = high, $\overline{FAULT}$ = high
Prequalification	From reset state if input power, reference, and inter- nal bias are within limits	Battery voltage ≤ undervoltage threshold, charging current = (fast-charge current / 10), timeout = 7.5min typ (C <sub>TIMER1</sub> = 1nF), <u>FASTCHG</u> = low, <u>FULLCHG</u> = high, <u>FAULT</u> = high
Fast Charge (Constant Current)	From prequalification state if battery voltage > undervoltage threshold	Undervoltage threshold ≤ battery voltage ≤ battery regulation voltage, charging current = charge current limit, timeout = 90min typ (C <sub>TIMER2</sub> = 1nF), <u>FASTCHG</u> = low, <u>FULLCHG</u> = high, <u>FAULT</u> = high
Full Charge (Constant Voltage)	From fast-charge state if battery voltage = battery regulation voltage	Battery voltage = battery regulation voltage, charging current ≤ current limit, timeout = 90min typ (C <sub>TIMER1</sub> = 1nF), <u>FASTCHG</u> = high, <u>FULLCHG</u> = low, <u>FAULT</u> = high
Top-Off (Constant Voltage)	From full-charge state if full-charge timer expires <b>or</b> if charging current ≤ 330mA	Battery voltage = battery regulation voltage, charging current $\leq$ 330mA, timeout = 45min typ (C <sub>TIMER1</sub> = 1nF), FASTCHG = high, FULLCHG = high, FAULT = high
Done	From top-off state if top-off timer expires	Recharge voltage threshold ≤ battery, voltage ≤ voltage limit, charging current = 0, FASTCHG = high, FULLCHG = high, FAULT = high
Over/Undertemperature	From fast-charge state or full-charge state if battery temperature is outside limits	Charge current = 0, timers suspended, FASTCHG = no change, FULLCHG = no change, FAULT = no change
Fault	From reset state if battery temperature ≥ maximum battery temperature or from prequalification state if prequalification timer expires or from fast-charge state if fast-charge timer expires	Charging current = 0, FASTCHG = high, FULLCHG = high, FAULT = low

The MAX1758 includes a state machine that controls the charging algorithm. Figure 4 shows the state diagram. Table 1 is the charging state table. When power is applied, or SHDN input is driven high, the part goes into the reset state where the timers are reset to zero to prepare for charging. From the reset state, it enters the pregualification state. In this state, 1/10 of the fastcharge current charges the battery, and the battery temperature and voltage are measured. If the voltage is above the undervoltage threshold and the temperature is within the limits, then it will enter the fast-charge state. If the battery voltage does not rise above the undervoltage threshold before the prequalification timer expires, the charging terminates and the FAULT output goes low. The prequalification time is set by the TIMER1 capacitor (CTIMER1). If the battery is outside the temperature limits, charging and the timer are suspended. Once the temperature is back within limits, charging and the timer resume.

In the fast-charge state, the FASTCHG output goes low and the batteries charge with a constant current (see *Charging Current Regulator* section). If the battery voltage reaches the voltage limit before the fast timer expires, the part enters the full-charge state. If the fastcharge timer expires before the voltage limit is reached, charging terminates and the FAULT output goes low. The fast-charge time limit is set by the TIMER2 capacitor (CTIMER2). If the battery temperature is outside the limits, charging pauses and the timers are suspended until the temperature returns to within the limits.

In the full-charge state, the FULLCHG output goes low and the batteries charge at a constant voltage (see the *Voltage Regulation* section). When the charging current drops below 150mA (330mA peak inductor current), or if the full-charge timer expires, the state machine enters the top-off state. In the top-off state, the batteries continue to charge at a constant voltage until the top-off timer expires when it enters the done state. In the done state, charging stops until the battery voltage drops below the recharge-voltage threshold when it enters the reset state to start the charging process again. In the full-charge or the top-off state, if the battery temperature is outside the limits, charging pauses and the timers are suspended until the battery temperature returns to within limits.

#### Voltage Regulator

Li+ batteries require a high-accuracy voltage limit while charging. The MAX1758 uses a high-accuracy voltage regulator (±0.8%) to limit the charging voltage. The battery regulation voltage is nominally set to 4.2V per cell and can be adjusted ±5% by changing the voltage at



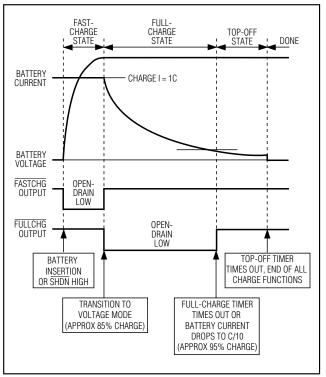


Figure 2. Charge State and Indicator Output Timing for a Typical Charging Sequence

the V<sub>ADJ</sub> pin between reference voltage and ground. By limiting the adjust range of the regulation voltage, an overall voltage accuracy of better than 1% is maintained while using 1% resistors. CELL sets the cell count from 1-to-4 series cells (see *Setting the Battery Regulation Voltage* section).

An internal error amplifier (GMV) maintains voltage regulation (Figure 3). The GMV amplifier is compensated at CCV. The component values shown in Figure 1 provide suitable performance for most applications. Individual compensation of the voltage regulation and current regulation loops allows for optimum stability.

#### **Charging Current Regulator**

The charging current-limit regulator limits the charging current. Current is sensed by measuring the voltage across the internal current-sense resistor R<sub>CS</sub> between BATT and CS. The voltage at ISETOUT adjusts the charging current. Full-scale charging current is achieved when ISETOUT is connected to REF.

The charging current error amplifier (GMI) is compensated at CCI. A  $0.1\mu$ F capacitor at CCI provides suitable performance for most applications.



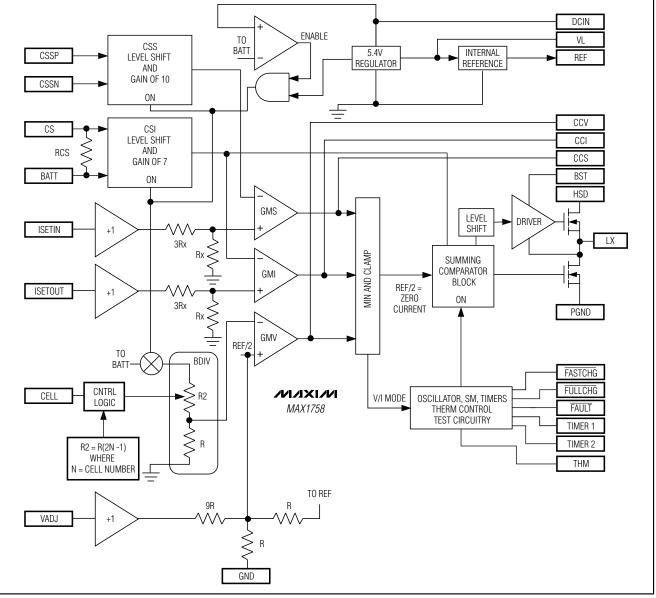


Figure 3. MAX1758 Functional Diagram

#### **Input Current Regulator**

The total input current (from a wall cube or other DC source) is the sum of system load current plus the battery-charging current. The input current regulator limits the source current by reducing charging current when input current exceeds the set input current limit. System current will normally fluctuate as portions of the system are powered up or put to sleep. Without input current regulation, the input source must be able to supply the

maximum system load current plus the maximum charger input current. By using the input current limiter, the current capability of the AC wall adapter may be lowered, reducing system cost.

Input current is measured through an external sense resistor at CSSP and CSSN. The voltage at ISETIN also adjusts the input current limit. Full-scale input current is achieved when ISETIN is connected to REF, setting the full-scale current-sense regulation voltage to 100mV.



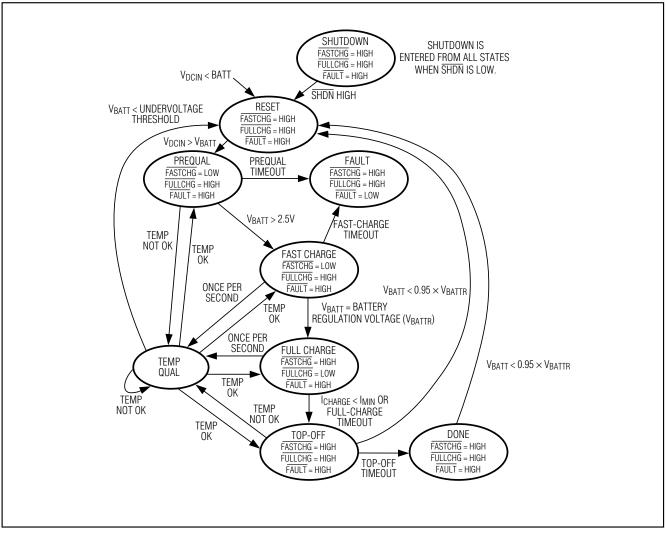


Figure 4. State Diagram

When the current-sense resistor is chosen, note that the voltage drop across this resistor adds to the power loss, reducing efficiency. Reducing the voltage across the current-sense resistor may degrade input current limit accuracy due to the input offset of the input current-sense amplifier.

The input current error amplifier (GMS) is compensated at CCS. A  $0.1\mu$ F capacitor at CCS provides suitable performance for most applications.

#### **PWM Controller**

The PWM controller drives the internal high-side MOS-FET to control charging current or voltage. The input to the PWM controller is the lowest of CCI, CCV, or CCS.

M/X/W

An internal clamp limits the noncontrolling signals to within 200mV of the controlling signal to prevent delay when switching between regulation loops.

The current mode PWM controller measures the inductor current to regulate the output voltage or current, simplifying stabilization of the regulation loops. Separate compensation of the regulation circuits allows each to be optimally stabilized. Internal slope compensation is included, ensuring stable operation over a wide range of duty cycles.

The controller drives an internal N-channel MOSFET switch to step the input voltage down to the battery voltage. The high-side MOSFET gate is driven to a voltage higher than the input source voltage by a bootstrap **MAX1758** 

**MAX1758** 

capacitor. This capacitor (between BST and LX) is charged through a diode from VL when LX is low. An internal N-channel MOSFET turns on momentarily after the high-side switch turns off, pulling LX to PGND to ensure that the bootstrap capacitor charges. The highside MOSFET gate is driven from BST, supplying sufficient voltage to fully drive the MOSFET gate even when its source is near the input voltage.

#### **Timers**

The MAX1758 includes safety timers to terminate charging and to ensure that faulty batteries are not charged indefinitely. TIMER1 and TIMER2 set the time-out periods.

TIMER1 controls the maximum prequalification time, maximum full-charge time, and the top-off time. TIMER2 controls the maximum fast-charge time. The timers are set by external capacitors. The typical times of 7.5 minutes for prequalification, 90 minutes for full charge, 45 minutes for top-off, and 90 minutes for fast charge are set by using a 1nF capacitor on TIMER1 and TIMER2 (Figure 1).

#### **Charge Monitoring Outputs**

FASTCHG, FULLCHG, and FAULT are open-drain outputs that can be used as LED drivers. FASTCHG indicates the battery is being fast charged. FULLCHG indicates the charger has completed the fast-charge cycle (approximately 85% charge) and is operating in voltage mode. The FASTCHG and FULLCHG outputs can be tied together to indicate charging or done (Figure 2). FAULT indicates the charger has detected a charging fault and that charging has terminated. The charger can be brought out of the FAULT condition only by removing and reapplying the input power, or by pulling SHDN low.

Thermistor The intent of THM is to inhibit charging when the battery is too cold or too hot (+2.5°C  $\leq$  TOK  $\leq$  +47.5°C), using an external thermistor. THM time multiplexes two sense currents to test for both hot and cold qualification. The thermistor should be  $10k\Omega$  at +25°C and have a negative temperature coefficient (NTC); the THM pin expects 3.97k $\Omega$  at +47.5°C and 28.7k $\Omega$  at +2.5°C. Connect the thermistor between THM and GND. If no temperature qualification is desired, replace the thermistor with a  $10k\Omega$  resistor. Thermistors by Philips/BC components (2322-640-63103), Cornerstone Sensors (T101D103-CA), and Fenwall Electronics (140-103LAG-RB1) work well. The battery temperature is measured at a 1.12Hz rate (CTIMER1 = CTIMER2 = 1nF). Charging pauses briefly to allow accurate measurement.

### Table 2. Cell-Count Programming Table

CELL	CELL COUNT (N)
GND	1
Float	2
REF	3
VL	4

If the temperature goes out of limits while charging is in progress, charging will be suspended until the temperature returns to within the limits. While charging is suspended, the timers will also be suspended but will continue counting from where they left off when charging resumes.

#### Shutdown

When SHDN is pulled low, the MAX1758 enters the shutdown mode and charging is stopped. In shutdown, the internal resistive voltage-divider is removed from BATT to reduce the current drain on the battery to less than 5 $\mu$ A. The high-side power MOSFET switch is off. However, the internal linear regulator (VLO) and the reference (REF) remain on. Status outputs FASTCHG, FULLCHG, and FAULT are high impedance. When exiting the shutdown mode, the MAX1758 goes to the power-on reset state, which resets the timers and begins a new charge cycle.

**Source Undervoltage Shutdown (Dropout)** If the voltage on DCIN drops within 100mV of the voltage on BATT, the charger turns off. This prevents battery discharge by the charger during low input voltage conditions.

## **Design Procedure**

### **Setting the Battery Regulation Voltage**

VADJ sets the per-cell voltage limit. To set the VADJ voltage, use a voltage-divider from REF to VADJ. A GND-to-V<sub>REF</sub> change at VADJ results in a ±5% change in the battery limit voltage. Since the full VADJ range results in only a 10% change on the battery regulation voltage, the resistor-divider's accuracy need not be as high as the output-voltage accuracy. Using 1% resistors for the voltage dividers results in no more than 0.1% degradation in output-voltage accuracy. VADJ is internally buffered so that high-value resistors can be used. Set V<sub>VADJ</sub> by choosing a value less than 100k $\Omega$  for R5 (Figure 1) from V<sub>ADJ</sub> to GND. The per-cell battery termination voltage is a function of the battery chemistry and construction; thus, consult the battery manufacturer to determine this voltage.

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cell voltage limit battery regulation voltage is determined, the VADJ voltage is calculated by the equation:

CELL is the programming input for selecting cell count N. Table 2 shows how CELL is connected to charge 1, 2, 3, or 4 cells.

#### **Setting the Charging Current Limit**

A resistor-divider from REF to GND sets the voltage at ISETOUT (VISETOUT). This determines the charging current during the current-regulation (fast-charge) mode. The full-scale charging current is 1.5A.

The charging current (ICHG) is, therefore:

$$I_{CHG} = 1.5A\left(\frac{V_{SETOUT}}{V_{REF}}\right)$$

Connect ISETOUT to REF to get the full-scale current limit.

#### Setting the Input Current limit

A resistor-divider from REF to GND sets the voltage at ISETIN (VISETIN). This sets the maximum source current allowed at any time during charging. The source current IFSS is set by the current-sense resistor RSOURCE between CSSP and CSSN. The full-scale source current is IFSS = 0.1V / R1 (Figure 1).

The input current limit (IIN) is therefore:

$$I_{\text{IN}} = I_{\text{FSS}} \left( \frac{V_{\text{ISETIN}}}{V_{\text{REF}}} \right)$$

Connect ISETIN to REF to get the full-scale input current limit. Short CSSP and CSSN if the input source current limit is not used.

In choosing the current-sense resistor, note that the drop across this resistor adds to the power loss and thus reduces efficiency. However, too low a resistor value may degrade input current-limit accuracy.

#### Inductor Selection

The inductor value may be changed for more or less ripple current. The higher the inductance, the lower the ripple current will be; however, as the physical size is kept the same, typically, higher inductance will result in higher series resistance and lower saturation current. A good tradeoff is to choose the inductor so that the ripple current is approximately 30% to 50% of the DC average charging current. The ratio of ripple current to

M/X/W

DC charging current (LIR) can be used to calculate the optimal inductor value:

$$= \frac{V_{BATT}(V_{DCIN(MAX)} - V_{BATT})}{V_{DCIN(MAX)} \times f_{OSC} \times I_{CHG} \times LIF}$$

where f<sub>OSC</sub> is the switching frequency (300kHz). The peak inductor current is given by:

$$I_{\text{PEAK}} = I_{\text{ISETOUT}} \left( 1 + \frac{\text{LIR}}{2} \right)$$

#### **Capacitor Selection**

The input capacitor shunts the switching current from the charger input and prevents that current from circulating through the source, typically an AC wall cube. Thus, the input capacitor must be able to handle the input RMS current. Typically, at high charging currents, the converter will operate in continuous conduction (the inductor current does not go to 0). In this case, the RMS current of the input capacitor may be approximated by the equation:

$$I_{CIN} \cong I_{CHG} \sqrt{D - D^2}$$

where:

ICIN is the input capacitor RMS current.

D is the PWM converter duty ratio (typically  $V_{\text{BATT}}$  /  $V_{\text{DCIN}}$ ).

ICHG is the battery charging current.

The maximum RMS input current occurs at 50% duty cycle; thus, the worst-case input ripple current is  $0.5 \times I_{CHG}$ . If the input-to-output voltage ratio is such that the PWM controller will never work at 50% duty cycle, then the worst-case capacitor current will occur where the duty cycle is nearest 50%.

The input capacitor impedance is critical to preventing AC currents from flowing back into the wall cube. This requirement varies depending on the wall cube impedance and the requirements of any conducted or radiated EMI specifications that must be met. Aluminum electrolytic capacitors are generally the cheapest, but usually are a poor choice for portable devices due to their large size and poor equivalent series resistance (ESR). Tantalum capacitors are better in most cases, as are high-value ceramic capacitors. For equivalent size and voltage rating, tantalum capacitors will have higher capacitance, but also higher ESR than ceramic capacitors. This makes consideration of RMS current and power

**MAX1758** 

dissipation ratings more critical when using tantalum capacitors.

The output filter capacitor is used to absorb the inductor ripple current. The output capacitor impedance must be significantly less than that of the battery to ensure that it will absorb the ripple current. Both the capacitance and ESR rating of the capacitor are important for its effectiveness as a filter and to ensure stability of the PWM circuit. The minimum output capacitance for stability is:

$$C_{OUT} > \frac{V_{REF} \left(1 + \frac{V_{BATT}}{V_{DCIN(MIN)}}\right)}{V_{BATT} \times f_{OSC} \times R_{CS}}$$

where:

COUT is the total output capacitance.

VREF is the reference voltage (4.2V).

VBATT is the maximum battery regulation voltage (typically 4.2V per cell).

V<sub>DCIN (MIN)</sub> is the minimum source input voltage.

The maximum output capacitor ESR required for stability is:

$$R_{ESR} < \frac{R_{CS} \times V_{BATT}}{V_{REF}}$$

where:

RESR is the output capacitor ESR.

RCs is the current-sense resistor from CS to BATT (100m $\Omega$  typ).

#### Setting the Timers

The MAX1758 contains four timers: a prequalification timer, fast-charge timer, full-charge timer, and top-off timer. Connecting a capacitor from TIMER1 to GND and TIMER2 to GND sets the timer periods. The TIMER1 input controls the prequalification, full-charge, and top-off times, while TIMER2 controls the fast-charge timeout. The typical timeouts for a 1C charge rate are set to 7.5 minutes for the prequalification timer, 90 minutes for the fast-charge timer, and 45 minutes for the top-off timer by connecting 1nF capacitors to TIMER1 and TIMER2. Each timer period is directly proportional to the capacitance at the corresponding pin (see *Typical Operating Characteristics*).

#### **Compensation**

Each of the three regulation loops—the input current limit, the charging current limit, and the charging voltage limit—can be compensated separately at the CCS, CCI, and CCV pins, respectively.

The charge-current loop error amp output is brought out at CCI. Likewise, the source-current error amplifier output is brought out at CCS. The current loops in most charger designs can be compensated by  $0.1\mu$ F capacitors to ground at CCI and CCS. Raising the value of these capacitors reduces the bandwidth of these loops.

The voltage-regulating loop error amp output is brought out at CCV. Compensate this loop by connecting a capacitor in parallel with a series resistor-capacitor (RC) from CCV to GND. Recommended values are shown in Figure 1.

## **Applications Information**

#### **Diode Selection**

A Schottky rectifier with a rating of at least 1.5A must be connected from LX to PGND.

#### VL and REF Bypassing

The MAX1758 uses an internal linear regulator to drop the input voltage down to 5.4V, which powers the internal circuitry. The output of the linear regulator is the VL pin. The internal linear regulator may also be used to power external circuitry as long as the maximum current of the linear regulator is not exceeded.

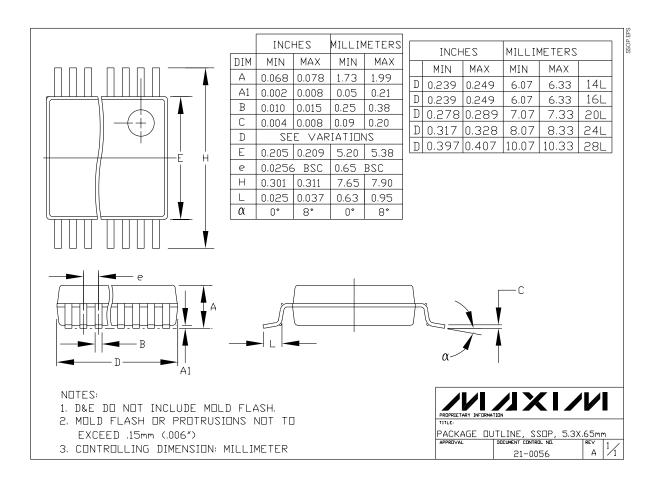
A 4.7 $\mu$ F bypass capacitor is required at VL to ensure that the regulator is stable. A 1 $\mu$ F bypass capacitor is also required between REF and GND to ensure that the internal 4.2V reference is stable. In both cases, use a low-ESR ceramic capacitor.

## Chip Information

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TRANSISTOR COUNT: 5996

## \_Package Information



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