3A Low Dropout Positive Regulators

PRODUCTION DATA SHEET

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Power Dissipation	Internally Limited
Input Voltage	10V
Input to Output Voltage Differential	10V
Operating Junction Temperature	150°C
Storage Temperature Range	-65°C to 150 °C
Peak Package Solder Reflow Temp (40 seconds max. exposure)	260°C (+0, -5)

Note 1: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

THERMAL DATA

DD Plastic TO-263 3-Pin

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	60°C/W
THERMAL RESISTANCE-JUNCTION TO TAB, θ_{JT}	2.7°C/W

P Plastic TO-220 3-Pin

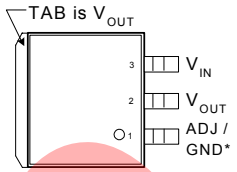
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	60°C/W
THERMAL RESISTANCE-JUNCTION TO TAB, θ_{JT}	2.7°C/W

DT Plastic TO-252 3-Pin

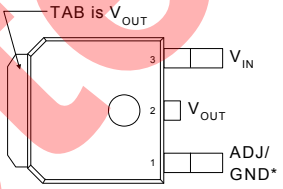
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	60°C/W
THERMAL RESISTANCE-JUNCTION TO TAB, θ_{JT}	2.7°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JT})$.
The θ_{JA} & θ_{JT} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

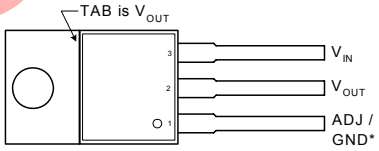
PACKAGE PIN OUT



DD PACKAGE (3-PIN)
(Top View)



DT PACKAGE (3-PIN)
(Top View)

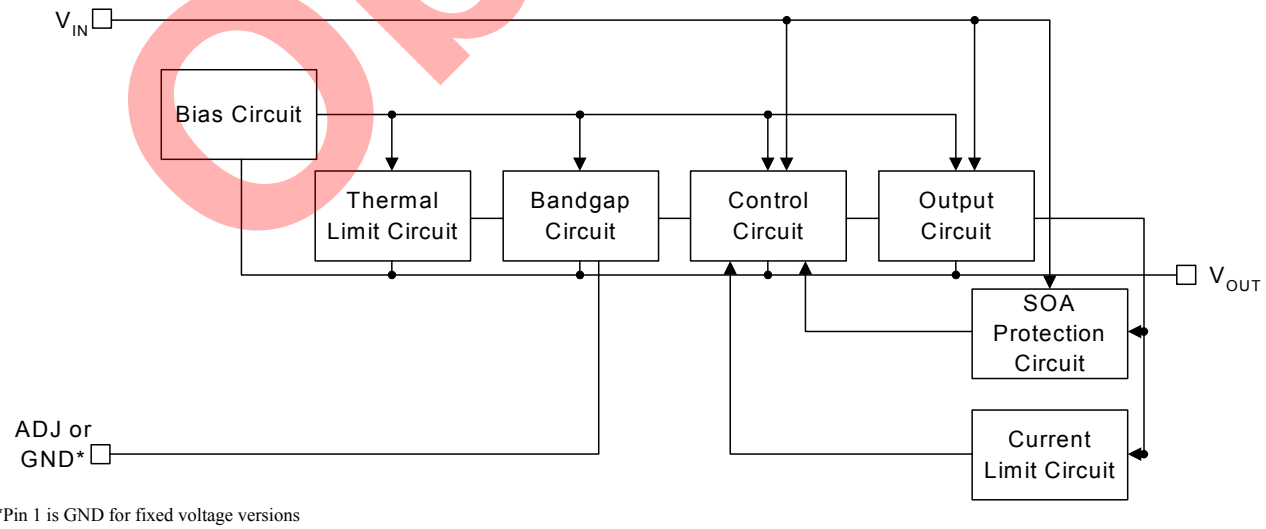


P PACKAGE (3-PIN)
(Top View)

*Pin 1 is GND for fixed voltage versions

RoHS 100% Matte Tin Lead Finish

BLOCK DIAGRAM



*Pin 1 is GND for fixed voltage versions

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature for the LX8385x-xxC with 0°C ≤ T_A ≤ 125°C and the LX8385-xxI with -25°C ≤ T_A ≤ 125°C except where otherwise noted. Test conditions: V_{IN} -V_{OUT} = 3V; I_{OUT} = 3A. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

Parameter	Symbol	Test Conditions	LX8385x-xx Min	LX8385x-xx Typ	LX8385x-xx Max	Units
LX8385-00 / 8385A-00 / 8385B-00 (ADJUSTABLE)						
Reference Voltage (Note 4) LX8385/85A-00	V_{REF}	I_{OUT} = 10mA, T_A = 25°C	1.238	1.250	1.262	V
		10mA ≤ I_{OUT} ≤ 3A, 1.5V ≤ (V_{IN} -V_{OUT}), V_{IN} ≤ 10V, P ≤ P_{MAX}	1.225	1.250	1.270	V
LX8385B-00		I_{OUT} = 10mA, T_A = 25°C	1.240	1.250	1.260	V
		10mA ≤ I_{OUT} ≤ 3A, 1.5V ≤ (V_{IN} -V_{OUT}), V_{IN} ≤ 10V, P ≤ P_{MAX}	1.238	1.250	1.262	V
Line Regulation (Note 2)	Δ V_{REF} (V_{IN})	1.5V ≤ (V_{IN} -V_{OUT}), V_{IN} ≤ 7V, I_{OUT} = 10mA		0.015	0.2	%
Load Regulation (Note 2)	Δ V_{REF} (I_{OUT})	V_{OUT} ≥ V_{REF}, V_{IN} - V_{OUT} = 3V, 10mA ≤ I_{OUT} ≤ 3A		0.15	0.5	%
Thermal Regulation	$ΔV_{OUT}$ (Pwr)	T_A = 25°C, 20ms pulse		0.01	0.04	% / W
Ripple Rejection (Note 3)		V_{OUT} = 5V, f= 120Hz, C_{OUT} = 100µF Tantalum, V_{IN} = 6.5V, C_{ADJ} = 10µF, I_{OUT} = 3A	65	83		dB
Adjust Pin Current	I_{ADJ}			55	100	µA
Adjust Pin Current Change (Note 4)	$ΔI_{ADJ}$	10mA ≤ I_{OUT} ≤ $I_{OUT(MAX)}$, 1.5V ≤ (V_{IN} -V_{OUT}), V_{IN}≤10V		0.2	5	µA
Dropout Voltage LX8385-00	ΔV	$ΔV_{REF}$ = 1%, I_{OUT} = 3A		1.2	1.5	V
LX8385A/85B-00		$ΔV_{REF}$ = 1%, I_{OUT} = 3A		1.1	1.3	V
Minimum Load Current	$I_{OUT(MIN)}$	V_{IN} ≤ 10V		2	10	mA
Maximum Output Current	$I_{OUT(MAX)}$	(V_{IN} - V_{OUT}) ≤ 7V, V_{IN} ≤ 10V	3	3.5		A
Long Term Stability (Note 3)	$ΔV_{OUT}$(t)	T_A = 125°C, 1000 hours		0.3	1	%
Temperature Stability (Note 3)	$ΔV_{OUT}$(T)			0.25		%
RMS Output Noise (% of V_{OUT}) (Note 3)	$ΔV_{OUT(RMS)}$	T_A = 25°C, 10Hz ≤ f ≤ 10kHz		0.003		%
LX8385-33/ 8385A-33/ 8385B-33 (3.3V FIXED)						
Output Voltage (Note 4) LX8385/85A-33	V_{OUT}	V_{IN} = 5V, I_{OUT} = 0mA, T_A = 25°C	3.267	3.3	3.333	V
		4.75V ≤ V_{IN} ≤ 10V, 0mA ≤ I_{OUT} ≤ 3A, P ≤ P_{MAX}	3.235	3.3	3.365	V
LX8385B-33		V_{IN} = 5V, I_{OUT} = 0mA, T_A = 25°C	3.274	3.3	3.326	V
		4.75V ≤ V_{IN} ≤ 10V, 0A ≤ I_{OUT} ≤ 3A, P ≤ P_{MAX}	3.267	3.3	3.333	V
Line Regulation (note 2)	$ΔV_{OUT}$ (V_{IN})	4.75V ≤ V_{IN} ≤ 7V		1	6	mV
		4.75V ≤ V_{IN} ≤ 10V		2	10	mV
Load Regulation (note 2)	$ΔV_{OUT}$ (I_{OUT})	V_{IN} = 5V, 0mA ≤ I_{OUT} ≤ $I_{OUT(MAX)}$		5	15	mV
Thermal Regulation	$ΔV_{OUT}$ (Pwr)	T_A = 25°C, 20ms pulse		0.01	0.02	% / W
Ripple Rejection (note 3)		C_{OUT} = 100µF (Tantalum), I_{OUT} = 3A	60	83		dB
Quiescent Current	I_Q	0mA ≤ I_{OUT} ≤ $I_{OUT(MAX)}$, 4.75V ≤ V ≤ 10V		4	10	mA
Dropout Voltage LX8385-33	ΔV	$ΔV_{OUT}$ = 1%, I_{OUT} ≤ $I_{OUT(MAX)}$		1.2	1.5	V
LX8385A/85B-33		$ΔV_{OUT}$ = 1%, I_{OUT} ≤ $I_{OUT(MAX)}$		1.1	1.3	V

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, the following specifications apply over the operating ambient temperature for the LX8385x-xxC with 0°C ≤ T_A ≤ 125°C and the LX8385-xxI with -25°C ≤ T_A ≤ 125°C except where otherwise noted. Test conditions: V_{IN} -V_{OUT} = 3V; I_{OUT} = 3A. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

Parameter	Symbol	Test Conditions	LX8385x-xx Min	Typ	Max	Units
LX8385-33 / 8385A-33 / 8385B- (3.3V FIXED)(CONTINUED)						
Maximum Output Current	$I_{OUT(MAX)}$	V_{IN} ≤ 7V	3	3.5		A
Temperature Stability (Note 3)	$\Delta V_{OUT}(T)$			0.25		%
Long Term Stability (Note 3)	ΔV_{OUT} (t)	T_A=125°C, 1000 hours		0.3	1	%
RMS Output Noise (% of V_{OUT}) (Note 3)	$V_{OUT\ (RMS)}$	T_A=25°C, 10Hz ≤ f ≤ 10kHz		0.003		%
LX8385-05 / 8385A-05 / 8385B-05 (5.0V FIXED)						
Output Voltage (Note 4) LX8385/85A-05	V_{OUT}	V_{IN}=7V, I_{OUT}=0mA, T_A=25°C	4.950	5.00	5.050	V
		7V ≤ V_{IN} ≤ 10V, 0mA ≤ I_{OUT} ≤ 3A, P ≤ P_{MAX}	4.900	5.00	5.100	V
LX8385B-05		V_{IN}=7V, I_{OUT}=0mA, T_A=25°C	4.960	5.00	5.040	V
		7V ≤ V_{IN} ≤ 10V, 0mA ≤ I_{OUT} ≤ 3A, P ≤ P_{MAX}	4.950	5.00	5.050	V
Line Regulation (Note 2)	$\Delta V_{OUT}(V_{IN})$	7V ≤ V_{IN} ≤ 10V		2	10	mV
Load Regulation (Note 2)	ΔV_{OUT} (I_{OUT})	V_{IN}=7V, 0mA ≤ I_{OUT} ≤ $I_{OUT(MAX)}$		5	25	mV
Thermal Regulation	ΔV_{OUT} (Pwr)	T_A=25°C, 20ms pulse		0.01	0.02	% / W
Ripple Rejection (Note 3)		C_{OUT}=100µF (Tantalum), I_{OUT}=3A	60	83		dB
Quiescent Current	I_Q	0mA ≤ I_{OUT} ≤ $I_{OUT(MAX)}$, 4.75V ≤ V_{IN} ≤ 10V		4	10	mA
Dropout Voltage LX8385-33	ΔV	ΔV_{OUT}=1%, I_{OUT} ≤ $I_{OUT(MAX)}$		1.2	1.5	V
LX8385A/85B-33		ΔV_{OUT}=1%, I_{OUT} ≤ $I_{OUT(MAX)}$		1.1	1.3	V
Maximum Output Current	$I_{OUT(MAX)}$	V_{IN} ≤ 10V	3	3.5		A
Temperature Stability (Note 3)	ΔV_{OUT} (T)			0.25		%
Long Term Stability (Note 3)	ΔV_{OUT} (t)	T_A=125°C, 1000 hours		0.3	1	%
RMS Output Noise (% of V_{OUT}) (Note 3)	$V_{OUT\ (RMS)}$	T_A=25°C, 10Hz ≤ f ≤ 10kHz		0.003		%

Note 2 Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.
Note 3 These parameters, although guaranteed are not tested in production.
Note 4 See Maximum Output Current Section

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APPLICATION NOTES

The LX8385/85A/85B Series ICs are easy to use Low-Dropout (LDO) voltage regulators. They have all of the standard self-protection features expected of a voltage regulator: short circuit protection, safe operating area protection and automatic thermal shutdown if the device temperature rises above approximately 165°C.

Use of an output capacitor is REQUIRED with the LX8385/85A/85B series. Please see the table below for recommended minimum capacitor values.

These regulators offer a more tightly controlled reference voltage tolerance and superior reference stability when measured against the older pin-compatible regulator types that they replace.

STABILITY

The output capacitor is part of the regulator's frequency compensation system. Many types of capacitors are available, with different capacitance value tolerances, capacitance temperature coefficients, and equivalent series impedances. For all operating conditions, connection of a 220µF aluminum electrolytic capacitor or a 47µF (<400mΩ ESR) solid tantalum capacitor between the output terminal and ground will guarantee stable operation.

If a bypass capacitor is connected between the output voltage adjust (ADJ) pin and ground, ripple rejection will be improved (please see the section entitled "RIPPLE REJECTION"). When ADJ pin bypassing is used, the required output capacitor value increases. Output capacitor values of 220µF (aluminum) or 47µF (tantalum) provide for all cases of bypassing the ADJ pin. If an ADJ pin bypass capacitor is not used, smaller output capacitor values are adequate. The table below shows recommended minimum capacitance values for operation.

Minimum Capacitor Values

INPUT	OUTPUT	ADJ
10µF	15µF Tantalum, 100µF Aluminum	None
10µF	47µF Tantalum, 220µF Aluminum	15µF

To ensure good transient response from the power supply system under rapidly changing current load conditions, designers generally use several output capacitors connected in parallel. Such an arrangement serves to minimize the effects of the parasitic resistance (ESR) and inductance (ESL) that are present in all capacitors. Cost-effective solutions that sufficiently limit ESR and ESL effects generally result in total capacitance values in the range of hundreds to thousands of microfarads, which is more than adequate to meet regulator output capacitor specifications. Output capacitance values may be increased without limit.

The circuit shown in Figure 1 can be used to observe the transient response characteristics of the regulator in a power system under changing loads. The effects of different capacitor types and values on transient response parameters, such as overshoot and under-shoot, can be compared quickly in order to develop an optimum solution.

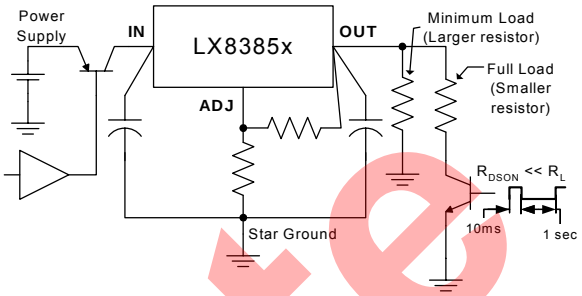


FIGURE 1 - DYNAMIC INPUT AND OUTPUT TEST

OVERLOAD RECOVERY

Like almost all IC power regulators, the LX8385/85A/85B regulators are equipped with Safe Operating Area (SOA) protection. The SOA circuit limits the regulator's maximum output current to progressively lower values as the input-to-output voltage difference increases. By limiting the maximum output current, the SOA circuit keeps the amount of power that is dissipated in the regulator itself within safe limits for all values of input-to-output voltage within the operating range of the regulator. The LX8385/85A/85B SOA protection system is designed to be able to supply some output current for all values of input-to-output voltage, up to the device breakdown voltage.

Under some conditions, a correctly operating SOA circuit may prevent a power supply system from returning to regulated operation after removal of an intermittent short circuit at the output of the regulator. This is a normal mode of operation, which can be seen, in most similar products, including older devices such as 7800 series regulators. It is most likely to occur when the power system input voltage is relatively high and the load impedance is relatively low.

When the power system is started "cold", both the input and output voltages are very close to zero. The output voltage closely follows the rising input voltage, and the input-to-output voltage difference is small. The SOA circuit therefore permits the regulator to supply large amounts of current as needed to develop the designed voltage level at the regulator output.

Now consider the case where the regulator is supplying regulated voltage to a resistive load under steady state conditions. A moderate input-to-output voltage appears across the regulator but the voltage difference is small enough that the SOA circuitry allows sufficient current to flow through the regulator to develop the designed output voltage across the load resistance. If the output resistor is short-circuited to ground, the input-to-output voltage difference across the regulator suddenly becomes larger by the amount of voltage that had appeared across the load resistor. The SOA circuit reads the increased input-to-output voltage, and cuts back the amount of current that it will permit the regulator to supply to its output terminal. When the short circuit across the output resistor is removed, all the regulator output current will again flow through the output resistor. The maximum current that the regulator can supply to the resistor will be limited by the SOA circuit, based on the large input-to-output

APPLICATION NOTES (CONTINUED)

OVERLOAD RECOVERY (continued)

voltage across the regulator at the time the short circuit is removed from the output. If this limited current is not sufficient to develop the designed voltage across the output resistor, the voltage will stabilize at some lower value, and will never reach the designed value. Under these circumstances, it may be necessary to cycle the input voltage down to zero in order to make the regulator output voltage return to regulation.

RIPPLE REJECTION

Ripple rejection can be improved by connecting a capacitor between the ADJ pin and ground. The value of the capacitor should be chosen so that the impedance of the capacitor is equal in magnitude to the resistance of *R1 at the ripple frequency*. The capacitor value can be determined by using this equation:

$$C = \frac{1}{(6.28 \times F_R \times R1)}$$

where: C ≡ the value of the capacitor in Farads; select an equal or larger standard value.
F_R ≡ the ripple frequency in Hz
$R1$ ≡ the value of resistor R1 in ohms

At a Ripple frequency of 120Hz, with R1= 100Ω:

$$C = \frac{1}{(6.28 \times 120\text{Hz} \times 100\Omega)} = 13.3\mu\text{F}$$

The closest equal or larger standard value should be used, in this case, 15µF. When an ADJ pin bypass capacitor is used, output ripple amplitude will be essentially independent of the output voltage. If an ADJ pin bypass capacitor is not used, output ripple will be proportional to the ratio of the output voltage to the reference voltage:

$$M = \frac{V_{OUT}}{V_{REF}}$$

where: M ≡ a multiplier for the ripple seen when the ADJ pin is optimally bypassed.
V_{REF} = 1.25V

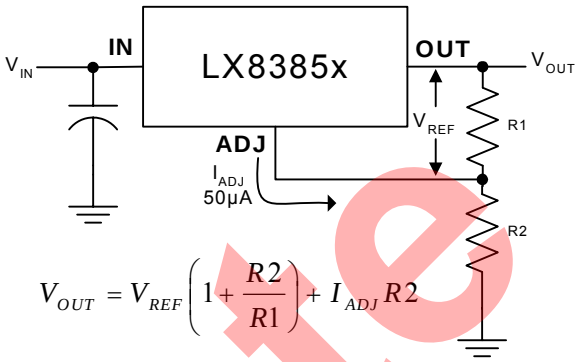
For example, if V_{OUT} = 2.5V the output ripple will be:

$$M = \frac{2.5V}{1.25V} = 2$$

Output ripple will be twice as bad as it would be if the ADJ pin were to be bypassed to ground with a properly selected capacitor.

OUTPUT VOLTAGE

The LX8385/85A/85B ICs develop a 1.25V reference voltage between the output and the adjust terminal (See Figure 2). By placing a resistor, R1, between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is the specified minimum load current of 10mA. Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored.



$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

FIGURE 2 - BASIC ADJUSTABLE REGULATOR

LOAD REGULATION

Because the LX8385/85A/85B regulators are three-terminal devices, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider, (*R*1), is connected *directly* to the case of the regulator, *not to the load*. This is illustrated in Figure 3. If *R*1 were connected to the load, the effective resistance between the regulator and the load would be:

$$R_{Peff} = R_P \times \left(\frac{R2 + R1}{R1}\right)$$

where: R_P ≡ Actual parasitic line resistance.

When the circuit is connected as shown in Figure 3, the parasitic resistance appears as its actual value, rather than the higher R_{Peff}.

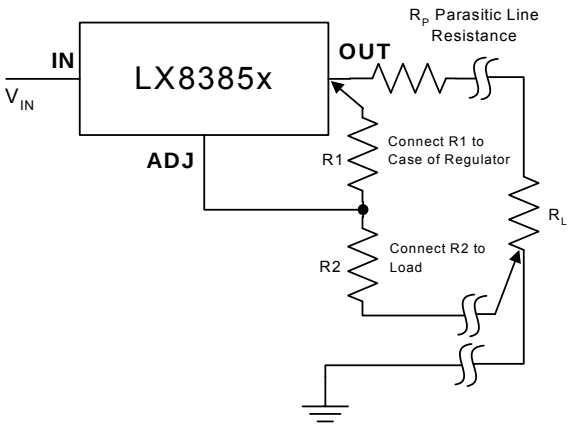


FIGURE 3 - CONNECTIONS FOR BEST LOAD REGULATION

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APPLICATION NOTES (CONTINUED)

LOAD REGULATION (continued)

Even when the circuit is configured optimally, parasitic resistance can be a significant source of error. A 20 mil. wide PC trace built from 1 oz. copper-clad circuit board material has a parasitic resistance of about 25 milliohms per inch of its length at room temperature. If a 3-terminal regulator used to supply 2.50 volts is connected by 2 inches of this trace to a load which draws 1.5 amps of current, a 75 millivolt drop will appear between the regulator and the load. Even when the regulator output voltage is precisely 2.50 volts, the load will only see 2.43 volts, which is a 3% error. It is important to keep the connection between the regulator output pin and the load as short as possible, and to use wide traces or heavy-gauge wire.

The minimum specified output capacitance for the regulator should be located near the regulator package. If several capacitors are used in parallel to construct the power system output capacitance, any capacitors beyond the minimum needed to meet the specified requirements of the regulator should be located near the sections of the load that require rapidly-changing amounts of current. Placing capacitors near the sources of load transients will help ensure that power system transient response is not impaired by the effects of trace impedance.

To maintain good load regulation, wide traces should be used on the input side of the regulator, especially between the input capacitors and the regulator. Input capacitor ESR must be small enough that the voltage at the input pin does not drop below $V_{IN(MIN)}$ during transients.

$$V_{IN(MIN)} = V_{OUT} + V_{DROPOUT(MAX)}$$

where: $V_{IN(MIN)}$ ≡ the lowest allowable instantaneous voltage at the input pin.

V_{OUT} ≡ the designed output voltage for the power supply system.

$V_{DROPOUT(MAX)}$ ≡ the specified dropout voltage for the installed regulator.

THERMAL CONSIDERATIONS

The LX8385/85A/85B regulators have internal power and thermal limiting circuitry designed to protect each device under overload conditions. For continuous normal load conditions, however, maximum junction temperature ratings must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. This includes junction to case, case to heat sink interface, and heat sink thermal resistance itself.

Junction-to-case thermal resistance is specified from the IC junction to the back surface of the case directly opposite the die. This is the lowest resistance path for heat flow. Proper mounting is required to ensure the best possible thermal flow from this area of the package to the heat sink. Thermal compound at the case to heat sink interface is strongly recommended. If the case of the device must be electrically isolated, a thermally conductive spacer can be used, as long as its added contribution to thermal resistance is considered. Note that the case of all devices in this series is electrically connected to the output.

Example

Given: V_{IN} = 5V
V_{OUT} = 2.5V
I_{OUT} = 1.5A
T_A = 50°C
$R_{\theta JT}$ = 2.7°C/W for TO-220

Find: Proper Heat Sink to keep IC's junction temperature below 125°C.**

Solution: The junction temperature is:

$$T_J = P_D(R_{\theta JT} + R_{\theta CS} + R_{\theta SA}) + T_A$$

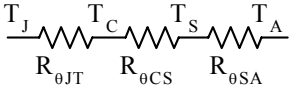
where: P_D ≡ Dissipated power.

$R_{\theta JT}$ ≡ Thermal resistance from the junction to the mounting tab of the package.

$R_{\theta CS}$ ≡ Thermal resistance through the interface between the IC and the surface on which it is mounted. (1.0°C/W at 6 in-lbs mounting screw torque).

$R_{\theta SA}$ ≡ Thermal resistance from the mounting surface to ambient (thermal resistance of the heat sink).

T_S ≡ Heat Sink Temperature.



First, find the maximum allowable thermal resistance of the heat sink:

$$R_{\theta SA} = \frac{T_J - T_A}{P_D} - (R_{\theta JT} + R_{\theta CS})$$

$$P_D = (V_{IN(MAX)} - V_{OUT})\, I_{OUT} = (5.0V - 2.5V) \times 1.5A$$

$$P_D = 3.75W$$

$$R_{\theta SA} = \frac{125°C - 50°C}{(5.0V - 2.5V) * 1.5A} - (2.7°C/W + 1.0°C/W)$$

$$R_{\theta SA} = 16.3°C/W$$

Next, select a suitable heat sink. The selected heat sink must have $R_{\theta SA}$ < 3.1°C/W. Thermalloy heatsink 6230B has $R_{\theta SA}$ = 12°C/W.

Finally, verify that junction temperature remains within specification using the selected heat sink:

$$T_J = 3.75W(2.7°C/W + 1.0°C/W + 12.0°C/W) + 50°C$$

$$T_J = 109°C$$

** Although the device can operate up to 150°C junction, it is recommended for long term reliability to keep the junction temperature below 125°C whenever possible.

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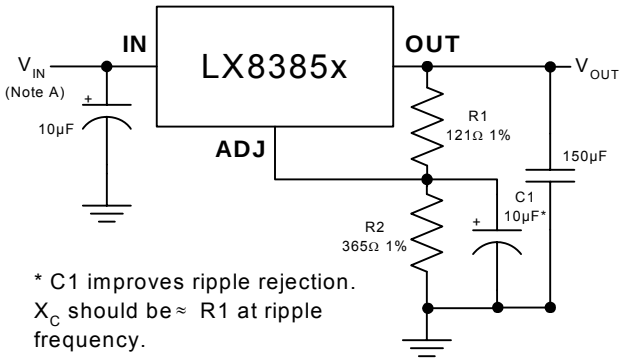
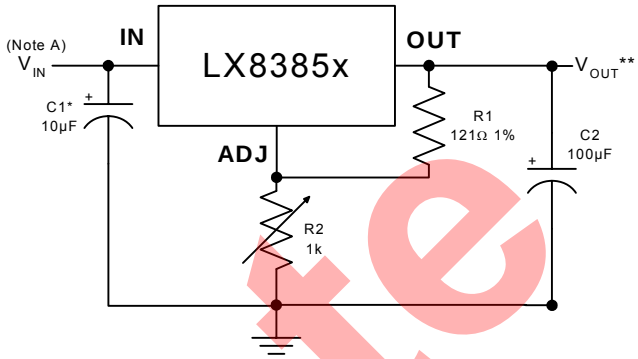
TYPICAL APPLICATIONS



* C1 improves ripple rejection. X_C should be ≈ R1 at ripple frequency.

FIGURE 4 - IMPROVING RIPPLE REJECTION



* Needed if device is far from filter capacitors.

$$** V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right)$$

FIGURE 5 - 1.2V - 8V ADJUSTABLE REGULATOR

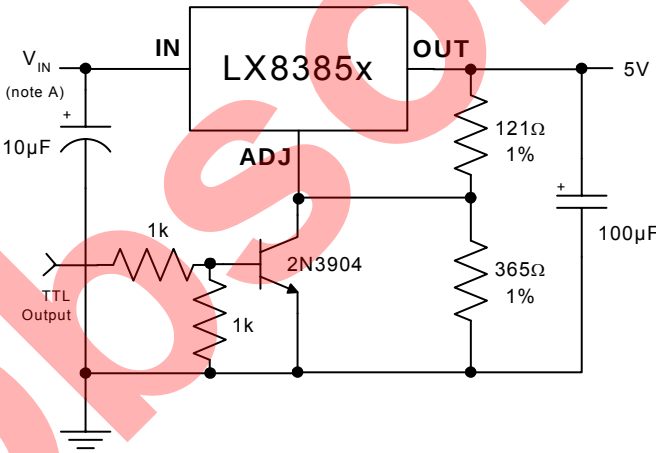


FIGURE 6 - 5V REGULATOR WITH SHUTDOWN

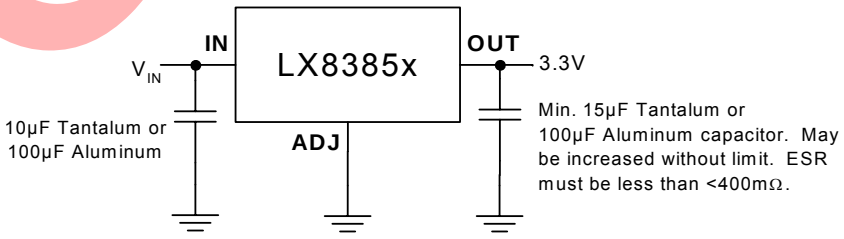


FIGURE 7 - FIXED 3.3V OUTPUT REGULATOR

Note A: $V_{IN(MIN)} = (\text{Intended } V_{OUT}) + V_{DROPOUT(MAX)}$

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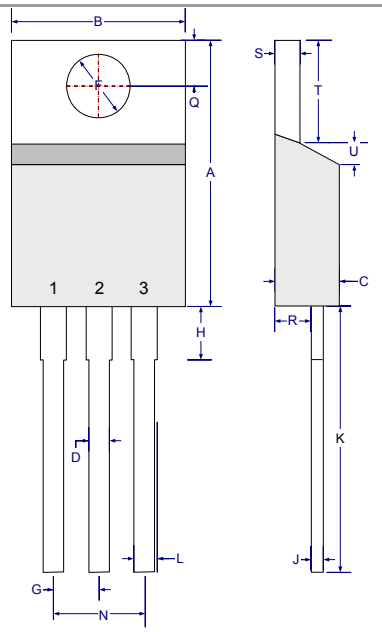
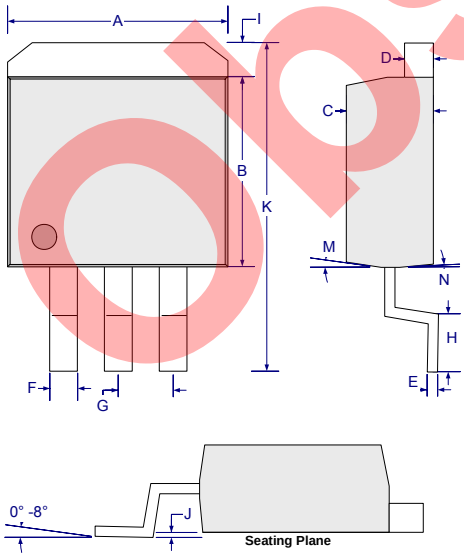
PACKAGE DIMENSIONS

P — 3-Pin Plastic TO-220



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.22	15.88	0.560	0.625
B	9.65	10.67	0.380	0.420
C	3.56	4.83	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.53	4.09	0.139	0.161
G	2.54 BSC		0.100 BSC	
H		6.35		0.250
J	0.30	1.14	0.012	0.045
K	12.70	14.73	0.500	0.580
L	1.14	1.27	0.045	0.050
N	5.08 TYP		0.200 TYP	
Q	2.54	3.05	0.100	0.120
R	2.03	2.92	0.080	0.115
S	1.14	1.40	0.045	0.055
T	5.84	6.86	0.230	0.270
U	0.508	1.14	0.020	0.045

DD — 3-Pin Plastic TO-263

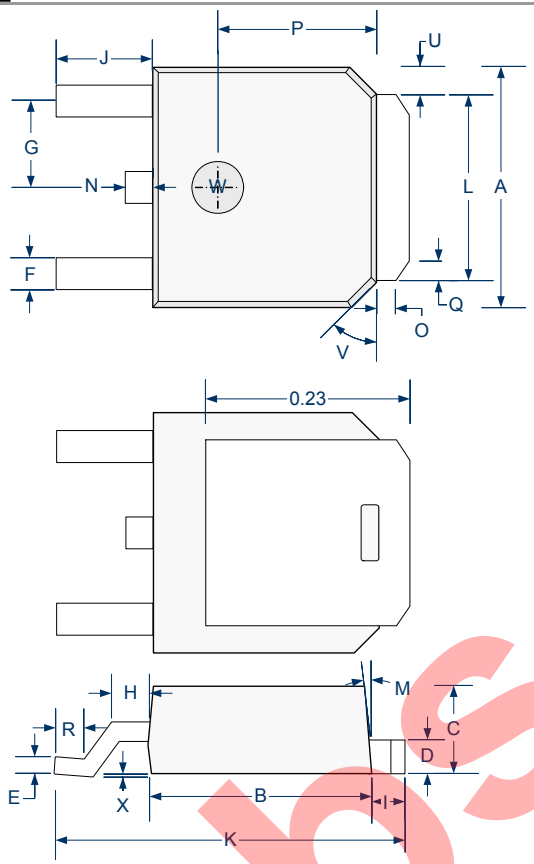


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.03	10.67	0.395	0.420
B	8.51	9.17	0.335	0.361
C	4.19	4.59	0.165	0.181
D	1.14	1.40	0.045	0.055
E	0.330	0.51	0.013	0.020
F	1.19	1.34	0.047	0.053
G	2.41	2.66	0.095	0.104
H	2.29	2.79	0.090	0.110
I	–	1.65	–	0.065
J	0	0.25	0	0.010
K	14.60	15.87	0.575	0.625
M	7°		7°	
N	3°		3°	

Note: Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

PACKAGE DIMENSIONS

DT 3-Pin Plastic TO-252



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.47	6.73	0.255	0.265
B	5.97	6.23	0.235	0.245
C	2.16	2.42	0.085	0.095
D	0.68	0.94	0.027	0.037
E	0.38	0.64	0.015	0.025
F	0.63	0.89	0.025	0.035
G	2.16	2.42	0.085	0.095
H	0.84	1.10	0.033	0.043
I	0.89	1.15	0.035	0.045
J	2.44	2.70	0.096	0.106
K	9.55	9.81	0.376	0.386
L	5.20	5.46	0.205	0.215
M	7.0°		7.0°	
N	0.51	0.77	0.020	0.030
O	0.51	0.77	0.020	0.030
P	4.19	4.45	0.165	0.175
Q	0.76	1.02	0.030	0.040
R	0.48	0.74	0.019	0.029
U	0.51	0.77	0.020	0.030
V	45°		45°	
W	1.44	1.70	0.057	0.067
X	0	0.10	0	0.004

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NOTES

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