

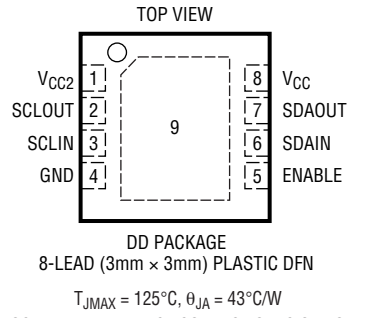
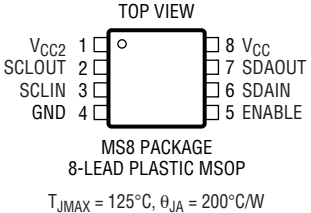
# LTC4300A-3

## ABSOLUTE MAXIMUM RATINGS (Note 1)

|                                    |               |
|------------------------------------|---------------|
| $V_{CC}$ to GND .....              | -0.3 to 7V    |
| $V_{CC2}$ to GND .....             | -0.3 to 7V    |
| SDAIN, SCLIN, SDAOUT, SCLOUT ..... | -0.3 to 7V    |
| ENABLE .....                       | -0.3 to 7V    |
| Operating Temperature Range        |               |
| LTC4300A-3C .....                  | 0°C to 70°C   |
| LTC4300A-3I .....                  | -40°C to 85°C |

|                                      |                |
|--------------------------------------|----------------|
| Storage Temperature Range            |                |
| MSOP .....                           | -65°C to 150°C |
| DFN .....                            | -65°C to 125°C |
| Lead Temperature (Soldering, 10 sec) |                |
| MSOP Only .....                      | 300°C          |

## PACKAGE/ORDER INFORMATION

|  | ORDER PART NUMBER              |  | ORDER PART NUMBER                |
|--|--------------------------------|--|----------------------------------|
|  | LTC4300A-3CDD<br>LTC4300A-3IDD |  | LTC4300A-3CMS8<br>LTC4300A-3IMS8 |
|  | DD<br>PART MARKING*            |  | MS8<br>PART MARKING              |
|  | LBHG<br>LBHG                   |  | LTBHD<br>LTBFH                   |

Consult LTC marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 2.7\text{V}$  to  $5.5\text{V}$ ,  $V_{CC2} = 2.7\text{V}$  to  $5.5\text{V}$ , unless otherwise noted.

| SYMBOL                    | PARAMETER                       | CONDITIONS  | MIN                | TYP                | MAX                | UNITS         |
|---------------------------|---------------------------------|---|--------------------|--------------------|--------------------|---------------|
| <b>Power Supply</b>       |                                 |   |                    |                    |                    |               |
| $V_{CC}$                  | Positive Supply Voltage         | ●   | 2.7                |                    | 5.5                | V             |
| $V_{CC2}$                 | Card Side Supply Voltage        | ●   | 2.7                |                    | 5.5                | V             |
| $I_{SD}$                  | Supply Current in Shutdown Mode | $V_{ENABLE} = 0\text{V}$  |                    | 20                 |                    | $\mu\text{A}$ |
| $I_{VCC1}$                | $V_{CC}$ Supply Current         | $V_{SDAIN} = V_{SCLIN} = 0\text{V}$ , $V_{CC1} = V_{CC2} = 5.5\text{V}$   |                    | 3                  | 4.1                | mA            |
| $I_{VCC2}$                | $V_{CC2}$ Supply Current        | $V_{SDAOUT} = V_{SCLOUT} = 0\text{V}$ , $V_{CC1} = V_{CC2} = 5.5\text{V}$ |                    | 2.1                | 2.9                | mA            |
| <b>Start-Up Circuitry</b> |                                 |   |                    |                    |                    |               |
| $V_{PRE}$                 | Precharge Voltage               | SDA, SCL Floating ●   | 0.8                | 1.0                | 1.2                | V             |
| $t_{IDLE}$                | Bus Idle Time                   | ●   | 50                 | 95                 | 150                | $\mu\text{s}$ |
| $V_{EN}$                  | ENABLE Threshold Voltage        |   |                    | $0.5 \cdot V_{CC}$ | $0.9 \cdot V_{CC}$ | V             |
| $V_{DIS}$                 | Disable Threshold Voltage       | ENABLE Pin  | $0.1 \cdot V_{CC}$ | $0.5 \cdot V_{CC}$ |                    | V             |
| $I_{EN}$                  | ENABLE Input Current            | ENABLE from 0V to $V_{CC}$  |                    | $\pm 0.1$          | $\pm 1$            | $\mu\text{A}$ |
| $t_{PHL}$                 | ENABLE Delay, On-Off            |   |                    | 10                 |                    | ns            |
| $t_{PLH}$                 | ENABLE Delay, Off-On            |   |                    | 95                 |                    | $\mu\text{s}$ |

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## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 2.7\text{V}$  to  $5.5\text{V}$ ,  $V_{CC2} = 2.7\text{V}$  to  $5.5\text{V}$ , unless otherwise noted.

| SYMBOL                  | PARAMETER                                      | CONDITIONS   |   | MIN                       | TYP | MAX | UNITS |
|-------------------------|--|--|---|---------------------------|-----|-----|-------|
| Rise-Time Accelerators  |  |  |   |                           |     |     |       |
| I <sub>PULLUPAC</sub>   | Transient Boosted Pull-Up Current              | Positive Transition on SDA, SCL, V <sub>CC</sub> = 2.7V, V <sub>CC2</sub> = 2.7V, Slew Rate = 1.25V/μs (Note 2)      |   | 1                         | 2   |     | mA    |
| Input-Output Connection |  |  |   |                           |     |     |       |
| V <sub>OS</sub>         | Input-Output Offset Voltage                    | 10k to V <sub>CC</sub> on SDA, SCL, V <sub>CC</sub> = 3.3V (Note 3), V <sub>CC2</sub> = 3.3V, V <sub>IN</sub> = 0.2V | ● | 0                         | 100 | 175 | mV    |
| f <sub>SCL, SDA</sub>   | Operating Frequency                            | Guaranteed by Design, Not Subject to Test  |   | 0                         |     | 400 | kHz   |
| C <sub>IN</sub>         | Digital Input Capacitance                      | Guaranteed by Design, Not Subject to Test  |   |                           |     | 10  | pF    |
| V <sub>OL</sub>         | Output Low Voltage, Input = 0V                 | SDA, SCL Pins, I <sub>SINK</sub> = 3mA, V <sub>CC</sub> = 2.7V, V <sub>CC2</sub> = 2.7V                              | ● | 0                         |     | 0.4 | V     |
| I <sub>LEAK</sub>       | Input Leakage Current                          | SDA, SCL Pins = V <sub>CC</sub> = 5.5V, V <sub>CC2</sub> = 5.5V  |   |                           |     | ±5  | μA    |
| Timing Characteristics  |  |  |   |                           |     |     |       |
| f <sub>I2C</sub>        | I <sup>2</sup> C Operating Frequency           | (Note 4)   |   | 0                         |     | 400 | kHz   |
| t <sub>BUF</sub>        | Bus Free Time Between Stop and Start Condition | (Note 4)   |   | 1.3                       |     |     | μs    |
| t <sub>hD, STA</sub>    | Hold Time After (Repeated) Start Condition     | (Note 4)   |   | 0.6                       |     |     | μs    |
| t <sub>su, STA</sub>    | Repeated Start Condition Setup Time            | (Note 4)   |   | 0.6                       |     |     | μs    |
| t <sub>su, STO</sub>    | Stop Condition Setup Time                      | (Note 4)   |   | 0.6                       |     |     | μs    |
| t <sub>hD, DAT</sub>    | Data Hold Time                                 | (Note 4)   |   | 300                       |     |     | ns    |
| t <sub>su, DAT</sub>    | Data Setup Time                                | (Note 4)   |   | 100                       |     |     | ns    |
| t <sub>LOW</sub>        | Clock Low Period                               | (Note 4)   |   | 1.3                       |     |     | μs    |
| t <sub>HIGH</sub>       | Clock High Period                              | (Note 4)   |   | 0.6                       |     |     | μs    |
| t <sub>f</sub>          | Clock, Data Fall Time                          | (Notes 4, 5)   |   | 20 + 0.1 • C <sub>B</sub> |     | 300 | ns    |
| t <sub>r</sub>          | Clock, Data Rise Time                          | (Notes 4, 5)   |   | 20 + 0.1 • C <sub>B</sub> |     | 300 | ns    |

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

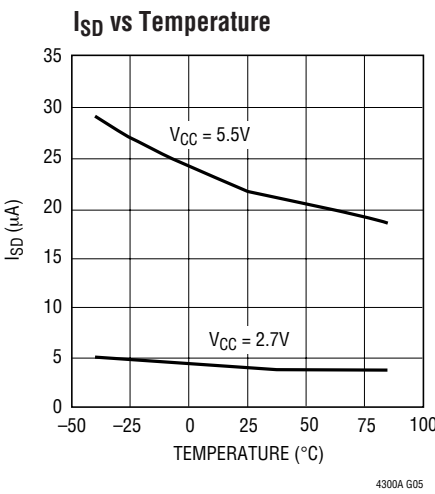
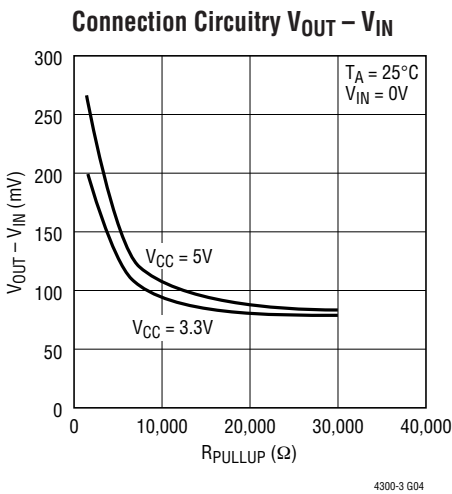
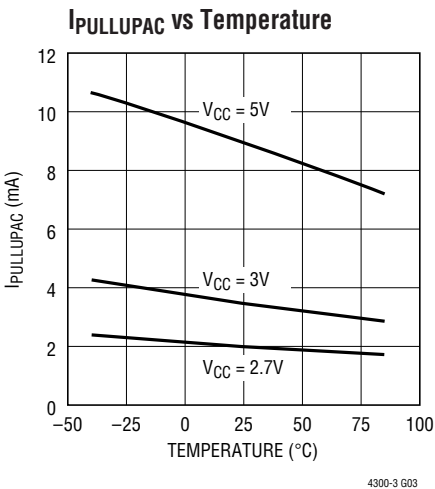
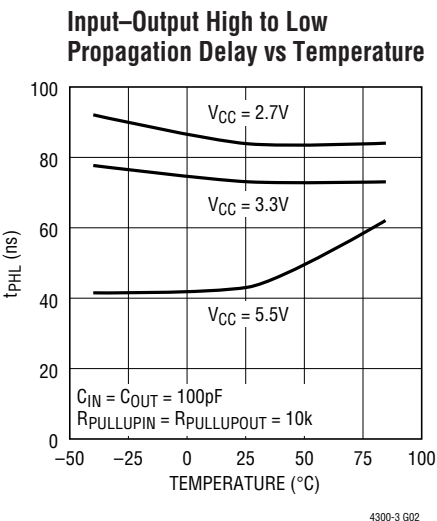
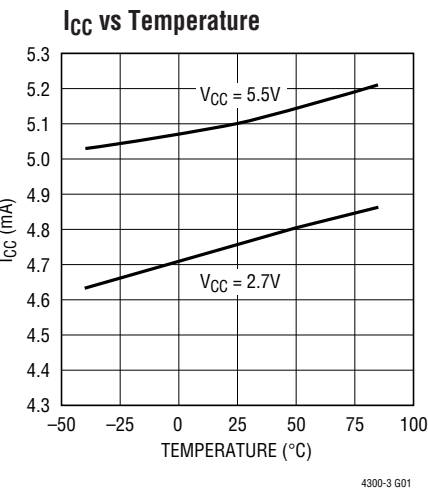
**Note 2:**  $I_{PULLUPAC}$  varies with temperature and  $V_{CC}$  voltage, as shown in the Typical Performance Characteristics section.

**Note 3:** The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pullup resistor and  $V_{CC}$  voltage is shown in the Typical Performance Characteristics section.

**Note 4:** Guaranteed by design, not subject to test.

**Note 5:**  $C_B$  = total capacitance of one bus line in pF.

TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS

**V<sub>CC2</sub> (Pin 1):** Card Supply Voltage. This is the supply voltage for the devices on the card I<sup>2</sup>C busses. Connect pull-up resistors from SDAOUT and SCLOUT to this pin. Place a bypass capacitor of at least 0.01 $\mu$ F close to this pin for best results.

**SCLOUT (Pin 2):** Serial Clock Output. Connect this pin to the SCL bus on the card.

**SCLIN (Pin 3):** Serial Clock Input. Connect this pin to the SCL bus on the backplane.

**GND (Pin 4):** Device Ground. Connect this pin to a ground plane for best results.

**ENABLE (Pin 5):** Digital CMOS Threshold Input. Grounding this pin puts the part in a low current mode. It also disables the rise-time accelerators, disables the bus discharge circuitry, isolates SDAIN from SDOUT and

isolates SCLIN from SCLOUT. For active operation, drive this pin to V<sub>CC</sub>. If this feature is unused, tie to V<sub>CC</sub>. Since ENABLE is V<sub>CC</sub> referenced, do not connect to V<sub>CC2</sub> or pull up to V<sub>CC2</sub>.

**SDAIN (Pin 6):** Serial Data Input. Connect this pin to the SDA bus on the backplane.

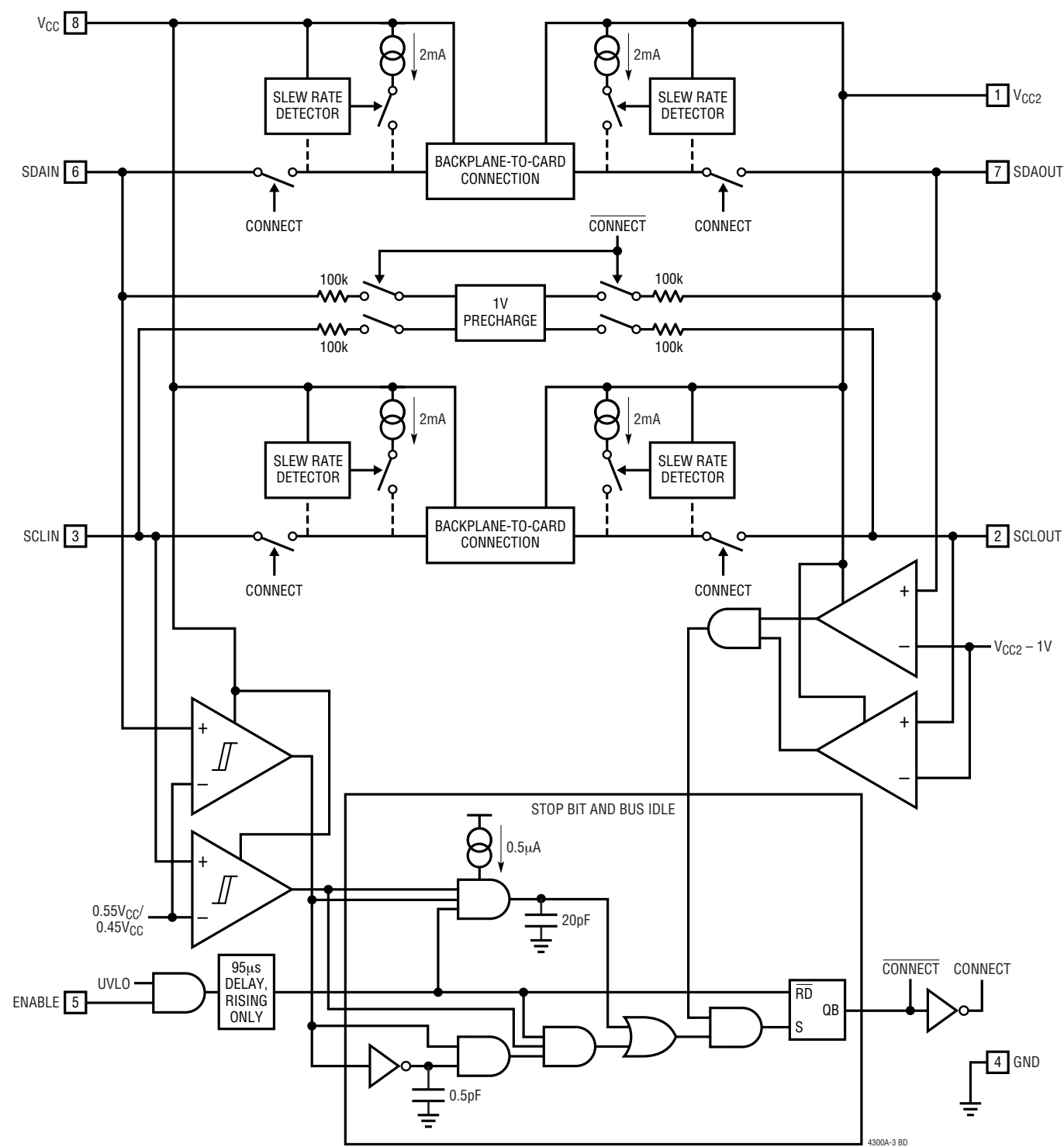
**SDAOUT (Pin 7):** Serial Data Output. Connect this pin to the SDA bus on the card.

**V<sub>CC</sub> (Pin 8):** Main Input Power Supply from Backplane. This is the supply voltage for the devices on the backplane I<sup>2</sup>C busses. Connect pull-up resistors from SDAIN and SCLIN to this pin. Place a bypass capacitor of at least 0.01 $\mu$ F close to this pin for best results.

**Exposed Pad (Pin 9, DFN Package Only):** Exposed Pad may be left open or connected to device ground.

BLOCK DIAGRAM

2-Wire Bus Buffer and Hot Swap™ Controller



Hot Swap is a trademark of Linear Technology Corporation.

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## OPERATION

### Start-Up

When the LTC4300A-3 first receives power on its  $V_{CC}$  pin, either during power-up or during live insertion, it starts in an undervoltage lockout (UVLO) state, ignoring any activity on the SDA and SCL pins until  $V_{CC}$  rises above 2.5V. The part also waits for  $V_{CC2}$  to rise above 2V. This ensures that the part does not try to function until it has enough voltage to do so.

During this time, the 1V precharge circuitry is also active and forces 1V through 100k nominal resistors to the SDA and SCL pins. Because the I/O card is being plugged into a live backplane, the voltage on the backplane SDA and SCL busses may be anywhere between 0V and  $V_{CC}$ . Precharging the SCL and SDA pins to 1V minimizes the worst-case voltage differential these pins will see at the moment of connection, therefore minimizing the amount of disturbance caused by the I/O card.

Once the LTC4300A-3 comes out of UVLO, it assumes that SDAIN and SCLIN have been inserted into a live system and that SDAOUT and SCLOUT are being powered up at the same time as itself. Therefore, it looks for either a stop bit or bus idle condition on the backplane side to indicate the completion of a data transaction. When either one occurs, the part also verifies that both the SDAOUT and SCLOUT voltages are high. When all of these conditions are met, the input-to-output connection circuitry is activated, joining the SDA and SCL busses on the I/O card with those on the backplane, and the rise time accelerators are enabled.

### Connection Circuitry

Once the connection circuitry is activated, the functionality of the SDAIN and SDAOUT pins is identical. A low forced on either pin at any time results in both pin voltages being low. For proper operation, logic low input voltages should be no higher than 0.4V with respect to the ground pin voltage of the LTC4300A-3. SDAIN and SDAOUT enter a logic high state only when all devices on both SDAIN and SDAOUT release high. The same is true for SCLIN and SCLOUT. This important feature ensures that clock stretching, clock synchronization, arbitration and the acknowledge protocol always work, regardless of how the devices in the system are tied to the LTC4300A-3.

Another key feature of the connection circuitry is that it provides bidirectional buffering, keeping the backplane and card capacitances isolated. Because of this isolation, the waveforms on the backplane busses look slightly different than the corresponding card bus waveforms, as described here.

### Input to Output Offset Voltage

When a logic low voltage,  $V_{LOW1}$ , is driven on any of the LTC4300A-3's data or clock pins, the LTC4300A-3 regulates the voltage on the other side of the part (call it  $V_{LOW2}$ ) to a slightly higher voltage, as directed by the following equation (typical):

$$V_{LOW2} = V_{LOW1} + 75\text{mV} + (V_{CC}/R) \cdot 70 [\Omega]$$

where R is the bus pull-up resistance in ohms. For example, if a device is forcing SDAOUT to 10mV where  $V_{CC} = 3.3\text{V}$  and the pull-up resistor R on SDAIN is 10k, then the voltage on SDAIN =  $10\text{mV} + 75\text{mV} + (3.3/10000) \cdot 70 = 108\text{mV}$  (typical). See the Typical Performance Characteristics section for curves showing the offset voltage as a function of  $V_{CC}$  and R.

### Propagation Delays

During a rising edge, the rise-time on each side is determined by the combined pull-up current of the LTC4300A-3 boost current and the bus resistor and the equivalent capacitance on the line. If the pull-up currents are the same, a difference in rise-time occurs which is directly proportional to the difference in capacitance between the two sides. This effect is displayed in Figure 1 for  $V_{CC} = V_{CC2} = 3.3\text{V}$  and a 10k pull-up resistor on each side (50pF on one side and 150pF on the other). Since the output side has less capacitance than the input, it rises faster and the effective propagation delay is negative.

There is a finite propagation delay through the connection circuitry for falling waveforms. Figure 2 shows the falling edge waveforms for the same  $V_{CC}$ , pull-up resistors and equivalent capacitance conditions as used in Figure 1. An external NMOS device pulls down the voltage on the side with 150pF capacitance; the LTC4300A-3 pulls down the voltage on the opposite side, with a delay of 55ns. This delay is always positive and is a function of supply voltage,

## OPERATION

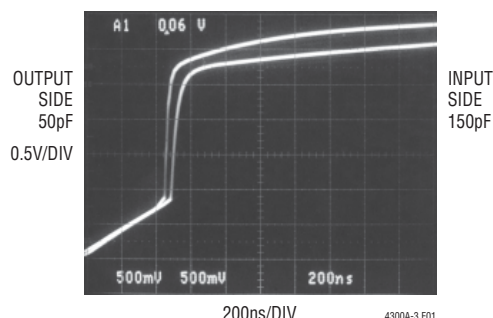


Figure 1. Input-Output Connection Low to High Transition

temperature and the pull-up resistors and equivalent bus capacitances on both sides of the bus. The Typical Performance Characteristics section shows  $t_{PHL}$  as a function of temperature and voltage for 10k pull-up resistors and 100pF equivalent capacitance on both sides of the part. By comparison with Figure 2, the  $V_{CC} = V_{CC2} = 3.3V$  curve shows that increasing the capacitance from 50pF to 100pF results in a propagation delay increase from 55ns to 75ns. Larger output capacitances translate to longer delays (up to 150ns). Users must quantify the difference in propagation times for a rising edge versus a falling edge in their systems and adjust setup and hold times accordingly.

### Rise-Time Accelerators

Once connection has been established, rise-time accelerator circuits on all four SDA and SCL pins are activated. These allow the user to choose weaker DC pull-up currents on the bus, reducing power consumption while still meeting system rise-time requirements. During positive bus transitions, the LTC4300A-3 switches in 2mA (typical) of current to quickly slew the SDA and SCL lines once their DC voltages exceed 0.6V. Using a general rule of 20pF of capacitance for every device on the bus (10pF for the device and 10pF for interconnect), choose a pull-up current so that the bus will rise on its own at a rate of at least 1.25V/ $\mu$ s to guarantee activation of the accelerators.

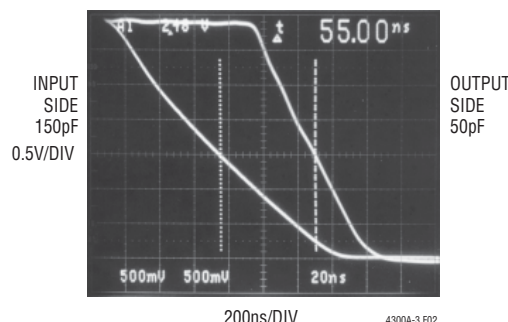


Figure 2. Input-Output Connection High to Low Transition

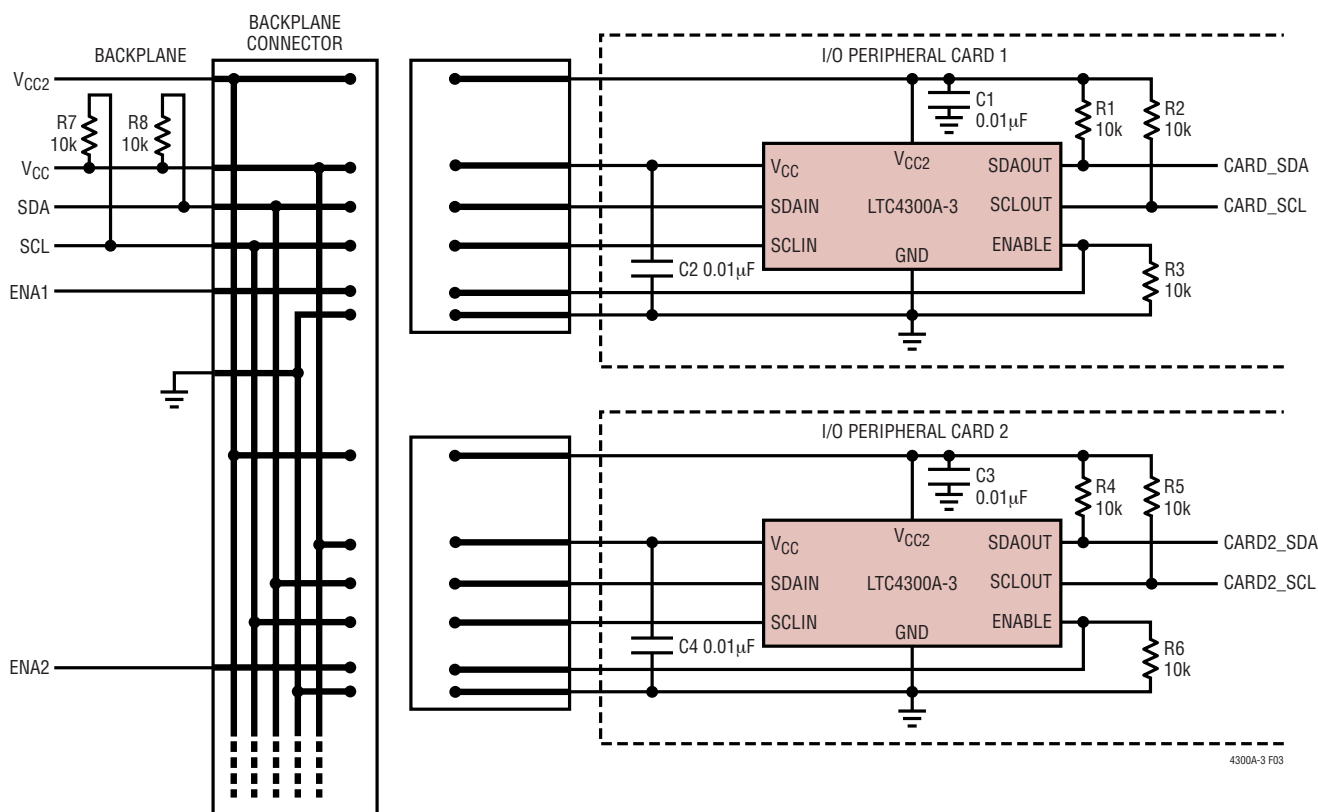
For example, assume an SMBus system with  $V_{CC} = 3V$ , a 10k pull-up resistor and equivalent bus capacitance of 200pF. The rise-time of an SMBus system is calculated from  $(V_{IL(MAX)} - 0.15V)$  to  $(V_{IH(MIN)} + 0.15V)$ , or 0.65V to 2.25V. It takes an RC circuit 0.92 time constants to traverse this voltage for a 3V supply; in this case,  $0.92 \cdot (10k \cdot 200pF) = 1.84\mu s$ . Thus, the system exceeds the maximum allowed rise-time of 1 $\mu$ s by 84%. However, using the rise-time accelerators, which are activated at a DC threshold of below 0.65V, the worst-case rise-time is:  $(2.25V - 0.65V) \cdot 200pF / 1mA = 320ns$ , which meets the 1 $\mu$ s rise-time requirement.

### ENABLE Low Current Disable

Grounding the ENABLE pin disconnects the backplane side from the card side, disables the rise-time accelerators, disables the bus precharge circuitry and puts the part in a near-zero current state. When the pin voltage is driven all the way to  $V_{CC}$ , the part waits for data transactions on both the backplane and card sides to be complete (as described in the Start-Up section) before reconnecting the two sides.

In addition, regardless of the bus capacitance, always choose  $R \leq 16k$  for  $V_{CC} = 5.5V$  maximum,  $R \leq 24k$  for  $V_{CC} = 3.6V$  maximum. The start-up circuitry requires logic high voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull-up values are needed to overcome the precharge voltage.

Figures 3 and 4 illustrate the usage of the LTC4300A-3 in applications that take advantage of both its Hot Swap controlling and capacitance buffering features. In all of these applications, note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise- and fall-time requirements difficult to meet. Placing a LTC4300A-3 on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the LTC4300A-3 drives the capacitance of everything on the card and the backplane must drive only the capacitance of the LTC4300A-3, which is less than 10pF.



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## APPLICATIONS INFORMATION

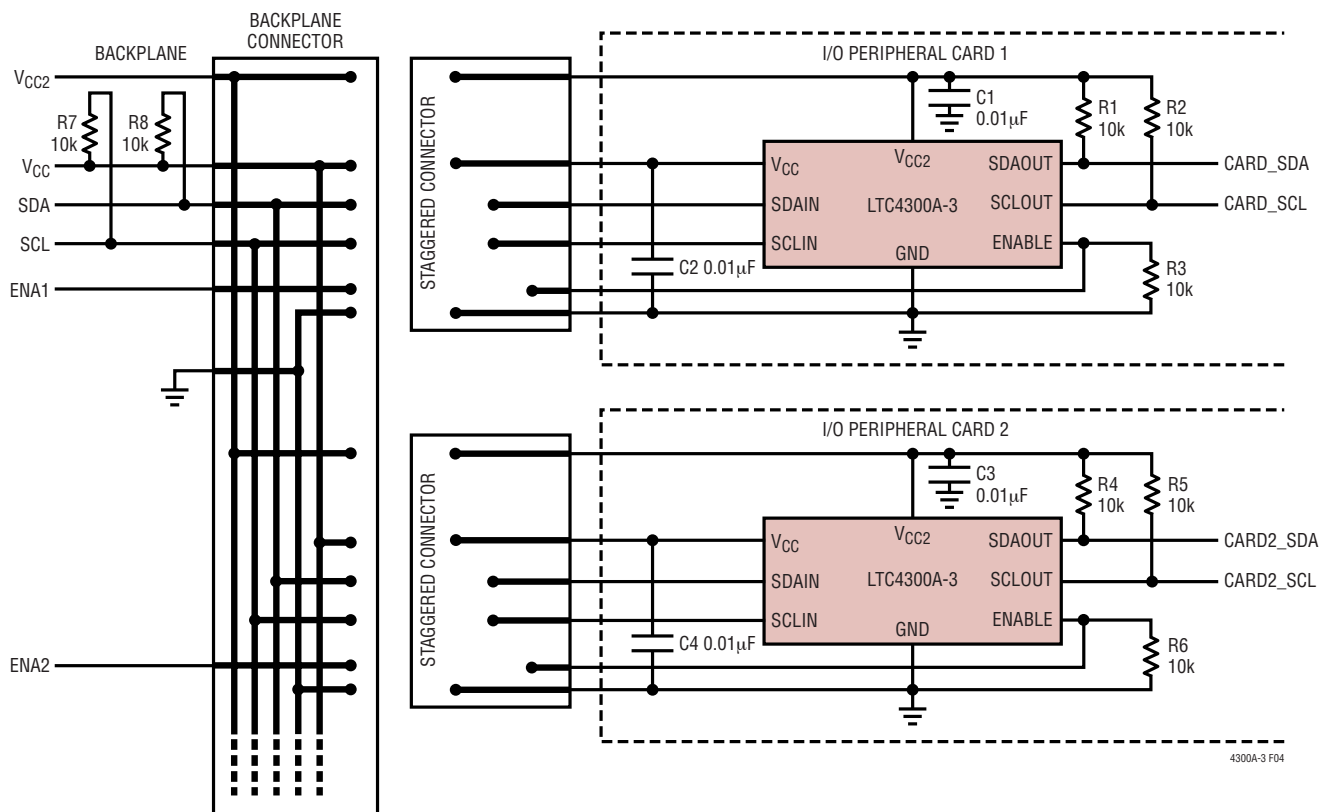


Figure 4. The LTC4300A-3 in a Custom Application. Making ENABLE the Shortest Pin Ensures that  $V_{CC}$  and  $V_{CC2}$  Connect Before ENABLE is Allowed to Go High, Connecting the Card to the Backplane

### 5V to 3.3V Level Translator and Power Supply Redundancy

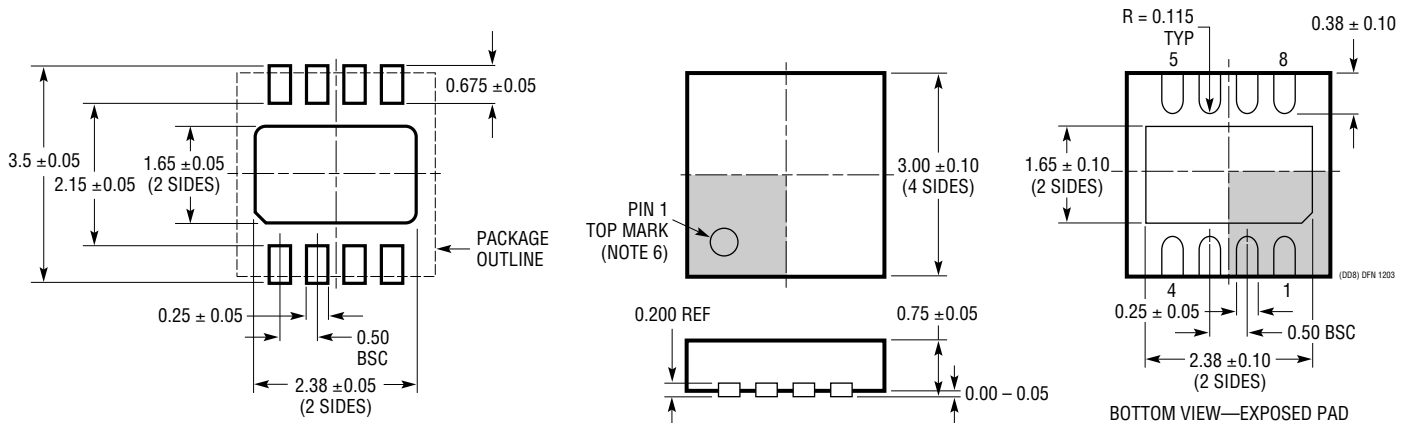
Systems requiring different supply voltages for the backplane side and the card side can use the LTC4300A-3, as shown in Figure 5. The pull-up resistors on the card side connect from SDAOUT to SCLOUT to  $V_{CC2}$ , and those on the backplane side connect from SDAIN and SCLIN to  $V_{CC}$ . The LTC4300A-3 functions for voltages ranging from 2.7V to 5.5V on both  $V_{CC}$  and  $V_{CC2}$ . There is no constraint on the

voltage magnitudes of  $V_{CC}$  and  $V_{CC2}$  with respect to each other.

This application also provides power supply redundancy. If the  $V_{CC2}$  voltage falls below its UVLO threshold, the LTC4300A-3 disconnects the backplane from the card, so that the backplane can continue to function. If the  $V_{CC}$  voltage falls below its UVLO threshold and the  $V_{CC2}$  voltage remains active, hold ENABLE at ground to ensure proper operation.

# PACKAGE DESCRIPTION

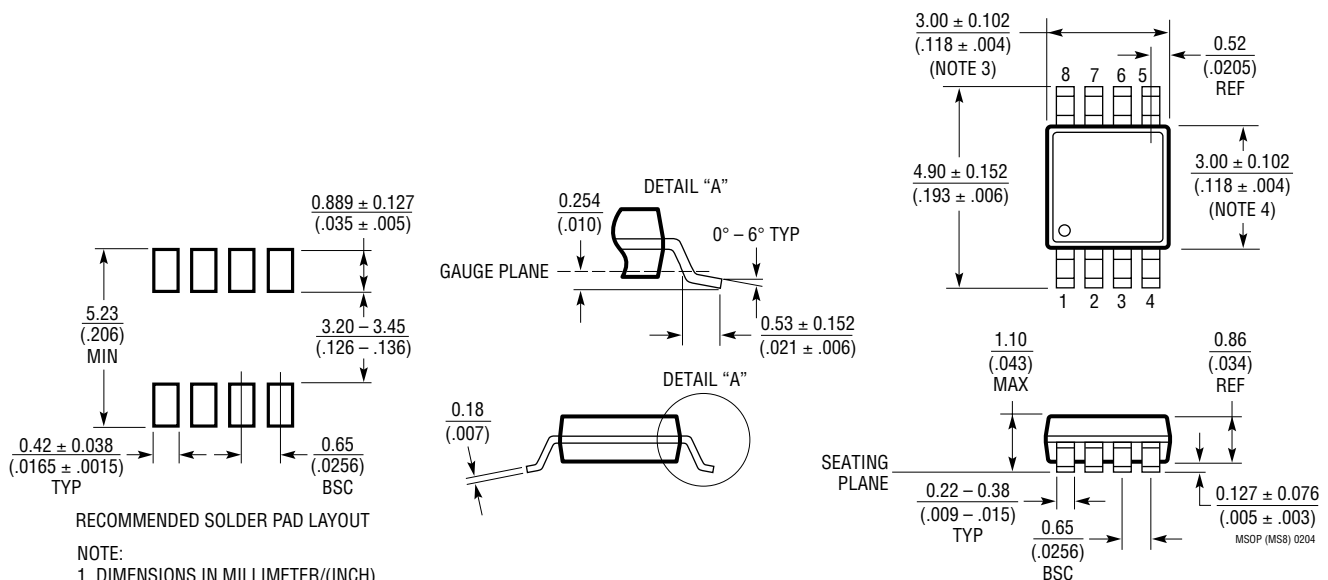
## DD Package 8-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1698)



### RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

- NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
  2. DRAWING NOT TO SCALE
  3. ALL DIMENSIONS ARE IN MILLIMETERS
  4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
  5. EXPOSED PAD SHALL BE SOLDER PLATED
  6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

## MS8 Package 8-Lead Plastic MSOP (Reference LTC DWG # 05-08-1660)



### RECOMMENDED SOLDER PAD LAYOUT

- NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
  2. DRAWING NOT TO SCALE
  3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
  4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
  5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

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TYPICAL APPLICATIONS

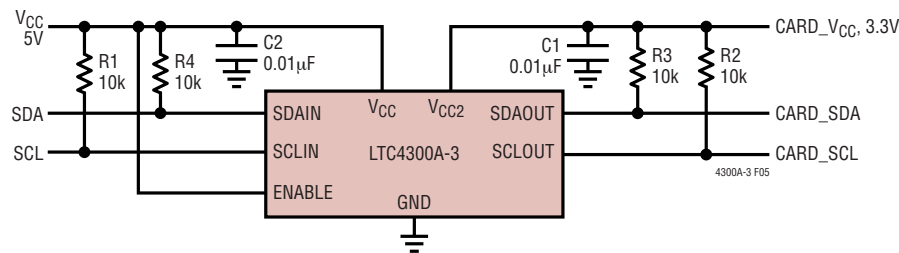


Figure 5. 5V to 3.3V Level Translator

RELATED PARTS

| PART NUMBER           | DESCRIPTION   | COMMENTS  |
|-----------------------|---|---|
| LTC1380/LTC1393       | Single-Ended 8-Channel/Differential 4-Channel Analog Mux with SMBus Interface | Low R <sub>ON</sub> : 35Ω Single-Ended/70Ω Differential, Expandable to 32 Single or 16 Differential Channels            |
| LTC1427-50            | Micropower, 10-Bit Current Output DAC with SMBus Interface                    | Precision 50µA ± 2.5% Tolerance Over Temperature, 4 Selectable SMBus Addresses, DAC Powers up at Zero or Midscale       |
| LTC1623               | Dual High Side Switch Controller with SMBus Interface                         | 8 Selectable Addresses/16-Channel Capability  |
| LTC1663               | SMBus Interface 10-Bit Rail-to-Rail Micropower DAC                            | DNL < 0.75LSB Max, 5-Lead SOT-23 Package  |
| LTC1694/LTC1694-1     | SMBus Accelerator   | Improved SMBus/I <sup>2</sup> C Rise-Time, Ensures Data Integrity with Multiple SMBus/I <sup>2</sup> C Devices          |
| LT1786F               | SMBus Controlled CCFL Switching Regulator                                     | 1.25A, 200kHz, Floating or Grounded Lamp Configurations   |
| LTC1695               | SMBus/I <sup>2</sup> C Fan Speed Controller in ThinSOT™                       | 0.75Ω PMOS 180mA Regulator, 6-Bit DAC   |
| LTC1840               | Dual I <sup>2</sup> C Fan Speed Controller                                    | Two 100µA 8-Bit DACs, Two Tach Inputs, Four GPIO  |
| LTC4300A-1/LTC4300A-2 | Hot Swappable 2-Wire Bus Buffer   | Preserves Data integrity Under Hot Swap Conditions, Provides Capacitive Buffering, Rise-Time Acceleration               |
| LTC4301               | Supply Independent 2-Wire Bus Buffer  | Provides Capacitive Buffer, 3.3V to 5V Level Translation with Only the Card Bus V <sub>CC</sub> Supply                  |
| LTC4301L              | Hot-Swappable 2-Wire Bus Buffer with Low Voltage Level Translation            | Level Translators, 1V Signals to Standard 3.3V and 5V Logic Rails   |
| LTC4302-1/LTC4302-2   | Addressable I <sup>2</sup> C and SMBus Compatible Bus Buffers                 | Provides Capacitive Buffering, Rise-Time Acceleration, and Input to Output Connection Control Using 2-Wire Bus Commands |

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