

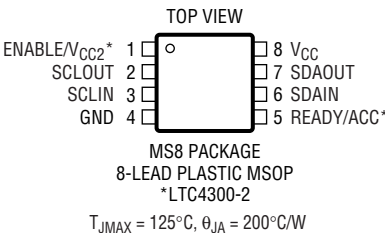
# LTC4300-1/LTC4300-2

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{CC}$ to GND .....	-0.5 to 7V
$V_{CC2}$ to GND (LTC4300-2) .....	-0.5 to 7V
SDAIN, SCLIN, SDAOUT, SCLOUT .....	-0.5 to 7V
READY, ENABLE (LTC4300-1) .....	-0.5 to 7V
ACC (LTC4300-2) .....	-0.5 to 7V
Operating Temperature Range	
LTC4300-1C/LTC4300-2C .....	0°C to 70°C
LTC4300-1I/LTC4300-2I .....	-40°C to 85°C
Storage Temperature Range .....	-65°C to 125°C
Lead Temperature (Soldering, 10 sec) .....	300°C

## PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
	LTC4300-1CMS8 LTC4300-1IMS8 LTC4300-2CMS8 LTC4300-2IMS8
	MS8 PART MARKING
	LTUB LTUC LTVJ LTVK

Consult LTC marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 2.7\text{V}$  to  $5.5\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Power Supply</b>						
$V_{CC}$	Positive Supply Voltage		● 2.7		5.5	V
$I_{CC}$	Supply Current	$V_{CC} = 5.5\text{V}$ , $V_{SDAIN} = V_{SCLIN} = 0\text{V}$ , LTC4300-1	●	2.8	6	mA
$I_{SD}$	Supply Current in Shutdown Mode	$V_{ENABLE} = 0\text{V}$ , LTC4300-1		0.1		$\mu\text{A}$
$V_{CC2}$	Card Side Supply Voltage	LTC4300-2	● 2.7		5.5	V
$I_{VCC1}$	$V_{CC}$ Supply Current	$V_{SDAIN} = V_{SCLIN} = 0\text{V}$ , $V_{CC1} = V_{CC2} = 5.5\text{V}$ , LTC4300-2		1.8	3.6	mA
$I_{VCC2}$	$V_{CC2}$ Supply Current	$V_{SDAOUT} = V_{SCLOUT} = 0\text{V}$ , $V_{CC1} = V_{CC2} = 5.5\text{V}$ , LTC4300-2		1.2	2.4	mA
<b>Start-Up Circuitry</b>						
$V_{PRE}$	Precharge Voltage	SDA, SCL Floating	● 0.8	1.0	1.2	V
$t_{IDLE}$	Bus Idle Time		● 50	95	150	$\mu\text{s}$
$V_{EN}$	ENABLE Threshold Voltage	LTC4300-1		$0.5 \cdot V_{CC}$	$0.9 \cdot V_{CC}$	V
$V_{DIS}$	Disable Threshold Voltage	LTC4300-1, ENABLE Pin		$0.1 \cdot V_{CC}$	$0.5 \cdot V_{CC}$	V
$I_{EN}$	ENABLE Input Current	ENABLE from 0V to $V_{CC}$ , LTC4300-1		$\pm 0.1$	$\pm 1$	$\mu\text{A}$
$t_{PHL}$	ENABLE Delay, On-Off	LTC4300-1		100		ns
	READY Delay, Off-On	LTC4300-1		10		ns
$t_{PLH}$	ENABLE Delay, Off-On	LTC4300-1		80		$\mu\text{s}$
	READY Delay, On-Off	LTC4300-1		10		$\mu\text{s}$
$I_{OFF}$	READY OFF State Leakage Current	LTC4300-1		$\pm 0.1$		$\mu\text{A}$
$V_{OL}$	READY Output Low Voltage	$I_{PULLUP} = 3\text{mA}$ , LTC4300-1	●		0.4	V

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## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 2.7\text{V}$  to  $5.5\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Rise-Time Accelerators							
IPULLUPAC	Transient Boosted Pull-Up Current	Positive Transition on SDA,SCL, V <sub>CC</sub> = 2.7V, Slew Rate = 1.25V/μs (Note 2), LTC4300-2, ACC = 0.7 • V <sub>CC2</sub> , V <sub>CC2</sub> = 2.7V		1	2		mA
VACCDIS	Accelerator Disable Threshold	LTC4300-2		0.3 • V <sub>CC2</sub>	0.5 • V <sub>CC2</sub>		V
VACCEN	Accelerator Enable Threshold	LTC4300-2			0.5 • V <sub>CC2</sub>	0.7 • V <sub>CC2</sub>	V
IVACC	ACC Input Current	LTC4300-2			±0.1	±1	μA
tPDOFF	ACC Delay, On/Off	LTC4300-2			5		ns
Input-Output Connection							
V <sub>OS</sub>	Input-Output Offset Voltage	10k to V <sub>CC</sub> on SDA, SCL, V <sub>CC</sub> = 3.3V (Note 3), LTC4300-2, V <sub>CC2</sub> = 3.3V, V <sub>IN</sub> = 0.2V	●	0	75	150	mV
f <sub>SCL, SDA</sub>	Operating Frequency	Guaranteed by Design, Not Subject to Test		0		400	kHz
C <sub>IN</sub>	Digital Input Capacitance	Guaranteed by Design, Not Subject to Test				10	pF
V <sub>OL</sub>	Output Low Voltage, Input = 0V	SDA, SCL Pins, I <sub>SINK</sub> = 3mA, V <sub>CC</sub> = 2.7V, V <sub>CC2</sub> = 2.7V, LTC4300-2	●	0		0.4	V
I <sub>LEAK</sub>	Input Leakage Current	SDA, SCL Pins = V <sub>CC</sub> = 5.5V, LTC4300-2, V <sub>CC2</sub> = 5.5V				±5	μA
Timing Characteristics							
f <sub>I2C</sub>	I <sup>2</sup> C Operating Frequency	(Note 4)		0		400	kHz
t <sub>BUF</sub>	Bus Free Time Between Stop and Start Condition	(Note 4)		1.3			μs
t <sub>hD,STA</sub>	Hold Time After (Repeated) Start Condition	(Note 4)		0.6			μs
t <sub>su,STA</sub>	Repeated Start Condition Setup Time	(Note 4)		0.6			μs
t <sub>su,STO</sub>	Stop Condition Setup Time	(Note 4)		0.6			μs
t <sub>hD,DAT</sub>	Data Hold Time	(Note 4)		300			ns
t <sub>su,DAT</sub>	Data Setup Time	(Note 4)		100			ns
t <sub>LOW</sub>	Clock Low Period	(Note 4)		1.3			μs
t <sub>HIGH</sub>	Clock High Period	(Note 4)		0.6			μs
t <sub>f</sub>	Clock, Data Fall Time	(Notes 4, 5)		20 + 0.1 • C <sub>B</sub>		300	ns
t <sub>r</sub>	Clock, Data Rise Time	(Notes 4, 5)		20 + 0.1 • C <sub>B</sub>		300	ns

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired

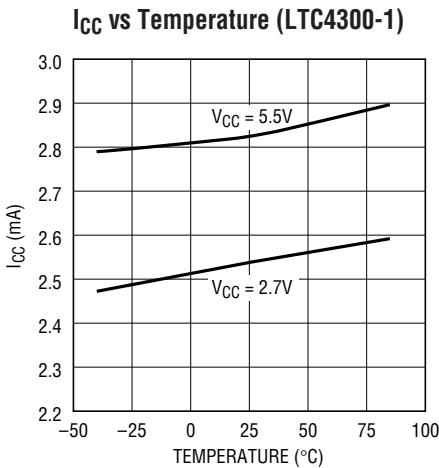
**Note 2:**  $I_{PULLUPAC}$  varies with temperature and  $V_{CC}$  voltage, as shown in the Typical Performance Characteristics section.

**Note 3:** The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pullup resistor and  $V_{CC}$  voltage is shown in the Typical Performance Characteristics section.

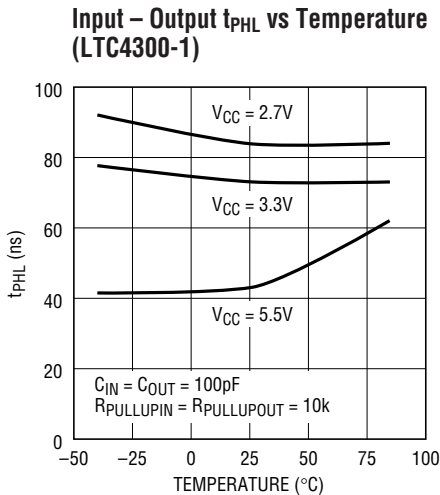
**Note 4:** Guaranteed by design, not subject to test.

**Note 5:**  $C_B$  = total capacitance of one bus line in pF.

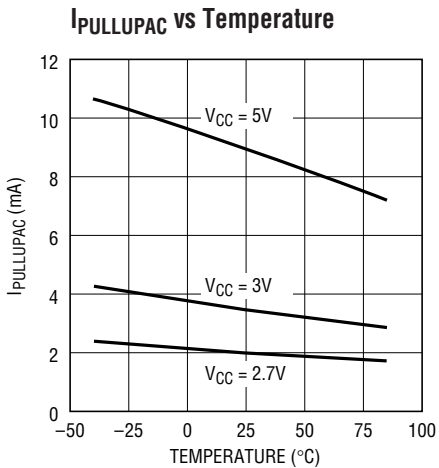
TYPICAL PERFORMANCE CHARACTERISTICS



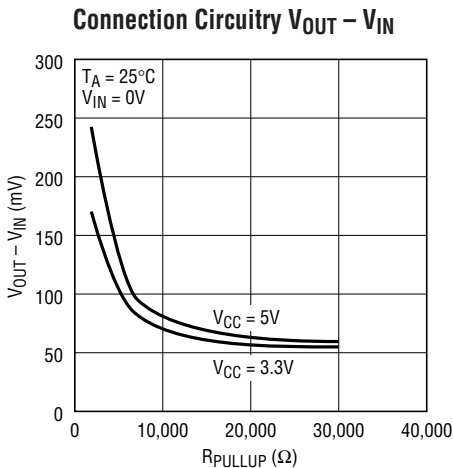
4300-1/2 G01



4300-1/2 G02



4300-1/2 G03



4300-1/2 G04

## PIN FUNCTIONS

**ENABLE/V<sub>CC2</sub> (Pin 1):** Chip Enable Pin/Card Supply Voltage. For the LTC4300-1, this is a digital CMOS threshold input pin. Grounding this pin puts the part in a low current ( $<1\mu\text{A}$ ) mode. It also disables the rise-time accelerators, disables the bus precharge circuitry, drives READY low, isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT. Drive ENABLE all the way to V<sub>CC</sub> for normal operation. Connect ENABLE to V<sub>CC</sub> if this feature is not being used. For the LTC4300-2, this is the supply voltage for the devices on the card I<sup>2</sup>C busses. Connect pull-up resistors from SDAOUT and SCLOUT to this pin. Place a bypass capacitor of at least  $0.01\mu\text{F}$  close to this pin for best results.

**SCLOUT (Pin 2):** Serial Clock Output. Connect this pin to the SCL bus on the card. See Figures 3 and 4 for bus pull-up resistance and capacitance requirements.

**SCLIN (Pin 3):** Serial Clock Input. Connect this pin to the SCL bus on the backplane. See Figures 3 and 4 for bus pull-up resistance and capacitance requirements.

**GND (Pin 4):** Ground. Connect this pin to a ground plane for best results.

**READY/ACC (Pin 5):** Connection Flag/Rise-Time Accelerator Control. For the LTC4300-1, this is an open-drain NMOS output which pulls low when either ENABLE is low or the start-up sequence described in the Operation section has not been completed. READY goes high when ENABLE is high and start-up is complete. Connect a 10k resistor from this pin to V<sub>CC</sub> to provide the pull up. For the LTC4300-2, this is a CMOS threshold digital input pin that enables and disables the rise-time accelerators on all four SDA and SCL pins. Drive ACC all the way to the V<sub>CC2</sub> supply voltage to enable all four accelerators; drive ACC to ground to turn them off.

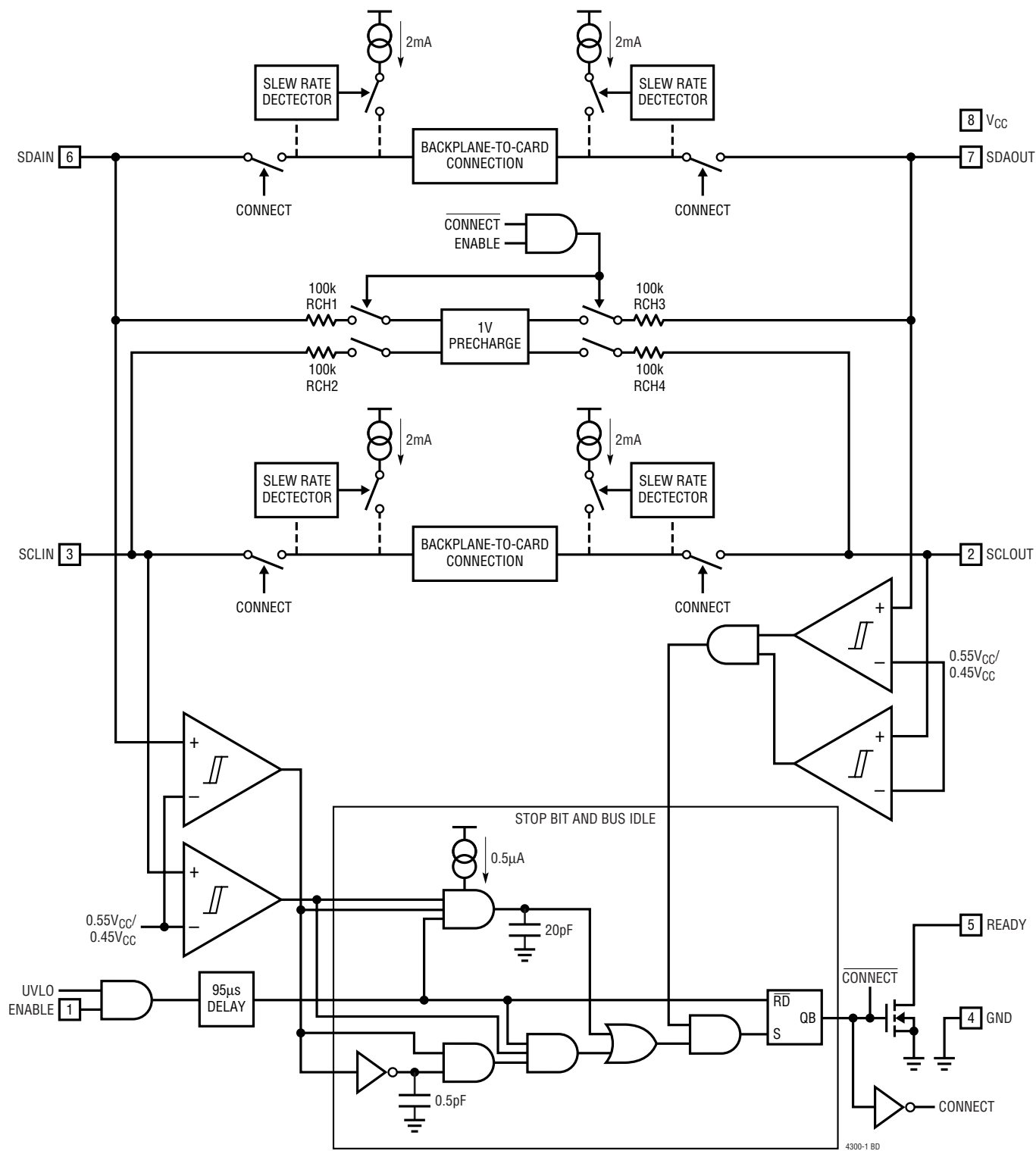
**SDAIN (Pin 6):** Serial Data Input. Connect this pin to the SDA bus on the backplane. See Figures 3 and 4 for bus pull-up resistance and capacitance requirements.

**SDAOUT (Pin 7):** Serial Data Output. Connect this pin to the SDA bus on the card. See Figures 3 and 4 for bus pull-up resistance and capacitance requirements.

**V<sub>CC</sub> (Pin 8):** Main Input Power Supply from Backplane. This is the supply voltage for the devices on the backplane I<sup>2</sup>C busses. Connect pull-up resistors from SDAIN and SCLIN to this pin. Place a bypass capacitor of at least  $0.01\mu\text{F}$  close to this pin for best results.

## BLOCK DIAGRAM (LTC4300-1)

### 2-Wire Bus Buffer and Hot Swap™ Controller



Hot Swap is a trademark of Linear Technology Corporation.

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## OPERATION

### Start-Up

When the LTC4300 first receives power on its  $V_{CC}$  pin, either during power-up or during hot swapping, it starts in an undervoltage lockout (UVLO) state, ignoring any activity on the SDA and SCL pins until  $V_{CC}$  rises above 2.5V. For the LTC4300-2, the part also waits for  $V_{CC2}$  to rise above 2V. This ensures that the part does not try to function until it has enough voltage to do so.

During this time, the 1V precharge circuitry is also active and forces 1V through 100k nominal resistors to the SDA and SCL pins. Because the I/O card is being plugged into a live backplane, the voltage on the backplane SDA and SCL busses may be anywhere between 0V and  $V_{CC}$ . Precharging the SCL and SDA pins to 1V minimizes the worst-case voltage differential these pins will see at the moment of connection, therefore minimizing the amount of disturbance caused by the I/O card.

Once the LTC4300 comes out of UVLO, it assumes that SDAIN and SCLIN have been hot swapped into a live system and that SDAOUT and SCLOUT are being powered up at the same time as itself. Therefore, it looks for either a stop bit or bus idle condition on the backplane side to indicate the completion of a data transaction. When either one occurs, the part also verifies that both the SDAOUT and SCLOUT voltages are high. When all of these conditions are met, the input-to-output connection circuitry is activated, joining the SDA and SCL busses on the I/O card with those on the backplane.

### Connection Circuitry

Once the connection circuitry is activated, the functionality of the SDAIN and SDAOUT pins is identical. A low forced on either pin at any time results in both pin voltages being low. SDAIN and SDAOUT enter a logic high state only when all devices on both SDAIN and SDAOUT force a high. The same is true for SCLIN and SCLOUT. This important feature ensures that clock stretching, clock arbitration and the acknowledge protocol always work, regardless of how the devices in the system are tied to the LTC4300.

Another key feature of the connection circuitry is that it provides bidirectional buffering, keeping the backplane and card capacitances isolated. Because of this isolation,

the waveforms on the backplane busses look slightly different than the corresponding card bus waveforms, as described here.

### Input to Output Offset Voltage

When a logic low voltage,  $V_{LOW1}$ , is driven on any of the LTC4300's data or clock pins, the LTC4300 regulates the voltage on the other side of the chip (call it  $V_{LOW2}$ ) to a slightly higher voltage, as directed by the following equation:

$$V_{LOW2} = V_{LOW1} + 50\text{mV} + (V_{CC}/R) \cdot 100$$

where  $R$  is the bus pull-up resistance in ohms. For example, if a device is forcing SDAOUT to 10mV and if  $V_{CC} = 3.3\text{V}$  and the pull-up resistor  $R$  on SDAIN is 10k, then the voltage on SDAIN =  $10\text{mV} + 50\text{mV} + (3.3/10000) \cdot 100 = 93\text{mV}$ . See the Typical Performance Characteristics section for curves showing the offset voltage as a function of  $V_{CC}$  and  $R$ .

### Propagation Delays

During a rising edge, the rise-time on each side is determined by the combined pull-up current of the LTC4300 boost current and the bus resistor and the equivalent capacitance on the line. If the pull-up currents are the same, a difference in rise-time occurs which is directly proportional to the difference in capacitance between the two sides. This effect is displayed in Figure 1 for  $V_{CC} = 3.3\text{V}$  and a 10k pull-up resistor on each side (50pF on one side and 150pF on the other). Since the output side has less capacitance than the input, it rises faster and the effective  $t_{PLH}$  is negative.

There is a finite propagation delay,  $t_{PHL}$ , through the connection circuitry for falling waveforms. Figure 2 shows the falling edge waveforms for the same  $V_{CC}$ , pull-up resistors and equivalent capacitance conditions as used in Figure 1. An external NMOS device pulls down the voltage on the side with 150pF capacitance; the LTC4300 pulls down the voltage on the opposite side, with a delay of 55ns. This delay is always positive and is a function of supply voltage, temperature and the pull-up resistors and equivalent bus capacitances on both sides of the bus. The Typical Performance Characteristics section shows  $t_{PHL}$



## OPERATION

as a function of temperature and voltage for 10k pull-up resistors and 100pF equivalent capacitance on both sides of the part. By comparison with Figure 2, the  $V_{CC} = 3.3V$  curve shows that increasing the capacitance from 50pF to 150pF results in a  $t_{PHL}$  increase from 55ns to 75ns. Larger output capacitances translate to longer delays (up to 150ns). Users must quantify the difference in propagation times for a rising edge vs a falling edge in their systems and adjust setup and hold times accordingly.

### Rise-Time Accelerators

Once connection has been established, rise-time accelerator circuits on all four SDA and SCL pins are activated. These allow the user to choose weaker DC pull-up currents on the bus, reducing power consumption while still meeting system rise-time requirements. During positive bus transitions, the LTC4300 switches in 2mA of current to quickly slew the SDA and SCL lines once their DC voltages exceed 0.6V. Using a general rule of 20pF of capacitance for every device on the bus (10pF for the device and 10pF for interconnect), choose a pull-up current so that the bus will rise on its own at a rate of at least 1.25V/ $\mu$ s to guarantee activation of the accelerators.

For example, assume an SMBus system with  $V_{CC} = 3V$ , a 10k pull-up resistor and equivalent bus capacitance of 200pF. The rise-time of an SMBus system is calculated from  $(V_{IL(MAX)} - 0.15V)$  to  $(V_{IH(MIN)} + 0.15V)$ , or 0.65V to 2.25V. It takes an RC circuit 0.92 time constants to traverse this voltage for a 3V supply; in this case,  $0.92 \cdot (10k \cdot 200pF) = 1.85\mu s$ . Thus, the system exceeds the maximum allowed rise-time of 1 $\mu$ s by 85%. However, using the rise-time accelerators, which are activated at a

DC threshold of below 0.65V, the worst-case rise-time is:  $(2.25V - 0.65V) \cdot 200pF/1mA = 320ns$ , which meets the 1 $\mu$ s rise-time requirement.

### READY Digital Output (LTC4300-1)

This pin provides a digital flag which is low when either ENABLE is low or the start-up sequence described earlier in this section has not been completed. READY goes high when ENABLE is high and start-up is complete. The pin is driven by an open drain pull-down capable of sinking 3mA while holding 0.4V on the pin. Connect a resistor of 10k to  $V_{CC}$  to provide the pull-up. This feature is available for the LTC4300-1 only.

### ENABLE Low Current Disable (LTC4300-1)

Grounding the ENABLE pin disconnects the backplane side from the card side, disables the rise-time accelerators, drives READY low, disables the bus precharge circuitry and puts the part in a near-zero current state. When the pin voltage is driven all the way to  $V_{CC}$ , the part waits for data transactions on both the backplane and card sides to be complete (as described in the Start-Up section) before reconnecting the two sides. This feature is available for the LTC4300-1 only.

### ACC Boost Current Enable (LTC4300-2)

Users having lightly loaded systems may wish to disable the rise-time accelerators. Driving this pin to ground turns off the rise-time accelerators on all four SDA and SCL pins. Driving this pin to the  $V_{CC2}$  voltage enables normal operation of the rise-time accelerators, as described in the Rise-Time Accelerators section above. This feature is available for the LTC4300-2 only.

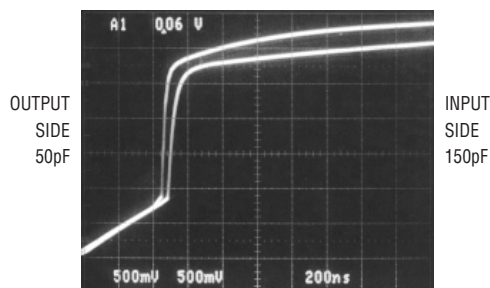


Figure 1. Input-Output Connection  $t_{PLH}$

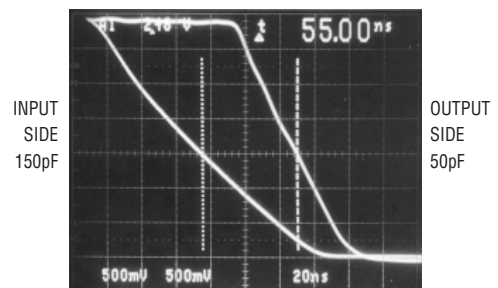


Figure 2. Input-Output Connection  $t_{PHL}$

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## APPLICATIONS INFORMATION

### Resistor Pull-Up Value Selection

The system pull-up resistors must be strong enough to provide a positive slew rate of  $1.25\text{V}/\mu\text{s}$  on the SDA and SCL pins, in order to activate the boost pull-up currents during rising edges. Choose maximum resistor value  $R$  using the formula:

$$R \leq (V_{CC(\text{MIN})} - 0.6) (800,000) / C$$

where  $R$  is the pull-up resistor value in ohms,  $V_{CC(\text{MIN})}$  is the minimum  $V_{CC}$  voltage and  $C$  is the equivalent bus capacitance in picofarads (pF).

In addition, regardless of the bus capacitance, always choose  $R \leq 16\text{k}$  for  $V_{CC} = 5.5\text{V}$  maximum,  $R \leq 24\text{k}$  for  $V_{CC} = 3.6\text{V}$  maximum. The start-up circuitry requires logic high voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull-up values are needed to overcome the precharge voltage. See the curves in Figures 3 and 4 for guidance in resistor pull-up selection.

### Minimum SDA and SCL Capacitance Requirements

The LTC4300 I/O connection circuitry requires a minimum capacitance loading on the SDA and SCL pins in order to function properly. The value of this capacitance is a function of  $V_{CC}$  and the bus pull-up resistance. Estimate the bus capacitance on both the backplane and the card data and clock busses, and refer to Figures 3 and 4 to choose appropriate pull-up resistor values. Note from the

figures that 5V systems must have at least 47pF capacitance on their busses and 3.3V systems must have at least 22pF capacitance for proper operation of the LTC4300. For applications with less capacitance, add a capacitor to ground to ensure these minimum capacitance conditions.

### Hot Swapping and Capacitance Buffering Application

Figures 5 through 8 illustrate the usage of the LTC4300 in applications that take advantage of both its hot swapping and capacitance buffering features. In all of these applications, note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise- and fall-time requirements difficult to meet. Placing a LTC4300 on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the LTC4300 drives the capacitance of everything on the card and the backplane must drive only the capacitance of the LTC4300, which is less than 10pF.

Figure 5 shows the LTC4300-1 in a CompactPCI™ configuration. Connect  $V_{CC}$  to the output of one of the CompactPCI power supply hot swap circuits and connect ENABLE to the short “board enable” pin.  $V_{CC}$  is monitored by a filtered UVLO circuit. With the  $V_{CC}$  voltage powering up after all other pins have established connection, the UVLO circuit ensures that the backplane and card data and clock busses are not connected until the transients asso-

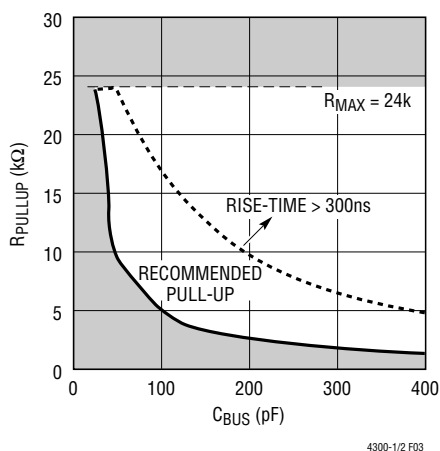


Figure 3. Bus Requirements for 3.3V Systems

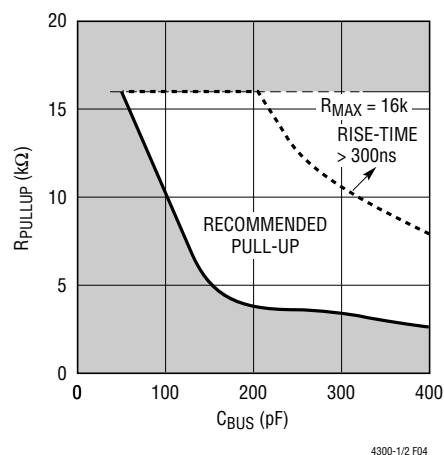


Figure 4. Bus Requirements for 5V Systems

CompactPCI is a trademark of the PCI Industrial Computer Manufacturers Group.

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## APPLICATIONS INFORMATION

ciated with hot swapping have settled. Owing to their small capacitance, the SDAIN and SCLIN pins cause minimal disturbance on the backplane busses when they make contact with the connector.

Figure 6 shows the LTC4300-2 in a CompactPCI configuration. The LTC4300-2 receives its  $V_{CC}$  voltage from one of the long “early power” pins. Because this power is not switched, add a  $5\Omega$  to  $10\Omega$  resistor between the  $V_{CC}$  pins of the connector and the LTC4300-2, as shown in the figure. In addition, make sure that the  $V_{CC}$  bypassing on the backplane is large compared to the  $0.01\mu F$  bypass capacitor on the card. Establishing early power  $V_{CC}$  ensures that the 1V precharge voltage is present at the SDAIN and SCLIN pins before they make contact. Connect  $V_{CC2}$  to the output of one of the CompactPCI power supply hot swap circuits.  $V_{CC2}$  is monitored by a filtered UVLO circuit. With the  $V_{CC2}$  voltage powering up after all other pins have established connection, the UVLO circuit ensures that the backplane and card data and clock busses are not connected until the transients associated with hot swapping have settled.

Figure 7 shows the LTC4300-1 in a PCI application, where all of the pins have the same length. In this case, connect an RC series circuit on the I/O card between  $V_{CC}$  and ENABLE. An RC product of 10ms provides a filter to prevent the LTC4300-1 from becoming activated until the transients associated with hot swapping have settled.

Figure 8 shows the LTC4300-2 in an application where the user has a custom connector with pins of three different lengths available. Making  $V_{CC2}$  the shortest pin ensures that all other pins are firmly connected before  $V_{CC2}$  receives any voltage. A filtered UVLO circuit on  $V_{CC2}$  ensures that the  $V_{CC2}$  pin is firmly connected before the LTC4300-2 connects the backplane to the card.

### Repeater/Bus Extender Application

Users who wish to connect two 2-wire systems separated by a distance can do so by connecting two LTC4300-1s back-to-back, as shown in Figure 9. The I<sup>2</sup>C specification allows for 400pF maximum bus capacitance, severely limiting the length of the bus. The SMBus specification

places no restriction on bus capacitance, but the limited impedances of devices connected to the bus require systems to remain small if rise- and fall-time specifications are to be met. The strong pull-up and pull-down impedances of the LTC4300-1 are capable of meeting rise- and fall-time specifications for one nanofarad of capacitance, thus allowing much more interconnect distance. In this situation, the differential ground voltage between the two systems may limit the allowed distance, because a valid logic low voltage with respect to the ground at one end of the system may violate the allowed  $V_{OL}$  specification with respect to the ground at the other end. In addition, the connection circuitry offset voltages of the back-to-back LTC4300-1s add together, directly contributing to the same problem.

### Systems with Disparate Supply Voltages (LTC4300-1)

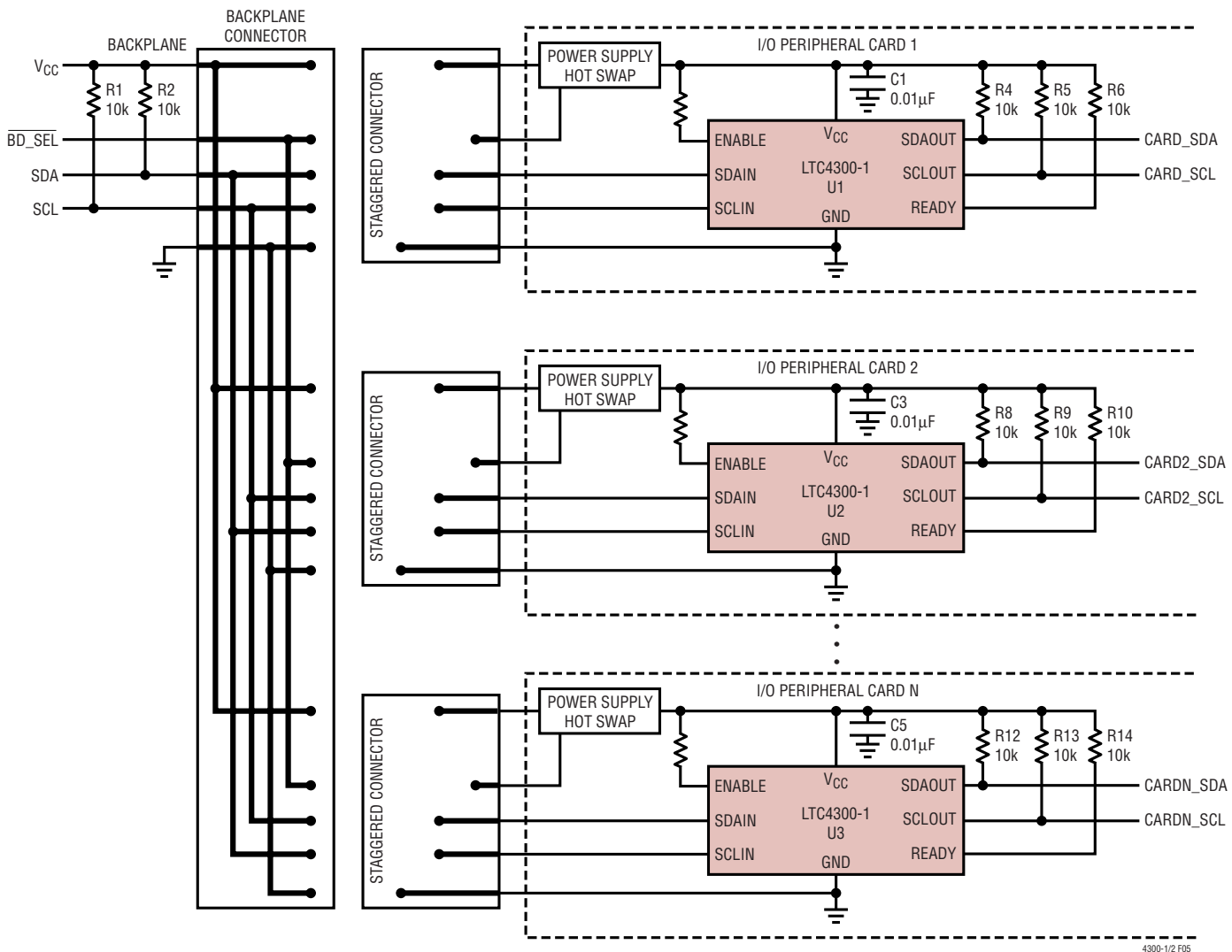
In large 2-wire systems, the  $V_{CC}$  voltages seen by devices at various points in the system can differ by a few hundred millivolts or more. This situation is well modelled by a series resistor in the  $V_{CC}$  line, as shown in Figure 10. For proper operation of the LTC4300-1, make sure that  $V_{CC(BUS)} \geq V_{CC(LTC4300)} - 0.5V$ .

### 5V to 3.3V Level Translator and Power Supply Redundancy (LTC4300-2)

Systems requiring different supply voltages for the backplane side and the card side can use the LTC4300-2, as shown in Figure 11. The pull-up resistors on the card side connect from SDAOUT to SCLOUT to  $V_{CC2}$ , and those on the backplane side connect from SDAIN and SCLIN to  $V_{CC}$ . The LTC4300-2 functions for voltages ranging from 2.7V to 5.5V on both  $V_{CC}$  and  $V_{CC2}$ . There is no constraint on the voltage magnitudes of  $V_{CC}$  and  $V_{CC2}$  with respect to each other.

This application also provides power supply redundancy. If either the  $V_{CC}$  or  $V_{CC2}$  voltage falls below its UVLO threshold, the LTC4300-2 disconnects the backplane from the card, so that the side that is still powered can continue to function.

APPLICATIONS INFORMATION

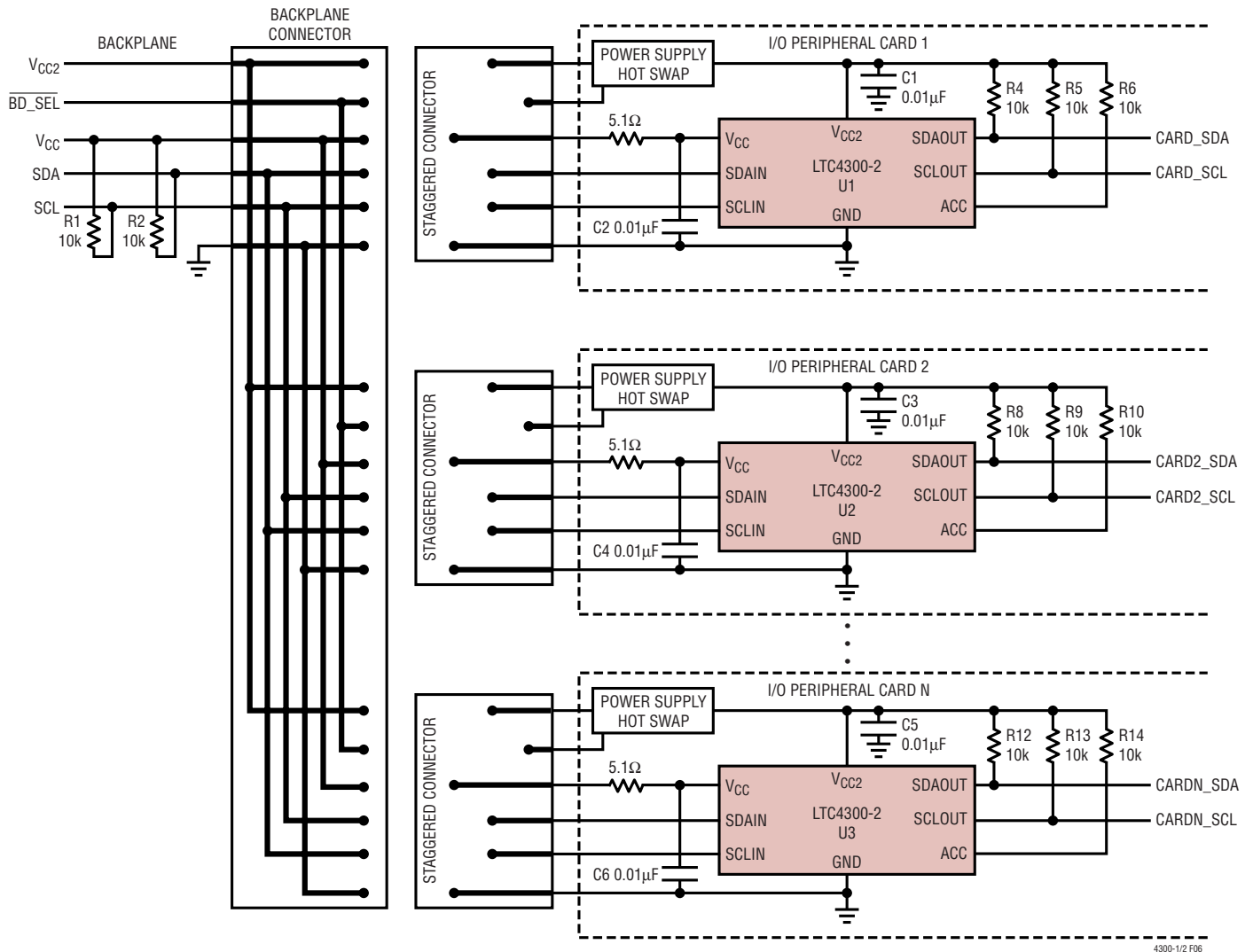


NOTE: APPLICATION ASSUMES BUS CAPACITANCES WITHIN "PROPER OPERATION" REGION OF FIGURES 3 AND 4

4300-1/2 F05

Figure 5. Hot Swapping Multiple I/O Cards into a Backplane Using the LTC4300-1 in a CompactPCI System

## APPLICATIONS INFORMATION



NOTE: APPLICATION ASSUMES BUS CAPACITANCES WITHIN "PROPER OPERATION" REGION OF FIGURES 3 AND 4

4300-1/2 F06

Figure 6. Hot Swapping Multiple I/O Cards into a Backplane Using the LTC4300-2 in a CompactPCI System



The schematic diagram illustrates the electrical connections for the I/O peripheral card. On the left, the **BACKPLANE CONNECTOR** is shown with pins for  $V_{CC2}$ ,  $V_{CC}$ , SDA, SCL, and ground. Pull-up resistors  $R1$  and  $R2$  (both 10k) are connected between  $V_{CC2}$  and the SDA/SCL lines. The **STAGGERED CONNECTOR** provides individual pins for each card. **I/O PERIPHERAL CARD 1** contains an **LTC4300-2** (U1) transceiver. Its  $V_{CC}$  pin is connected to the backplane  $V_{CC}$ , and its  $V_{CC2}$  pin is connected to the backplane  $V_{CC2}$ . The SDAIN pin is connected to the backplane SDA line, and the SCLIN pin is connected to the backplane SCL line. The SDAOUT pin is connected to the  $V_{CC2}$  line through a 0.01 $\mu$ F capacitor (C1), and the SCLOUT pin is connected to the  $V_{CC2}$  line through a 0.01 $\mu$ F capacitor (C2). The ACC pin is connected to ground. Pull-up resistors  $R4$ ,  $R5$ , and  $R6$  (all 10k) are connected between the  $V_{CC2}$  line and the CARD\_SDA, CARD\_SCL, and CARD2\_SCL lines, respectively. **I/O PERIPHERAL CARD 2** is identical to CARD 1, with an **LTC4300-2** (U2) transceiver. Its  $V_{CC}$  pin is connected to the backplane  $V_{CC}$ , and its  $V_{CC2}$  pin is connected to the backplane  $V_{CC2}$ . The SDAIN pin is connected to the backplane SDA line, and the SCLIN pin is connected to the backplane SCL line. The SDAOUT pin is connected to the  $V_{CC2}$  line through a 0.01 $\mu$ F capacitor (C3), and the SCLOUT pin is connected to the  $V_{CC2}$  line through a 0.01 $\mu$ F capacitor (C4). The ACC pin is connected to ground. Pull-up resistors  $R8$ ,  $R9$ , and  $R10$  (all 10k) are connected between the  $V_{CC2}$  line and the CARD2\_SDA, CARD2\_SCL, and CARD2\_SCL lines, respectively.

NOTE: APPLICATION ASSUMES BUS CAPACITANCES WITHIN “PROPER OPERATION” REGION OF FIGURES 3 AND 4

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## APPLICATIONS INFORMATION

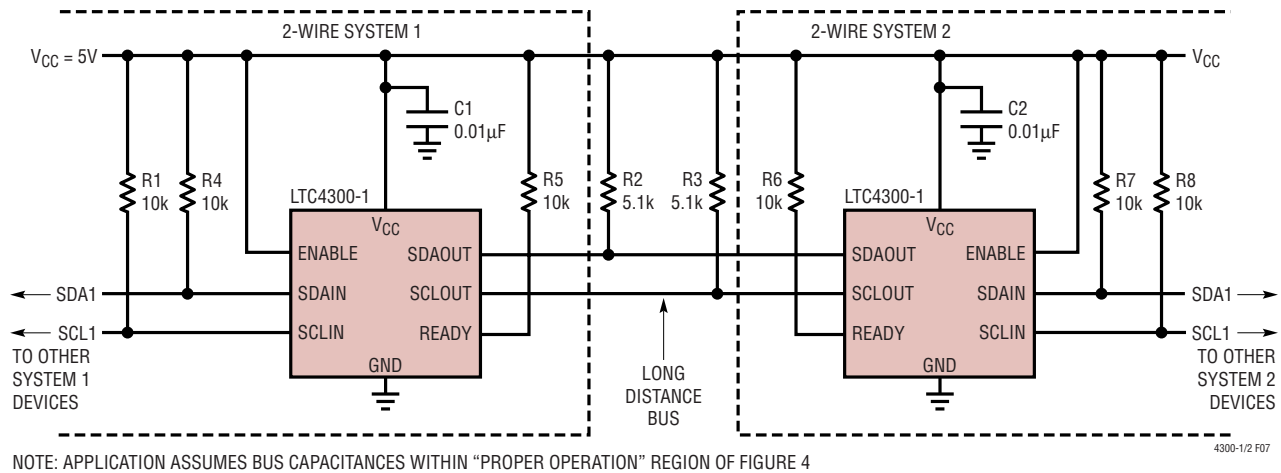
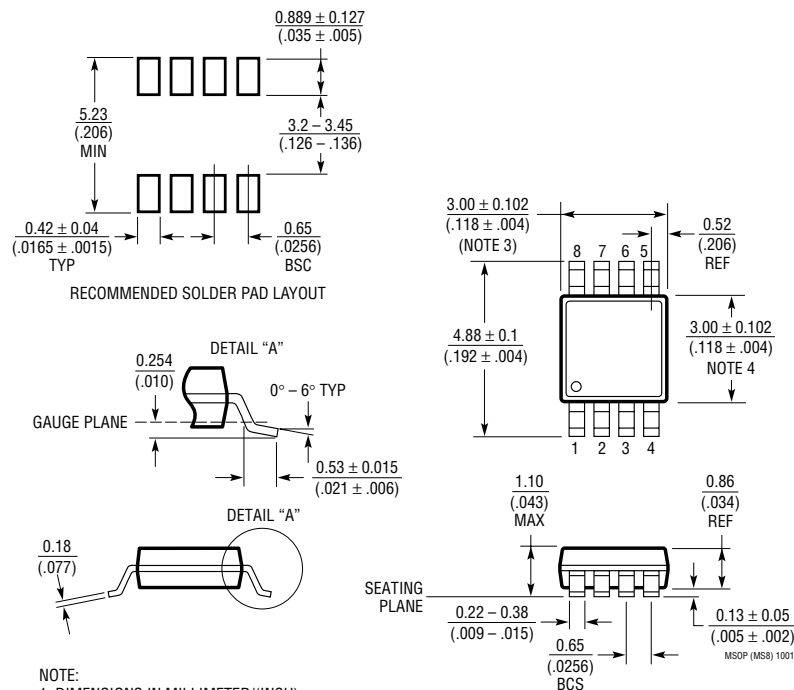


Figure 9. Repeater/Bus Extender Application

## PACKAGE DESCRIPTION

MS8 Package  
8-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1660)

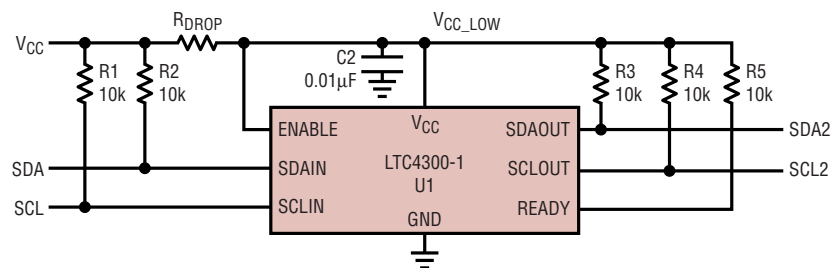


NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.  
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.  
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

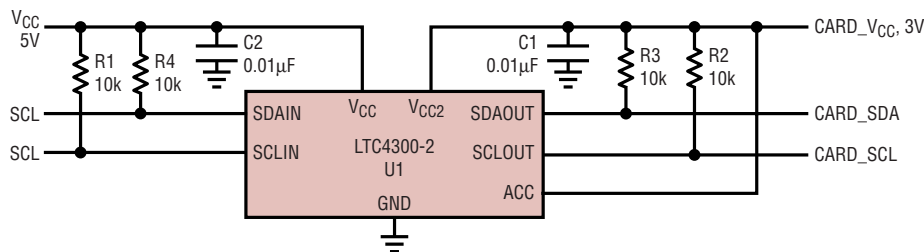
sn430012 430012fs

TYPICAL APPLICATIONS



NOTE: APPLICATION ASSUMES BUS CAPACITANCES WITHIN “PROPER OPERATION” REGION OF FIGURES 3 AND 4

Figure 10. System with Disparate V<sub>CC</sub> Voltages



NOTE: APPLICATION ASSUMES BUS CAPACITANCES WITHIN “PROPER OPERATION” REGION OF FIGURES 3 AND 4

Figure 11. 5V to 3.3V Level Translator

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1380/LTC1393	Single-Ended 8-Channel/Differential 4-Channel Analog Mux with SMBus Interface	Low R <sub>ON</sub> : 35Ω Single-Ended/70Ω Differential, Expandable to 32 Single or 16 Differential Channels
LTC1427-50	Micropower, 10-Bit Current Output DAC with SMBus Interface	Precision 50µA ± 2.5% Tolerance Over Temperature, 4 Selectable SMBus Addresses, DAC Powers up at Zero or Midscale
LTC1623	Dual High Side Switch Controller with SMBus Interface	8 Selectable Addresses/16-Channel Capability
LTC1663	SMBus Interface 10-Bit Rail-to-Rail Micropower DAC	DNL < 0.75LSB Max, 5-Lead SOT-23 Package
LTC1694/LTC1694-1	SMBus Accelerator	Improved SMBus/I <sup>2</sup> C Rise-Time, Ensures Data Integrity with Multiple SMBus/I <sup>2</sup> C Devices
LT1786F	SMBus Controlled CCFL Switching Regulator	1.25A, 200kHz, Floating or Grounded Lamp Configurations
LTC1695	SMBus/I <sup>2</sup> C Fan Speed Controller in ThinSOT™	0.75Ω PMOS 180mA Regulator, 6-Bit DAC
LTC1840	Dual I <sup>2</sup> C Fan Speed Controller	Two 100µA 8-Bit DACs, Two Tach Inputs, Four GPIO

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