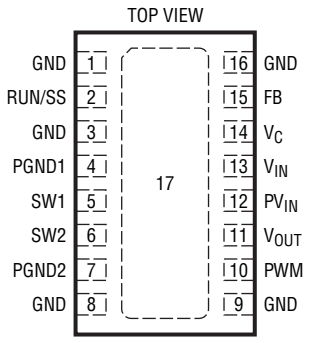
ABSOLUTE MAXIMUM RATINGS (Note 1)

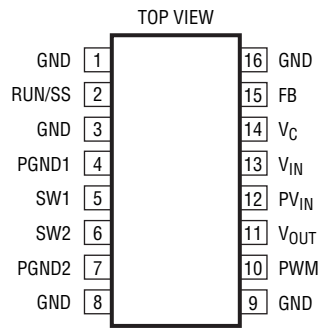
V_{IN}, PV_{IN} Voltages ..... –0.3V to 8V
V_{OUT} Voltage ..... –0.3V to 8V
SW1, SW2 Voltages
DC ..... –0.3V to 8V
Pulsed < 100ns ..... –0.3V to 9V
RUN/SS, PWM Voltages ..... –0.3V to 8V
V_C, FB Voltages ..... –0.3V to 6V
Operating Temperature Range (Note 2) ..... –40°C to 85°C
Maximum Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature
(Soldering, 10sec; GN Package) ..... 300°C

PIN CONFIGURATION



DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W (4-LAYER BOARD), θ_{JC} = 4°C/W
EXPOSED PAD (PIN 17) IS PGND, MUST BE SOLDERED TO PCB



GN PACKAGE
16-LEAD PLASTIC SSOP NARROW - FUSED

T_{JMAX} = 125°C, θ_{JA} = 90°C/W (4-LAYER BOARD), θ_{JC} = 37°C/W
PINS 1, 8, 9, AND 16 ARE PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3534EDHC#PBF	LTC3534EDHC#TRPBF	3534	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3534EGN#PBF	LTC3534EGN#TRPBF	3534	16-Lead SSOP Narrow - Fused	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3534EDHC	LTC3534EDHC#TR	3534	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3534EGN	LTC3534EDE#TR	3534	16-Lead SSOP Narrow - Fused	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{OUT} = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Start-Up Voltage		●		2.2	2.4	V
Input Operating Range		●	2.4		7	V
Output Voltage Adjust Range		●	1.8		7	V
Feedback Voltage	(Note 4)	●	0.975	1	1.015	V
Feedback Input Current	V_{FB} = Measured Feedback Voltage (Note 4)			1	50	nA
V_{IN} Quiescent Current – Burst Mode Operation	V_{FB} = 1.2V, V_{PWM} = 0V (Note 5)			25	50	µA
V_{IN} Quiescent Current – Shutdown	$V_{RUN/SS}$ = 0V, Not Including Switch Leakage, V_{OUT} = 0V			0.1	1	µA
V_{IN} Quiescent Current – Active	V_{FB} = 1.2V, V_{PWM} = 5V (Note 5)			420	700	µA
Input Current Limit	V_{PWM} = 5V	●	1	1.8		A
Reverse Current Limit	V_{PWM} = 5V			500		mA
Burst Current Limit	V_{PWM} = 0V			400		mA
NMOS Switches Leakage	Switches B and C			0.1	7	µA
PMOS Switches Leakage	Switches A and D			0.1	10	µA
PMOS Switches On-Resistance	Switches A and D			260		mΩ
NMOS B Switch On-Resistance	Switch B			275		mΩ
NMOS C Switch On-Resistance	Switch C			215		mΩ
Maximum Duty Cycle	Boost (% Switch C On) Buck (% Switch A On)	● ●	75 100	85		% %
Minimum Duty Cycle		●			0	%
Frequency		●	0.80	1	1.15	MHz
Error Amp AV_{OL}	(Note 4)			74		dB
Error Amp Source Current				–15		µA
Error Amp Sink Current				225		µA
RUN/SS Threshold		●	0.4	1	1.4	V
RUN/SS Input Current – Shutdown	$V_{RUN/SS}$ = 400mV; IC is Shut Down			0.02	1	µA
RUN/SS Input Current – Active	$V_{RUN/SS}$ = 5V; IC is Enabled			0.28	1	µA
PWM Threshold	Measured at PWM Pin; Voltage at which Burst Mode Operation is Disabled (PWMing Enabled)		0.4	1	1.4	V
PWM Input Current	V_{PWM} = 5V			1.25	2.5	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3534E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

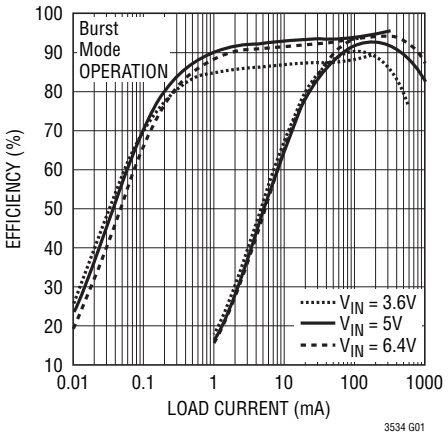
Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Note 4: The IC is tested in a feedback loop to make this measurement.

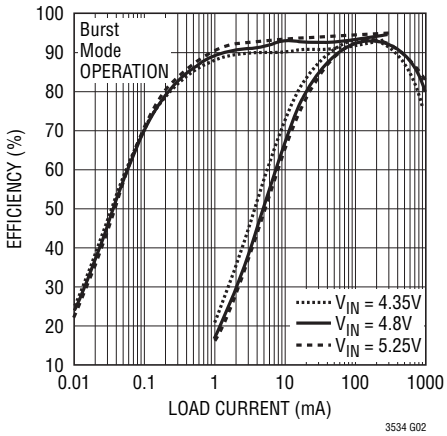
Note 5: Current Measurements are performed when the outputs are not switching.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

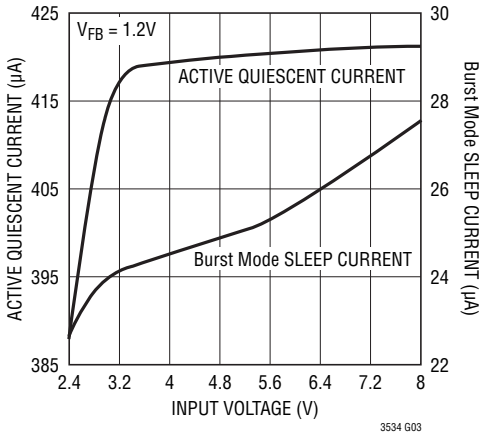
4 Alkaline Cells to 5V Efficiency vs I_{LOAD}



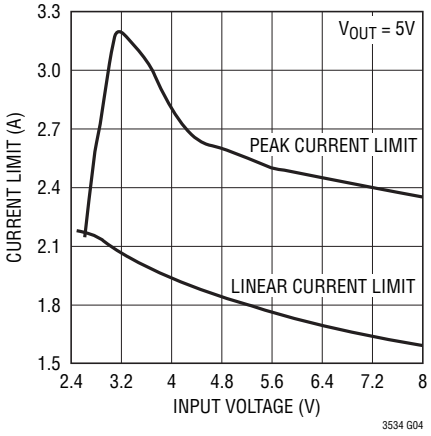
USB to 5V Efficiency vs I_{LOAD}



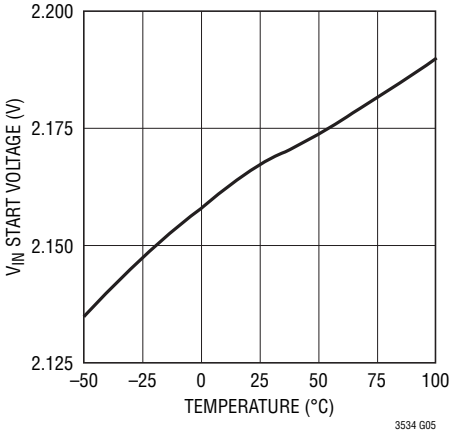
Active Quiescent and Burst Mode SLEEP Currents vs V_{IN}



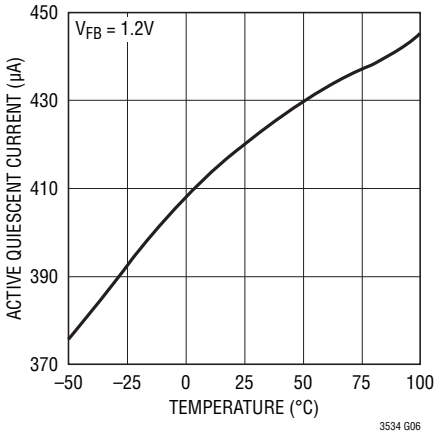
Current Limits vs V_{IN}



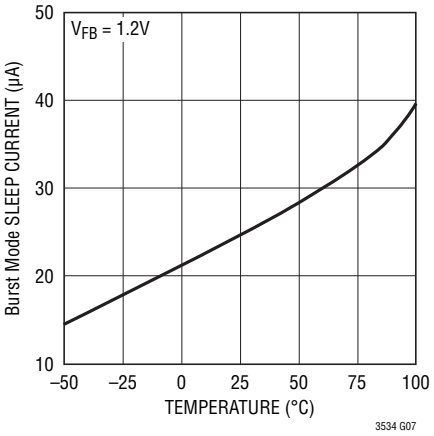
Minimum Start-Up Voltage vs Temperature



Active Quiescent Current vs Temperature

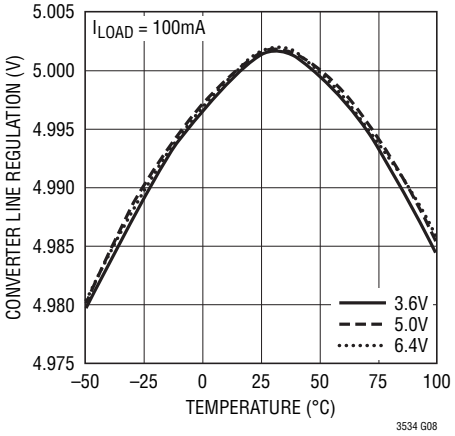


Burst Mode SLEEP Current vs Temperature

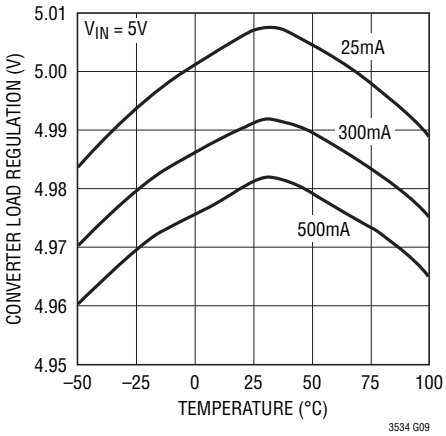


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

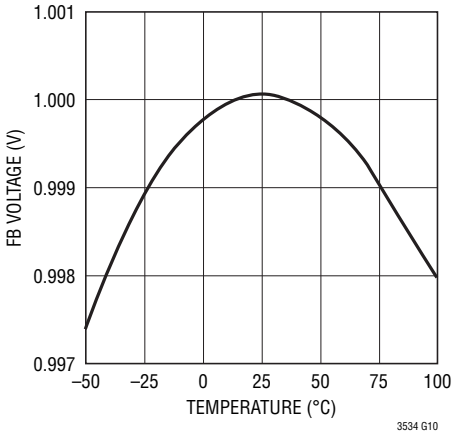
Converter Line Regulation vs Temperature



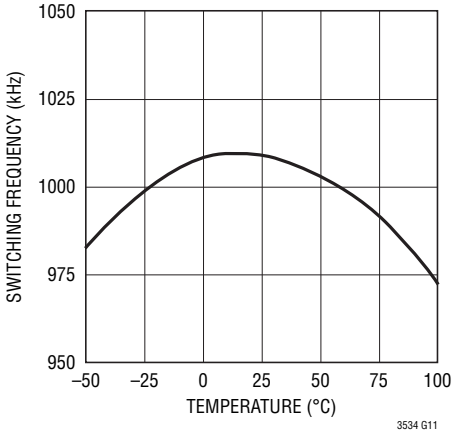
Converter Load Regulation vs Temperature



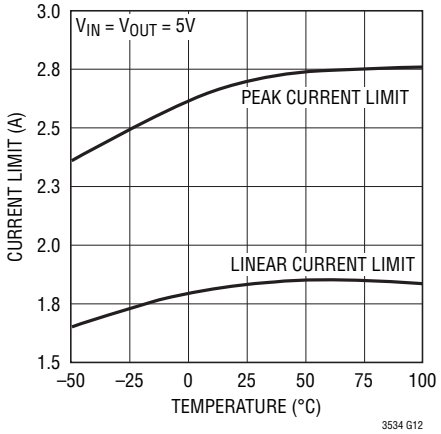
Feedback Voltage vs Temperature



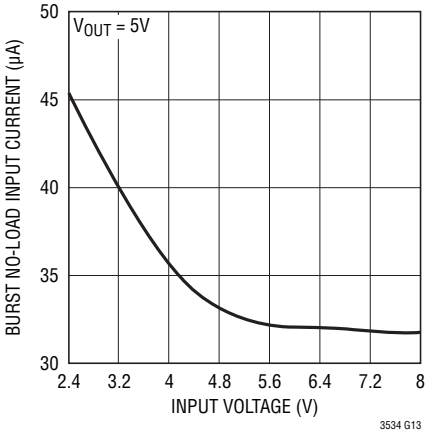
Switching Frequency vs Temperature



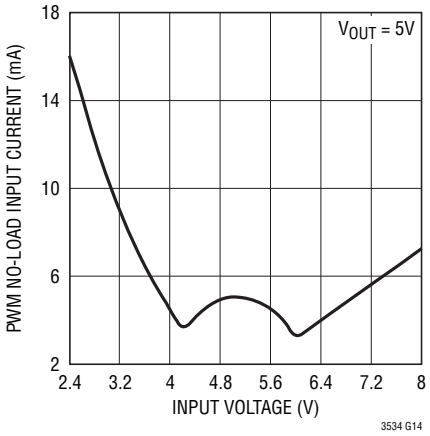
Current Limits vs Temperature



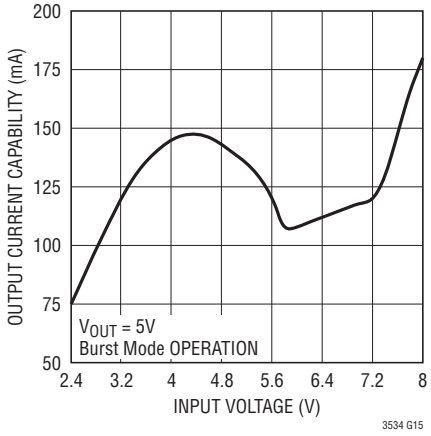
BURST No-Load Input Current vs V_{IN} (Switching)



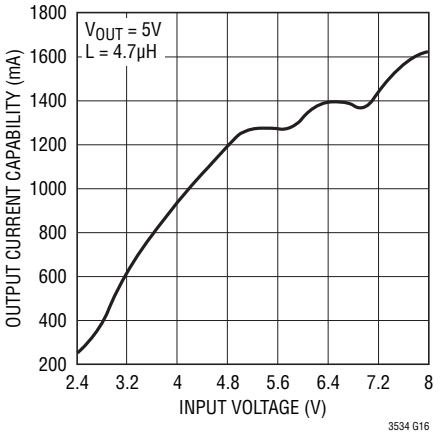
PWM No-Load Input Current vs V_{IN} (Switching)



BURST Maximum Output Current Capability vs V_{IN}

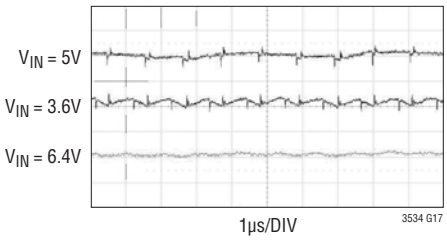


PWM Maximum Output Current Capability vs V_{IN}



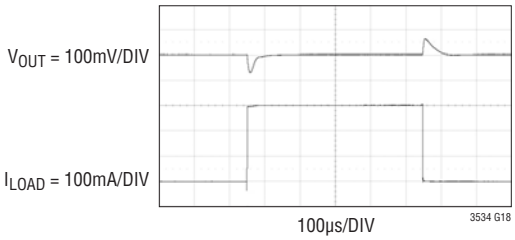
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

V_{OUT} Ripple at 300mA Load



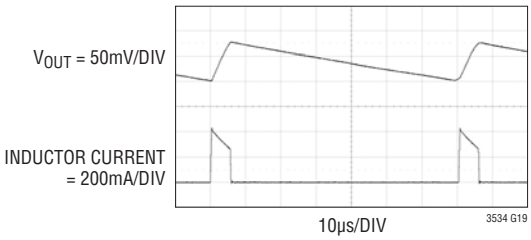
V_{OUT} = 5V, AC-COUPLED
20mV/DIV
C_{OUT} = 22µF
I_{LOAD} = 300mA

Load Transient Response in Fixed Frequency Mode, No-Load to 300mA



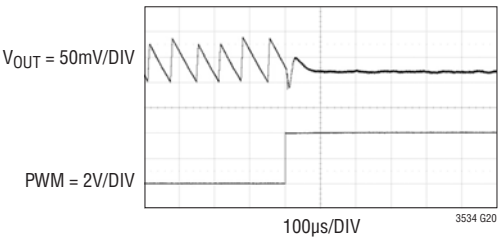
V_{IN} = V_{OUT} = 5V
I_{LOAD} = 0 TO 300mA
C_{OUT} = 22µF
X5R CERAMIC

Burst Mode Operation V_{OUT} Ripple at 25mA Load



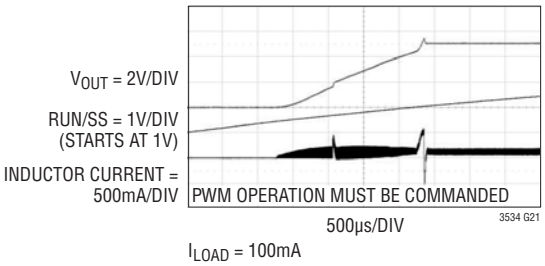
V_{IN} = V_{OUT} = 5V
C_{OUT} = 22µF
X5R CERAMIC

Transition from Burst Mode Operation to Fixed Frequency Mode



V_{IN} = V_{OUT} = 5V
I_{LOAD} = 25mA
C_{OUT} = 22µF
X5R CERAMIC

V_{OUT} Start-Up



I_{LOAD} = 100mA

PIN FUNCTIONS

GND Pads (Pins 1, 8, 9, 16; GN Package): IC Substrate Grounds. These pins **MUST** be soldered to the printed circuit board ground to provide both electrical contact and a good thermal contact to the PCB.

RUN/SS (Pin 2): Combined Shutdown and Soft-Start. Applying a voltage below 400mV shuts down the IC. Apply a voltage above 1.4V to enable the IC and above 2.4V to ensure that the error amp is not clamped from soft-start. An R-C from the enable command signal to this pin will provide a soft-start function by limiting the rise time of the V_C pin. PWM mode operation *must* be commanded to properly enable the IC.

GND (Pin 3): Signal Ground for the IC.

PGND1, PGND2 (Pins 4, 7): Power Ground for the Internal N-channel MOSFET Power Switches (Switches B and C).

SW1 (Pin 5): Switch Pin where Internal Switches A and B are Connected. Connect inductor from SW1 to SW2. Minimize trace length to reduce EMI.

SW2 (Pin 6): Switch Pin where Internal Switches C and D are Connected. Minimize trace length to reduce EMI.

PWM (Pin 10): Burst Mode Select. PWM must be driven HIGH during start-up. When V_{OUT} is in regulation, the PWM pin may be driven LOW to command Burst Mode operation. Applying a voltage below 400mV enables Burst Mode operation, providing a significant efficiency improvement at light loads. Burst Mode operation will continue until this pin is driven high. Applying a voltage above 1.4V disables Burst Mode operation, enabling low noise, fixed frequency operation.

V_{OUT} (Pin 11): Output of the Synchronous Rectifier. A filter capacitor is placed from V_{OUT} to GND. A ceramic bypass capacitor is recommended as close to the V_{OUT} and GND pins as possible. V_{OUT} is given by the following equation:

$$V_{OUT} = 1.000 \bullet \frac{R1+R2}{R2} V$$

PV_{IN} (Pin 12): Power V_{IN} Supply Pin. A 10µF ceramic capacitor is recommended as close to the PV_{IN} and PGND pins as possible.

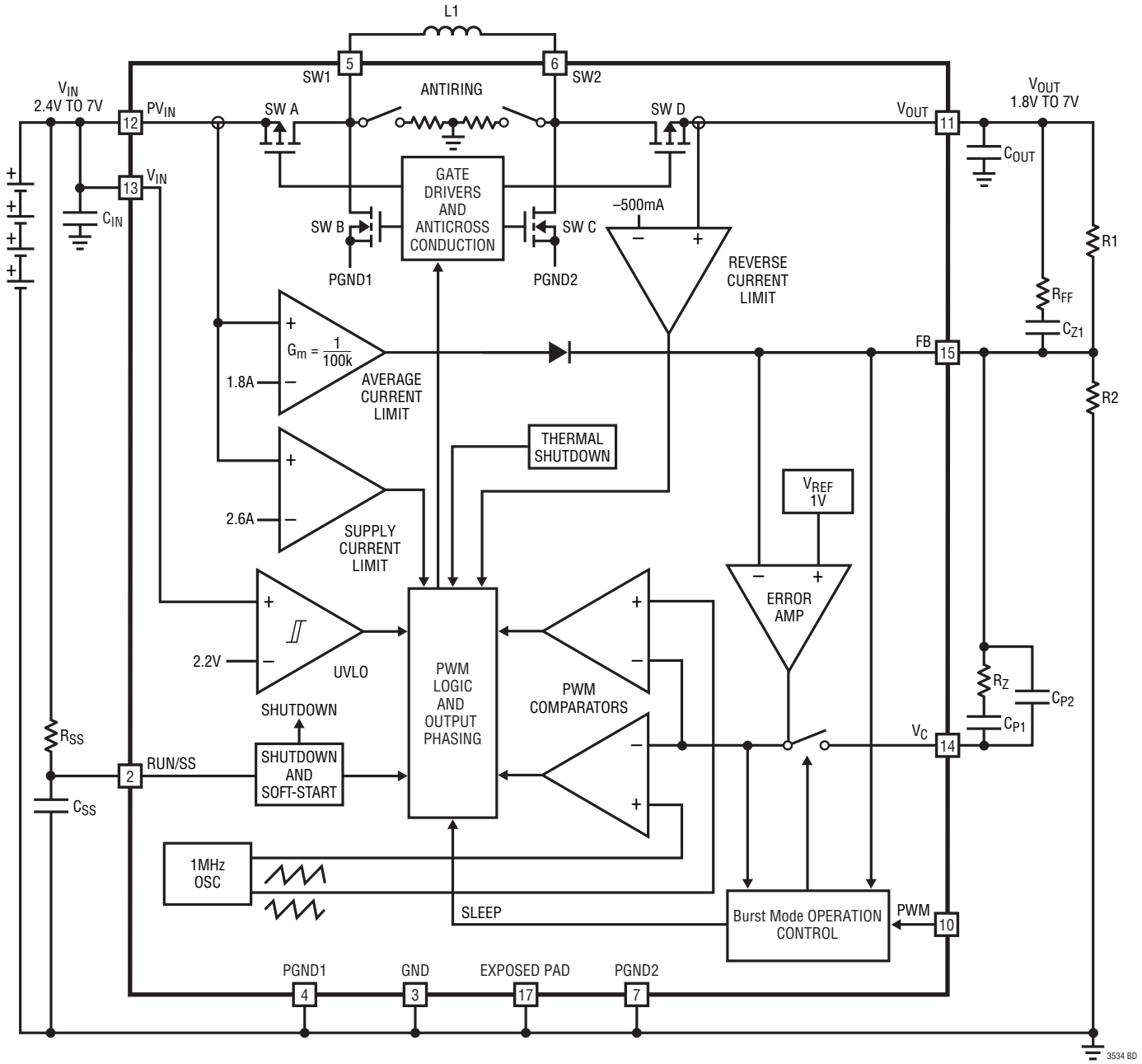
V_{IN} (Pin 13): Input Supply Pin. Connect the power source to this pin.

V_C (Pin 14): Error Amp Output. An R-C network is connected from this pin to FB for loop compensation. Refer to "Closing the Feedback Loop" section for component selection guidelines.

FB (Pin 15): Feedback Pin. Connect V_{OUT} resistor divider tap to this pin. The output voltage can be adjusted from 1.8V to 7V. The feedback reference voltage is typically 1V.

Exposed Pad (Pin 17; DHC Package): IC Substrate Ground. This pin **MUST** be soldered to the printed circuit board ground to provide both electrical contact and a good thermal contact to the PCB.

BLOCK DIAGRAM



OPERATION

The LTC3534 provides high efficiency, low noise power for a wide variety of handheld electronic devices. Linear Technology's proprietary topology allows input voltages above, below or equal to the output voltage by properly phasing the output switches. The error amplifier output voltage on V_C determines the output duty cycle of the switches. Since V_C is a filtered signal, it provides rejection of frequencies from well below the switching frequency. The low $R_{DS(ON)}$, low gate charge synchronous switches provide high frequency pulse width modulation control at high efficiency. High efficiency is achieved at light loads when Burst Mode operation is invoked and the LTC3534's quiescent current drops to a mere 25µA.

LOW NOISE FIXED FREQUENCY OPERATION

Oscillator

The frequency of operation is internally set to 1MHz.

Error Amplifier

The error amplifier is a voltage mode amplifier. The loop compensation components are configured around the amplifier (from FB to V_C) to obtain stability of the converter. For improved bandwidth, an additional R-C feedforward network can be placed across the upper feedback divider resistor. The voltage on RUN/SS clamps the error amplifier output, V_C, to provide a soft-start function.

Supply Current Limits

There are two different supply current limit circuits in the LTC3534, each having internally fixed thresholds.

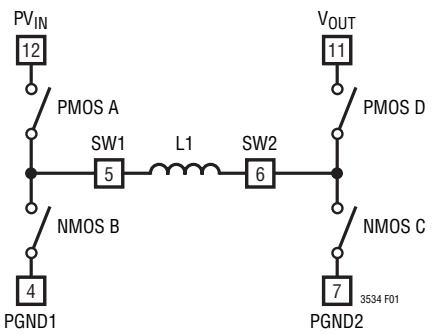


Figure 1. Simplified Diagram of Output Switches

The first circuit is an average current limit amplifier, sourcing current out of FB to drop the output voltage should the peak input current exceed 1.8A typical. This method provides a closed loop means of clamping the input current. During conditions where V_{OUT} is near ground, such as during a short circuit or start-up, this threshold is cut to 800mA typical, providing a foldback feature. For this current limit feature to be most effective, the Thevenin resistance from FB to ground should be greater than 100k.

Should the peak input current exceed 2.6A typical, the second circuit, a high speed peak current limit comparator, shuts off PMOS switch A. The delay to output of this comparator is typically 50ns.

Reverse Current Limit

During fixed frequency operation, the LTC3534 operates in forced continuous conduction mode. The reverse current limit comparator monitors the inductor current from the output through PMOS switch D. Should this negative inductor current exceed 500mA typical, the LTC3534 shuts off switch D.

Four-Switch Control

Figure 1 shows a simplified diagram of how the four internal switches are connected to the inductor, PV_{IN}, V_{OUT}, PGND1 and PGND2. Figure 2 shows the regions of operation for the LTC3534 as a function of the internal control voltage, V_{CI}. Dependent on the magnitude of V_{CI}, the LTC3534 will operate in buck, buck-boost or boost mode. V_{CI} is a level

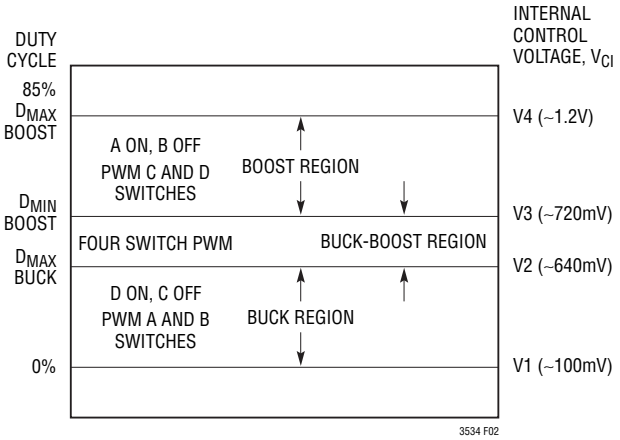


Figure 2. Switch Control vs Internal Control Voltage, V_{CI}

OPERATION

shifted voltage from the output of the error amplifier (V_C pin), see Figure 3. The four power switches are properly phased so the transfer between operating modes is continuous, smooth and transparent to the user. When V_{IN} approaches V_{OUT} the buck-boost region is entered, where the conduction time of the four switch region is typically 125ns. Referring to Figures 1 and 2, the various regions of operation will now be described.

Buck Region ($V_{IN} > V_{OUT}$)

Switch D is always on and switch C is always off during this mode. When the internal control voltage, V_{CI}, is above voltage V1, output A begins to switch. During the off-time of switch A, synchronous switch B turns on for the remainder of the period. Switches A and B will alternate similar to a typical synchronous buck regulator. As the control voltage increases, the duty cycle of switch A increases until the maximum duty cycle of the converter in buck mode reaches D_{MAX_BUCK}, given by:

$$D_{MAX\_BUCK} = (100 - D4_{SW})\%$$

where $D4_{SW}$ = duty cycle % of the four switch range.

$$D4_{SW} = (125ns \bullet f) \bullet 100\%$$

where f = operating frequency in Hz, typically 1MHz.

Hence, $D4_{SW}$ = 12.5% for the LTC3534.

$$D_{MAX\_BUCK} = 87.5\%$$

Beyond this point the "four switch", or buck-boost region is reached.

Buck-Boost or Four Switch ($V_{IN} \sim V_{OUT}$)

When the internal control voltage, V_{CI}, is above voltage V2, switch pair AD remain on for duty cycle D_{MAX_BUCK}, and the switch pair AC begins to phase in. As switch pair AC phases in, switch pair BD phases out accordingly. When V_{CI} reaches the edge of the buck-boost range, at voltage V3, the AC switch pair completely phase out the BD pair, and the boost phase begins at duty cycle $D4_{SW}$.

The input voltage, V_{IN}, where the four switch region begins is given by:

$$V_{IN} = \frac{V_{OUT}}{1-(125ns \bullet f)}\ V$$

The V_{IN} potential at which the four switch region ends is given by:

$$V_{IN} = V_{OUT} \bullet (1 - D) = V_{OUT} \bullet (1 - 125ns \bullet f)\ V$$

where f = operating frequency in Hz, typically 1MHz.

Hence, for the LTC3534,

$$V_{IN(ENTER4SW)} \cong \frac{V_{OUT}}{0.875}\ V$$

Approximate V_{IN} potential at which the four switch region is entered.

$$V_{IN(4SWEXIT)} \cong 0.875 \bullet V_{OUT}\ V$$

Approximate V_{IN} potential at which the four switch region is exited.

Boost Region ($V_{IN} < V_{OUT}$)

Switch A is always on and switch B is always off during this mode. When the internal control voltage, V_{CI}, is above voltage V3, switch pair CD will alternately switch to provide a boosted output voltage. This operation is typical to a synchronous boost regulator. The maximum duty cycle of the converter is limited to 85% typical and is reached when V_{CI} is above V4.

Burst Mode OPERATION

Burst Mode operation reduces the LTC3534's quiescent current consumption at light loads and improves overall conversion efficiency, increasing battery life. During Burst Mode operation the LTC3534 delivers energy to the output until it is regulated and then enters a sleep state where the switches are off and the quiescent current drops to 25µA typical. In this mode the output ripple has a variable frequency component that depends upon load current, and will typically be about 2% peak-to-peak. Burst Mode operation ripple can be reduced slightly by using more output capacitance (47µF or greater). Another method of reducing Burst Mode operation ripple is to place a small feedforward capacitor across the upper resistor in the V_{OUT} feedback divider network (as in Type III compensation), see Figure 6.

OPERATION

In Burst Mode operation the typical maximum average output currents in the three operating regions, buck, four switch, and boost are given by:

$I_{OUT(MAX)BURST–BUCK} \approx 100mA$;

Burst Mode operation – buck region: $V_{IN} > V_{OUT}$

$I_{OUT(MAX)BURST–FOUR\_SWITCH} \approx 125mA$;

Burst Mode operation – four switch region: $V_{IN} \approx V_{OUT}$

$$I_{OUT(MAX)BURST–BOOST} \approx \frac{125 \bullet V_{IN}}{V_{OUT}} \ mA;$$

Burst Mode operation – boost region: $V_{IN} < V_{OUT}$

The efficiency below 1mA becomes dominated primarily by the quiescent current. The Burst Mode operation efficiency is given by:

$$Efficiency \cong \frac{\eta \bullet I_{LOAD}}{25\mu A + I_{LOAD}}$$

where η is typically 90% during Burst Mode operation.

A graph of Burst Mode operation maximum output current vs V_{IN} (for V_{OUT} = 5V) is provided in the Typical Performance Characteristics section.

Burst Mode Operation to Fixed Frequency Transient Response

In Burst Mode operation, the compensation network is not used and V_C is disconnected from the error amplifier. During long periods of Burst Mode operation, leakage currents in the external components or on the PC board could cause the compensation capacitor to charge (or discharge), which could result in a large output transient when returning to fixed frequency mode operation, even at the same load current. To prevent this, the LTC3534 incorporates an active clamp circuit that holds the voltage on V_C at an optimal voltage during Burst Mode operation. This minimizes any output transient when returning to fixed frequency mode operation. For optimum transient response, Type III compensation is also recommended to broad band the control loop and roll off past the two pole response of the output LC filter. (See Closing the Feedback Loop).

Soft-Start

The soft-start function is combined with shutdown. When the RUN/SS pin is brought above 1V typical, the LTC3534 is enabled but the error amplifier duty cycle is clamped from V_C. A detailed diagram of this function is shown in Figure 3. The components R_{SS} and C_{SS} provide a slow ramping voltage on RUN/SS to provide a soft-start function. To ensure that V_C is not being clamped, RUN/SS must be raised to 2.4V or above. The IC must be enabled (even with a soft-start) commanding PWM mode. Once the LTC3534 is in regulation, then Burst Mode operation can be commanded.

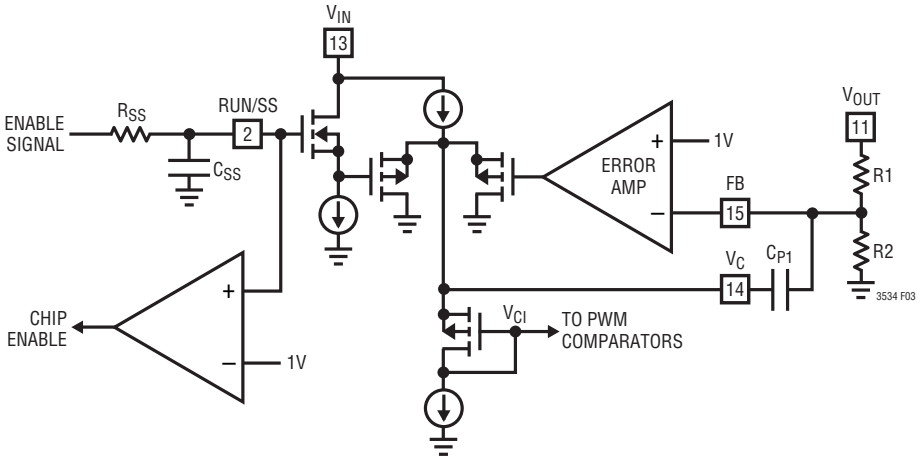


Figure 3. Soft-Start Circuitry

APPLICATIONS INFORMATION

COMPONENT SELECTION

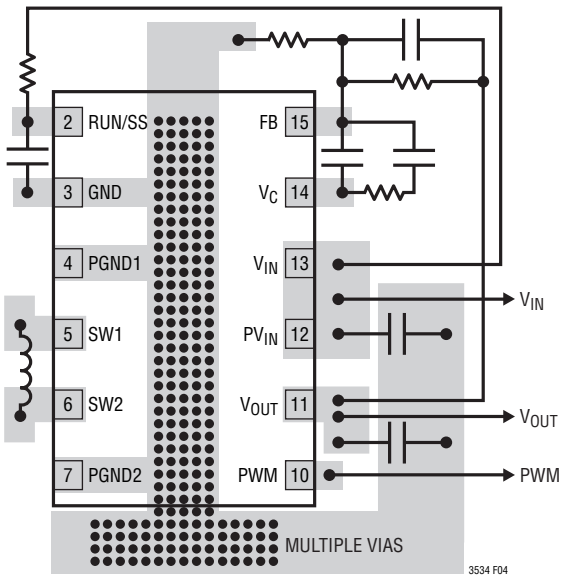


Figure 4. Recommended Component Placement. Traces Carrying High Current are Direct. Trace Area at FB and V_C Pins are Kept Low. Lead Length to Battery Should be Kept Short. Keep V_{OUT} and V_{IN} Ceramic Capacitors Close to their IC Pins.

Inductor Selection

The high frequency operation of the LTC3534 allows the use of small surface mount inductors. The inductor ripple current is typically set to 20% to 40% of the maximum inductor current. For a given ripple the inductance terms are given as follows:

$$L_{BOOST} > \frac{V_{IN(MIN)} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{f \bullet \Delta I_L \bullet V_{OUT}} \text{ H}$$

$$L_{BUCK} > \frac{V_{OUT} \bullet \left(V_{IN(MAX)} - V_{OUT}\right)}{f \bullet \Delta I_L \bullet V_{IN(MAX)}} \text{ H}$$

where f = switching frequency in Hz, typically 1MHz.

ΔI_L = maximum allowable inductor ripple current, A

$V_{IN(MIN)}$ = minimum input voltage, V

$V_{IN(MAX)}$ = maximum input voltage, V

V_{OUT} = output voltage, V

For high efficiency, choose a ferrite inductor with a high frequency core material to reduce core loses. The inductor should have low ESR (equivalent series resistance) to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. Molded chokes or chip inductors usually do not have enough core to support the peak inductor currents in the 1A to 2A region. To minimize radiated noise, use a shielded inductor. See Table 1 for a suggested list of inductor suppliers.

Table 1. Inductor Vendor Information

SUPPLIER	PHONE	FAX OR E-MAIL	WEBSITE
Coilcraft	(847) 639-6400	(847) 639-1469	www.coilcraft.com
FDK	(408) 432-8331	america@fdk.com	www.fdk.com
Murata	(814) 237-1431 (800) 831-9172	(814) 238-0490	www.murata.com
Sumida	USA: (847) 956-0666 Japan: 81(3) 3607-5111	USA: (847) 956-0702 Japan: 81(3) 3607-5144	www.sumida.com
TDK	(847) 803-6100	(847) 803-6296	www.component.tdk.com
TOKO	(847) 297-0070	(847) 699-7864	www.tokoam.com

APPLICATIONS INFORMATION

Output Capacitor Selection

The bulk value of the output filter capacitor is set to reduce the ripple due to charge into the capacitor each cycle. The steady state ripple due to charge is given by:

$$\Delta V_{P-P}\,Boost = \frac{I_{OUT} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{C_{OUT} \bullet V_{OUT} \bullet f}\ V$$

$$\Delta V_{P-P}\,Buck = \frac{1}{8 \bullet L \bullet C_{OUT} \bullet f^2} \bullet \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \bullet V_{OUT}}{V_{IN(MAX)}}\ V$$

where f = switching frequency in Hz, typically 1MHz.

C_{OUT} = output filter capacitor, F

I_{OUT} = output load current, A

The output capacitance is usually many times larger than the minimum value in order to handle the transient response requirements of the converter. As a rule of thumb, the ratio of the operating frequency to the unity-gain bandwidth of the converter is the amount the output capacitance will have to increase from the above calculations in order to maintain the desired transient response. A 22µF or larger ceramic capacitor is appropriate for most applications.

The other component of ripple is due to the ESR (equivalent series resistance) of the output capacitor. Low ESR capacitors should be used to minimize output voltage ripple. For surface mount applications, Taiyo Yuden or TDK ceramic capacitors, AVX TPS series tantalum capacitors or Sanyo POSCAP are recommended. See Table 2 for contact information.

Table 2. Capacitor Vendor Information

SUPPLIER	PHONE	FAX	WEBSITE
AVX	(803) 448-9411	(803) 448-1943	www.avxcorp.com
Sanyo	(619) 661-6322	(619) 661-1055	www.sanyovideo.com
Taiyo Yuden	(408) 573-4150	(408) 573-4159	www.t-yuden.com
TDK	(847) 803-6100	(847) 803-6296	www.component.tdk.com

Input Capacitor Selection

Since V_{IN} is the supply voltage for the IC, as well as the input to the power stage of the converter, it is recommended to place at least a 10µF, low ESR ceramic bypass capacitor close to the PV_{IN}/V_{IN} and PGND/GND pins. It is also important to minimize any stray resistance from the converter to the battery or other power source.

Optional Schottky Diodes

Schottky diodes across the synchronous switches B and D are not required, but do provide a lower drop during the break-before-make time (typically 15ns), thus improving efficiency. Use a surface mount Schottky diode such as an MBRM120T3 or equivalent. Do not use ordinary rectifier diodes since their slow recovery times will compromise efficiency.

Output Voltage < 1.8V

The LTC3534 can operate as a buck converter with output voltages as low as 400mV. Since synchronous switch D is powered from V_{OUT} and the $R_{DS(ON)}$ will increase significantly at output voltages below 1.8V typical, a Schottky diode is required from SW2 to V_{OUT} to provide the conduction path to the output at low V_{OUT} voltages. The current limit is folded back to 800mA when V_{OUT} < 0.9V typical which will significantly reduce the output current capability of the application. Note that Burst Mode operation is inhibited at output voltages below 1.6V typical.

Closing the Feedback Loop

The LTC3534 incorporates voltage mode PWM control. The control to output gain varies with operation region (buck, boost, buck-boost), but is usually no greater than 15. The output filter exhibits a double pole response, as given by:

$$f_{FILTER\_POLE} = \frac{1}{2 \bullet \pi \bullet \sqrt{L1 \bullet C_{OUT}}}\ Hz\ (in\ buck\ mode)$$

$$f_{FILTER\_POLE} = \frac{V_{IN}}{2 \bullet V_{OUT} \bullet \pi \bullet \sqrt{L1 \bullet C_{OUT}}}\ Hz\ (in\ boost\ mode)$$

where L1 is in Henries and C_{OUT} is in Farads.

The output filter zero is given by:

APPLICATIONS INFORMATION

$$f_{FILTER\_ZERO} = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}} \text{ Hz}$$

where R_{ESR} is the equivalent series resistance of the output capacitor.

A troublesome feature in boost mode is the right-half plane zero (RHP), given by:

$$f_{RHPZ} = \frac{V_{IN}^{2}}{2 \bullet \pi \bullet I_{OUT} \bullet L1 \bullet V_{OUT}} \text{ Hz}$$

The loop gain is typically rolled off before the RHP zero frequency.

A simple Type I compensation network can be incorporated to stabilize the loop, but at a cost of reduced bandwidth and slower transient response. To ensure proper phase margin using Type I compensation, the loop must be crossed over a decade before the LC double pole. Referring to Figure 5, the unity-gain frequency of the error amplifier utilizing Type I compensation is given by:

$$f_{UG} = \frac{1}{2 \bullet \pi \bullet R1 \bullet C_{P1}} \text{ Hz}$$

Most applications demand an improved transient response to allow a smaller output filter capacitor. To achieve a higher bandwidth, Type III compensation is required, providing two zeros to compensate for the double-pole response of the output filter. Referring to Figure 6, the location of the poles and zeros are given by:

$$f_{POLE1} \cong \frac{1}{2 \bullet \pi \bullet 5 \times 10^{3} \bullet R1 \bullet C_{P1}} \text{ Hz}$$

(which is extremely close to DC)

$$f_{ZERO1} = \frac{1}{2 \bullet \pi \bullet R_{Z} \bullet C_{P1}} \text{ Hz}$$

$$f_{ZERO2} = \frac{1}{2 \bullet \pi \bullet R1 \bullet C_{Z1}} \text{ Hz}$$

$$f_{POLE2} = \frac{1}{2 \bullet \pi \bullet R_{Z} \bullet C_{P2}} \text{ Hz}$$

where resistance is in Ohms and capacitance is in Farads.

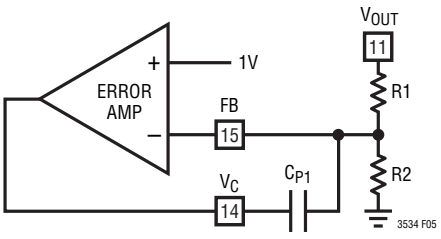


Figure 5. Error Amplifier with Type I Compensation

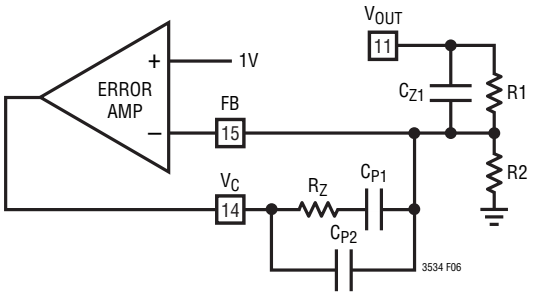
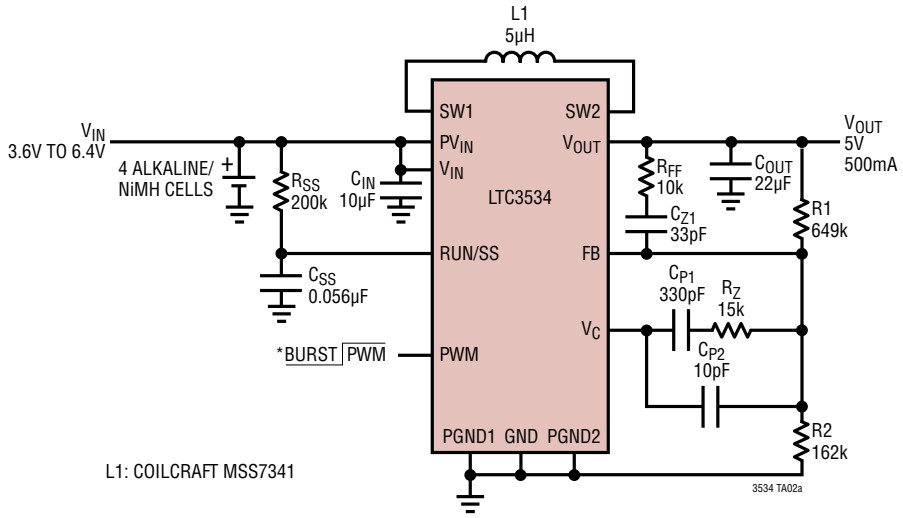


Figure 6. Error Amplifier with Type III Compensation

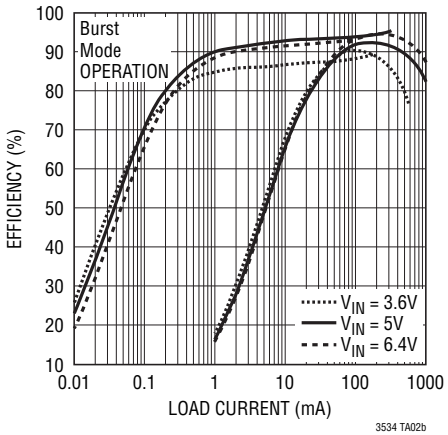
TYPICAL APPLICATIONS

4 Alkaline/NiMH to 5V at 500mA



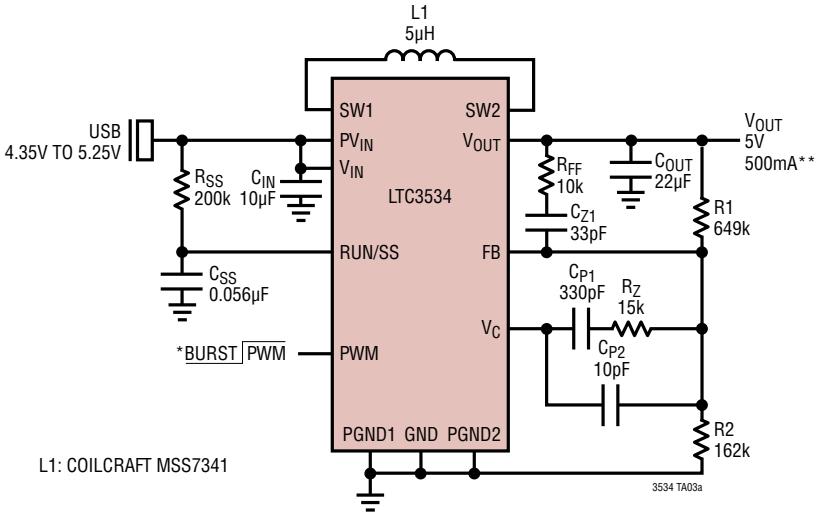
*PWM MUST BE DRIVEN HIGH DURING START-UP. WHEN V_{OUT} IS IN REGULATION, THE PWM PIN MAY BE DRIVEN LOW TO COMMAND BURST MODE OPERATION.

4 Alkaline/NiMH Cells to 5V Efficiency vs I_{LOAD}



TYPICAL APPLICATIONS

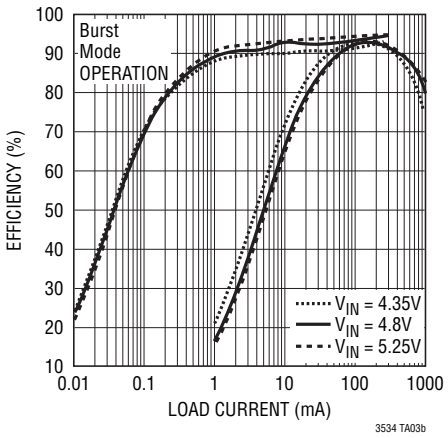
USB to 5V at 500mA



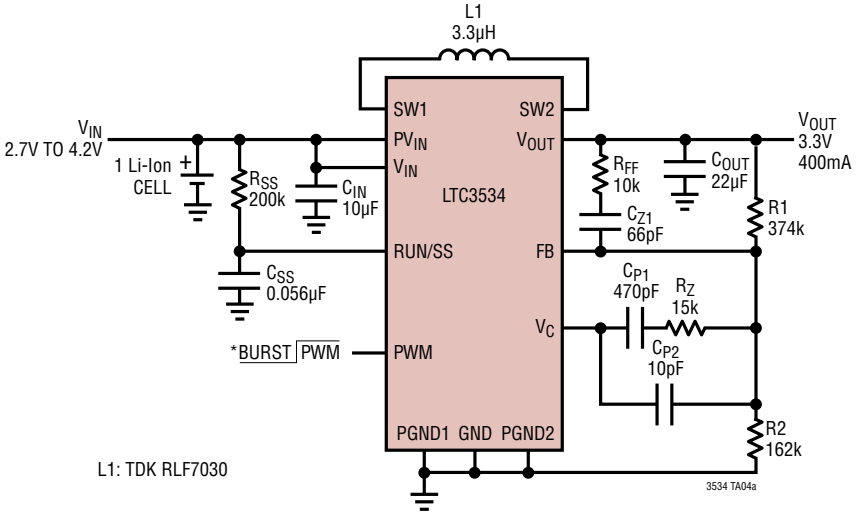
*PWM MUST BE DRIVEN HIGH DURING START-UP. WHEN V_{OUT} IS IN REGULATION, THE PWM PIN MAY BE DRIVEN LOW TO COMMAND BURST MODE OPERATION.

**NOTE: OUTPUT CURRENT CAN BE LESS THAN 500mA IF USB INPUT CURRENT LIMIT REACHED.

USB to 5V Efficiency vs I_{LOAD}

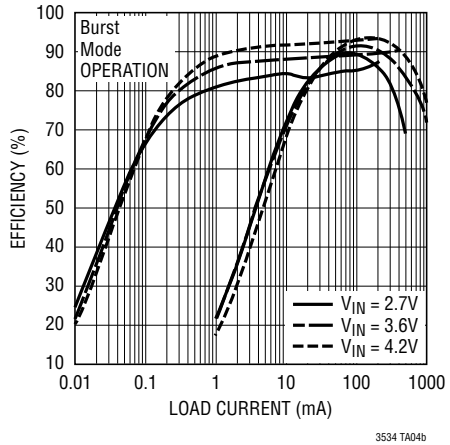


Li-Ion to 3.3V at 400mA



*PWM MUST BE DRIVEN HIGH DURING START-UP. WHEN V_{OUT} IS IN REGULATION, THE PWM PIN MAY BE DRIVEN LOW TO COMMAND BURST MODE OPERATION.

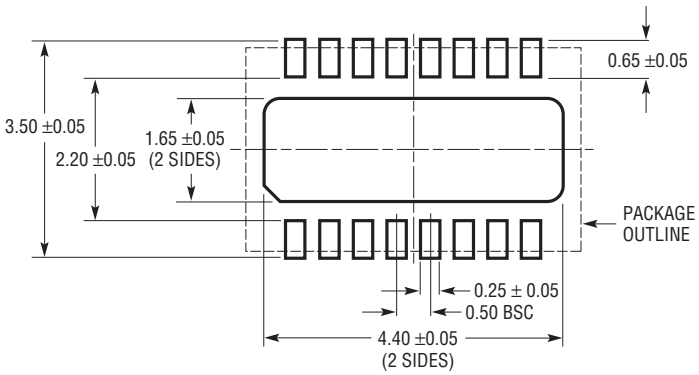
Li-Ion to 3.3V Efficiency vs I_{LOAD}



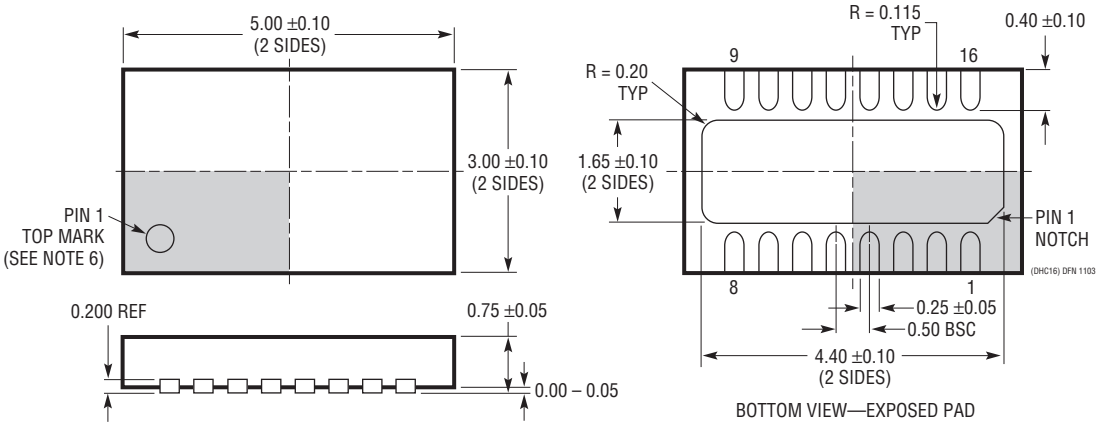
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



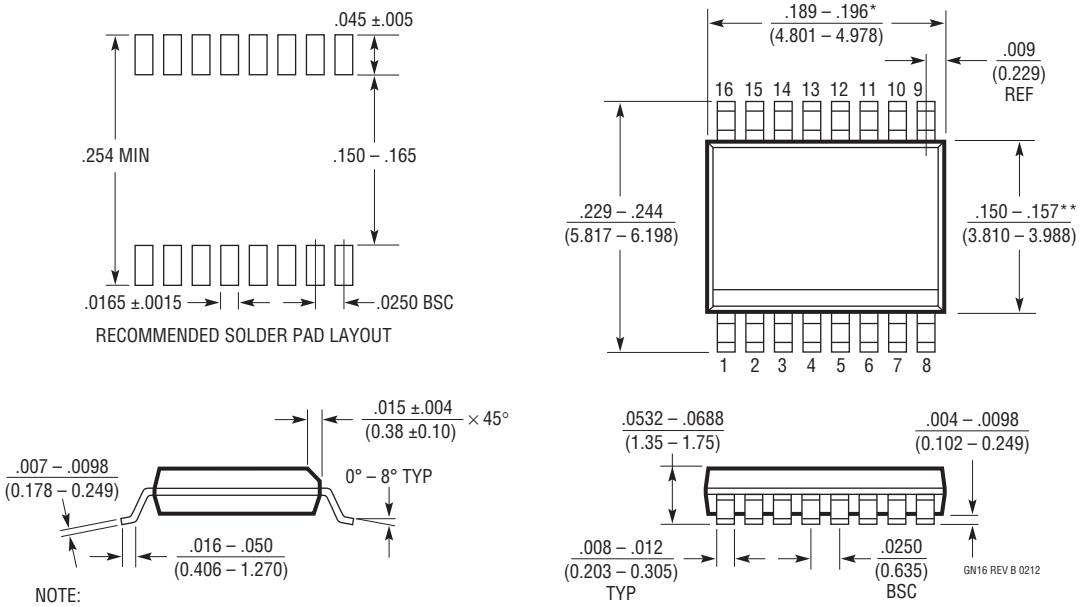
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	02/14	Updated BURST Maximum Output Current Capability vs V_{IN} curve.	5
		Added note to V_{OUT} Start-Up scope photo.	6
		Modified RUN/SS and PWM pin descriptions.	7
		Modified Burst Mode current equations and Soft-Start section.	11
		Added start-up conditions to Typical Applications figures.	15, 16

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3125	1.2A (I_{SW}), 1.5MHz, Synchronous Step-Up DC/DC Converter with Programmable Input Current	93% Efficiency, V_{IN}: 1.8V to 5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 15µA, I_{SD} < 1µA, ±5% Input Current Accuracy, 200mA to 1A Program Range, 2mm × 3mm DFN Package
LTC3421	3A (I_{SW}), 3MHz, Synchronous Step-Up DC/DC Converter with Output Disconnect	96% Efficiency, V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 12µA, I_{SD} <1µA, QFN24 Package
LTC3422	1.5A (I_{SW}), 3MHz, Synchronous Step-Up DC/DC Converter with Output Disconnect	96% Efficiency, V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 25µA, I_{SD} <1µA, DFN10 Package
LTC3425	5A (I_{SW}), 8MHz (Low Ripple), 4-Phase Synchronous Step-Up DC/DC Converter with Output Disconnect	95% Efficiency, V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 12µA, I_{SD} <1µA, QFN32 Package
LTC3429	600mA (I_{SW}), 500KHz, Synchronous Step-Up DC/DC Converter with Output Disconnect and Soft-Start	96% Efficiency, V_{IN}: 0.5V to 4.4V, $V_{OUT(MAX)}$ = 5V, I_Q = 20µA, I_{SD} <1µA, ThinSOT-23 Package
LTC3440	600mA (I_{OUT}), 2MHz, Synchronous Buck-Boost DC/DC Converter	96% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MAX)}$ = 5.5V, I_Q = 25µA, I_{SD} <1µA, MSOP and DFN Packages
LTC3441/LTC3443	1.2A (I_{OUT}), 1MHz/600kHz, Synchronous Buck-Boost DC/DC Converter	95%/96% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 35µA/28µA, I_{SD} <1µA, MSOP Packages
LTC3442	1.2A (I_{OUT}), 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 25µA, I_{SD} <1µA, DFN Package
LTC3444	400mA (I_{OUT}), 1.5MHz, Synchronous Buck-Boost DC/DC Converter with wide V_{OUT} Range	93% Efficiency, V_{IN}: 2.7V to 5.5V, V_{OUT}: 0.5V to 5V, I_{SD} <1µA, DFN Package, Ideal for WCDMA PA Bias
LTC3520	1A (I_{OUT}), 2MHz Synchronous Buck-Boost, 600mA Buck DC/DC Converter	95% Efficiency, V_{IN}: 2.2V to 5.5V, $V_{OUT(MAX)}$ = 5.25V, $V_{OUT(MIN)}$ = 0.8V; I_Q = 55µA, I_{SD} < 1µA, QFN Package
LTC3522	Synchronous 400mA (I_{OUT}) Buck-Boost and 200mA (I_{OUT}) Buck, 1MHz, DC/DC Converters	95% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MAX)}$ = 5.25V, $V_{OUT(MIN)}$ = 0.6V; I_Q = 25µA, I_{SD} <1µA, QFN Package
LTC3526L	500mA (I_{OUT}), 1MHz Synchronous Step-Up DC/DC Converter with Output Disconnect	94% Efficiency, V_{IN}: 0.8V to 5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 9µA, I_{SD} <1µA, 2mm × 2mm DFN-6 Package
LTC3530	600mA (I_{OUT}), 2MHz, Synchronous Buck-Boost DC/DC Converter with Wide Input Voltage Range	96% Efficiency, V_{IN}: 1.8V to 5.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 40µA, I_{SD} <1µA, MSOP and DFN Packages
LTC3531	200mA (I_{OUT}), Burst Mode Operation, Synchronous Buck-Boost DC/DC Converter with Adjustable and Fixed V_{OUT} Versions	90% Efficiency, V_{IN}: 1.8V to 5.5V, $V_{OUT(MAX)}$ = 5V, I_Q = 16µA Always since Burst Mode Operation, I_{SD} <1µA, Small ThinSOT and DFN Packages
LTC3532	500mA (I_{OUT}), 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 35µA, I_{SD} <1µA, MSOP and DFN Packages
LTC3533	2A (I_{OUT}), 2MHz, Synchronous Buck-Boost DC/DC Converter with Wide Input Voltage Range	96% Efficiency, V_{IN}: 1.8V to 5.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 40µA, I_{SD} <1µA, MSOP and DFN Packages
LTC3538	800mA (I_{OUT}), 1MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 35µA, I_{SD} = 1.5µA, DFN Package

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LTC3534
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