ABSOLUTE MAXIMUM RATINGS

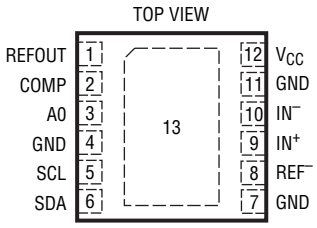
(Notes 1, 2)

Supply Voltage (V_{CC}) ..... –0.3V to 6V
Analog Input Voltage
(V_{IN}^+, V_{IN}^-, V_{IN}, V_{REF}^-,
V_{COMP}, V_{REFOUT}) ..... –0.3V to (V_{CC} + 0.3V)
Digital Voltage
(V_{SDA}, V_{SCL}, V_{A0}) ..... –0.3V to (V_{CC} + 0.3V)

Storage Temperature Range ..... –65°C to 150°C
Operating Temperature Range
LTC2461C/LTC2463C ..... 0°C to 70°C
LTC2461I/LTC2463I ..... –40°C to 85°C

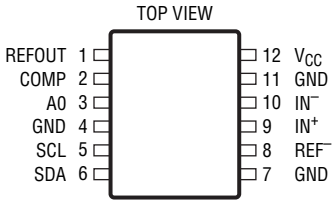
PIN CONFIGURATION

LTC2463



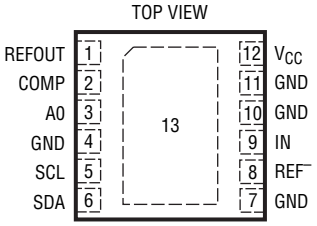
DD PACKAGE
12-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13)

LTC2463



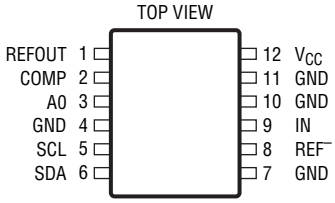
MS PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 135°C/W

LTC2461



DD PACKAGE
12-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13)

LTC2461



MS PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 135°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2461CDD#PBF	LTC2461CDD#TRPBF	LFGF	12-Lead Plastic (3mm × 3mm) DFN	0°C to 70°C
LTC2461IDD#PBF	LTC2461IDD#TRPBF	LFGF	12-Lead Plastic (3mm × 3mm) DFN	–40°C to 85°C
LTC2461CMS#PBF	LTC2461CMS#TRPBF	2461	12-Lead Plastic MSOP	0°C to 70°C
LTC2461IMS#PBF	LTC2461IMS#TRPBF	2461	12-Lead Plastic MSOP	–40°C to 85°C
LTC2463CDD#PBF	LTC2463CDD#TRPBF	LFGG	12-Lead Plastic (3mm × 3mm) DFN	0°C to 70°C
LTC2463IDD#PBF	LTC2463IDD#TRPBF	LFGG	12-Lead Plastic (3mm × 3mm) DFN	–40°C to 85°C
LTC2463CMS#PBF	LTC2463CMS#TRPBF	2463	12-Lead Plastic MSOP	0°C to 70°C
LTC2463IMS#PBF	LTC2463IMS#TRPBF	2463	12-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	(Note 3)	●	16			Bits
Integral Nonlinearity	(Note 4)	●		1	8	LSB
Offset Error	LTC2461, 30Hz, LTC2463 LTC2461, 60Hz	●		2 5	15	LSB LSB
Offset Error Drift				0.02		LSB/°C
Gain Error	Includes Contributions of ADC and Internal Reference	●		±0.01	±0.25	% of FS
Gain Error Drift	Includes Contributions of ADC and Internal Reference C-Grade I-Grade	●		 ±2 ±5	 ±10	 ppm/°C ppm/°C
Transition Noise				2.2		μV_{RMS}
Power Supply Rejection DC				80		dB

ANALOG INPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}^+	Positive Input Voltage Range	LTC2463	●	0		V_{REF}	V
V_{IN}^-	Negative Input Voltage Range	LTC2463	●	0		V_{REF}	V
V_{IN}	Input Voltage Range	LTC2461	●	0		V_{REF}	V
V_{OR}^+, V_{UR}^+	Overrange/Underrange Voltage, IN^+	V_{IN}^- = 0.625V (See Figure 3)			8		LSB
V_{OR}^-, V_{UR}^-	Overrange/Underrange Voltage, IN–	V_{IN}^+ = 0.625V (See Figure 3)			8		LSB
C_{IN}	IN^+, IN^-, IN Sampling Capacitance				0.35		pF
$I_{DC\_LEAK(IN^+, IN^-, IN)}$	IN^+, IN^- DC Leakage Current (LTC2463) IN DC Leakage Current (LTC2461)	V_{IN} = GND or V_{CC} (Note 8) V_{IN} = GND or V_{CC} (Note 8)	● ●	–10 –10	1 1	10 10	nA nA
I_{CONV}	Input Sampling Current (Note 5)				50		nA
V_{REF}	REFOUT Output Voltage		●	1.247	1.25	1.253	V
	REFOUT Voltage Temperature Coefficient	(Note 9) C-Grade I-Grade	●		 ±2 ±5	 ±10	 ppm/°C ppm/°C
	Reference Line Regulation	2.7V ≤ V_{CC} ≤ 5.5V			–90		dB
	Reference Short Circuit Current	V_{CC} = 5.5, Forcing REFOUT to GND	●			35	mA
	COMP Pin Short Circuit Current	V_{CC} = 5.5, Forcing REFOUT to GND	●			200	µA
	Reference Load Regulation	2.7V ≤ V_{CC} ≤ 5.5V, I_{OUT} = 100µA Sourcing			3.5		mV/mA
	Reference Output Noise Density	C_{COMP}= 0.1µF, C_{REFOUT} = 0.1µF, At f = 1kHz			30		$nV/\sqrt{Hz}$

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current Conversion Nap Sleep		 ● ● ●		 1.5 800 0.2	 2.5 1500 2	 mA µA µA

I²C INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 2, 7)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	$0.7V_{CC}$			V
V_{IL}	Low Level Input Voltage		●			$0.3V_{CC}$	V
I_I	Digital Input Current		●	–10		10	µA
V_{HYS}	Hysteresis of Schmidt Trigger Inputs	(Note 3)	●	$0.05V_{CC}$			V
V_{OL}	Low Level Output Voltage (SDA)	I = 3mA	●			0.4	V
I_{IN}	Input Leakage	$0.1V_{CC} \le V_{IN} \le 0.9V_{CC}$	●			1	µA
C_I	Capacitance for Each I/O Pin		●	10			pF
C_B	Capacitance Load for Each Bus Line		●			400	pF
$V_{IH(A0)}$	High Level Input Voltage for Address Pin		●	$0.95V_{CC}$			V
$V_{IL(A0)}$	Low Level Input Voltage for Address Pin		●			$0.05V_{CC}$	V

I²C TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 2, 7)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{CONV}	Conversion Time		●	13	16.6	23	ms
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(SDA,STA)}$	Hold Time (Repeated) START Condition		●	0.6			µs
t_{LOW}	LOW Period of the SCL Pin		●	1.3			µs
t_{HIGH}	HIGH Period of the SCL Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated START Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time for SDA, SCL Signals	(Note 6)	●	$20 + 0.1C_B$		300	ns
t_f	Fall Time for SDA, SCL Signals	(Note 6)	●	$20 + 0.1C_B$		300	ns
$t_{SU(STO)}$	Set-Up Time for STOP Condition		●	0.6			µs
t_{BUF}	Bus Free Time Between a Stop and Start Condition		●	1.3			µs
t_{OF}	Output Fall Time V_{IHMIN} to V_{ILMAX}	Bus Load C_B = 10pF to 400pF (Note 6)	●	$20 + 0.1C_B$		250	ns
t_{SP}	Input Spike Suppression		●			50	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND. V_{CC} = 2.7V to 5.5V unless otherwise specified.

Note 3: Guaranteed by design, not subject to test.

Note 4: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. Guaranteed by design and test correlation.

Note 5: Input sampling current is the average input current drawn from the input sampling network while the LTC2461/LTC2463 are converting.

Note 6: C_B = capacitance of one bus line in pF.

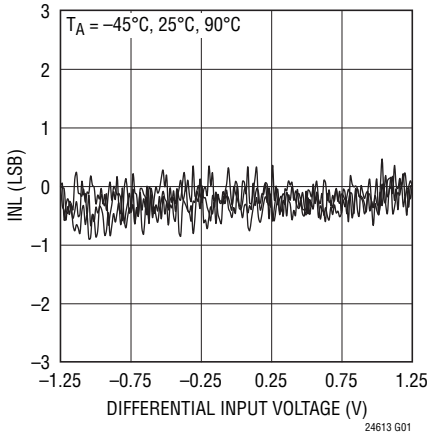
Note 7: All values refer to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

Note 8: A positive current is flowing into the DUT pin.

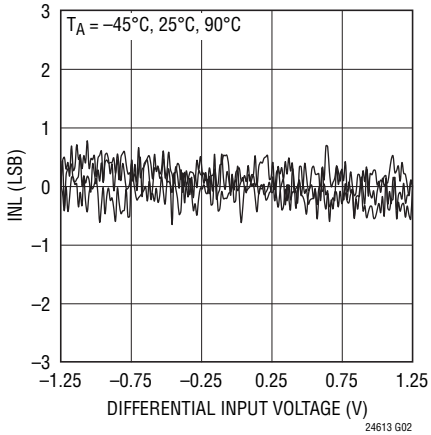
Note 9: Voltage temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

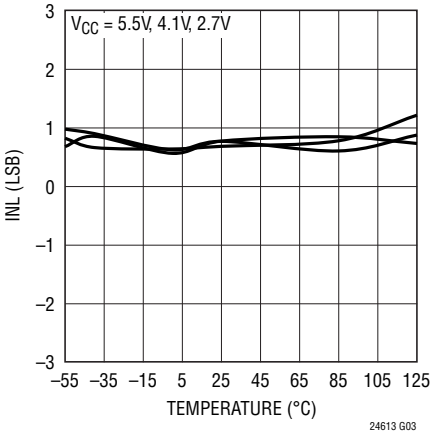
Integral Nonlinearity (V_{CC} = 5.5V)



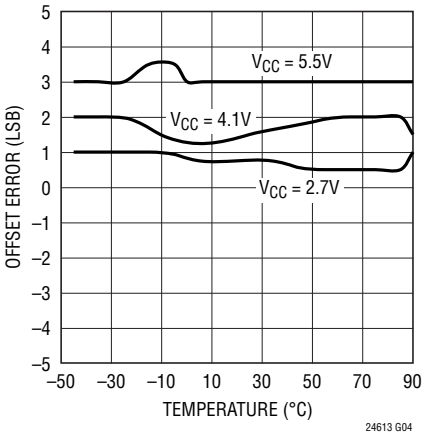
Integral Nonlinearity (V_{CC} = 2.7V)



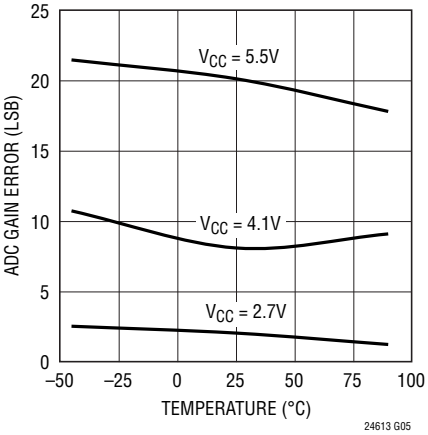
INL vs Temperature



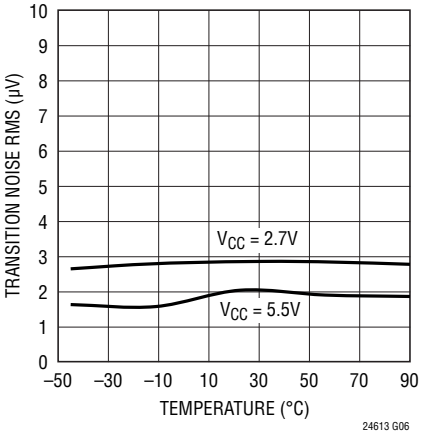
Offset Error vs Temperature



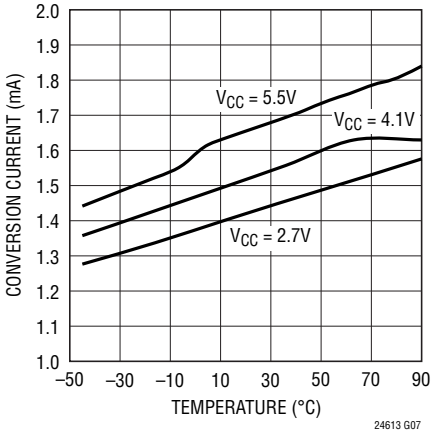
ADC Gain Error vs Temperature



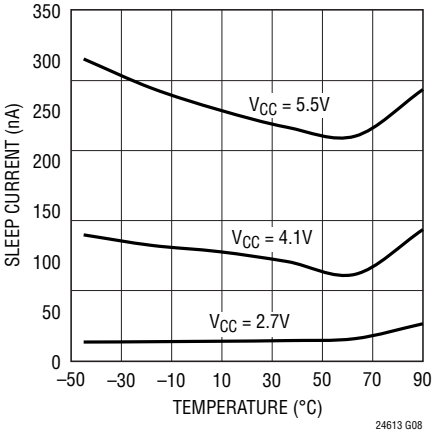
Transition Noise vs Temperature



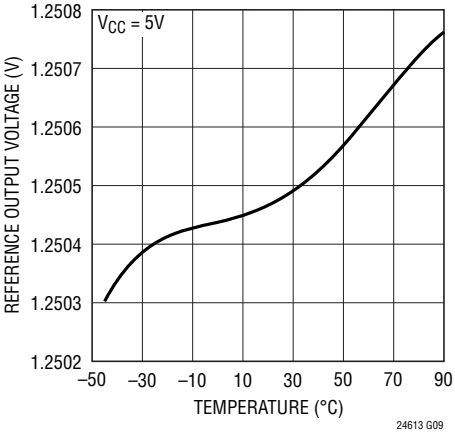
Conversion Mode Power Supply Current vs Temperature



Sleep Mode Power Supply Current vs Temperature

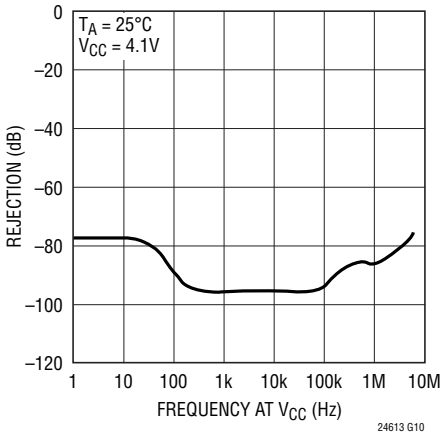


V_{REF} vs Temperature

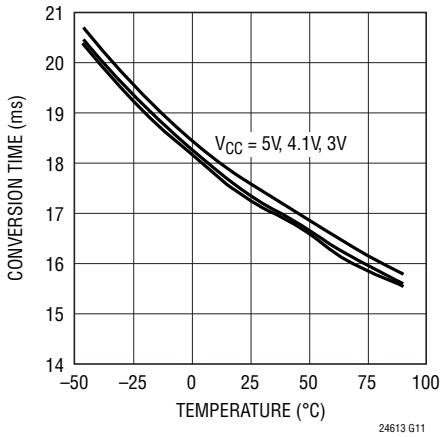


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

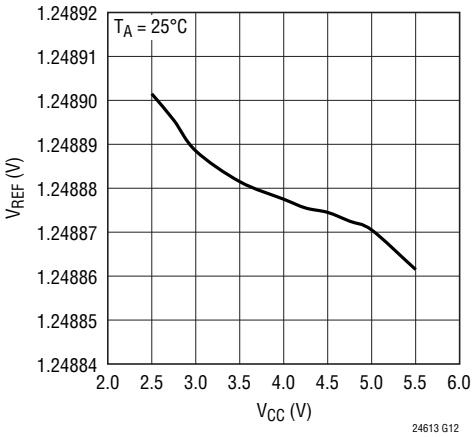
Power Supply Rejection vs Frequency at V_{CC}



Conversion Time vs Temperature



V_{REF} vs V_{CC}



PIN FUNCTIONS

REFOUT (Pin 1): Reference Output Pin. Nominally 1.25V, this voltage sets the fullscale input range of the ADC. For noise and reference stability connect to a 0.1µF capacitor tied to GND. This capacitor value must be less than or equal to the capacitor tied to the reference compensation pin (COMP). REFOUT cannot be overdriven by an external reference. For applications that require an input range greater than 0V to 1.25V, please refer to the LTC2451/LTC2453.

COMP (Pin 2): Internal Reference Compensation Pin. For low noise and reference stability, tie a 0.1µF capacitor to GND.

A0 (Pin 3): Chip Address Control Pin. The A0 pin can be tied to GND or V_{CC}. If A0 is tied to GND, the LTC2461/LTC2463 I^2C address is 0010100. If A0 is tied to V_{CC}, the LTC2461/LTC2463 I^2C address is 1010100.

GND (Pins 4, 7, 11): Ground. Connect directly to the ground plane through a low impedance connection.

SCL (Pin 5): Serial Clock Input of the I^2C Interface. The LTC2461/LTC2463 can only act as a slave and the SCL pin only accepts external serial clock. Data is shifted into the SDA pin on the rising edges of SCL and output through the SDA pin on the falling edges of SCL.

SDA (Pin 6): Bidirectional Serial Data Line of the I^2C Interface. The conversion result is output through the SDA pin. The pin is high impedance unless the LTC2461/LTC2463 is in the data output mode. While the LTC2461/LTC2463 is in the data output mode, SDA is an open drain pull down (which requires an external 1.7k pull-up resistor to V_{CC}).

REF^- (Pin 8): Negative Reference Input to the ADC. The voltage on this pin sets the zero input to the ADC. This pin should tie directly to ground or the ground sense of the input sensor.

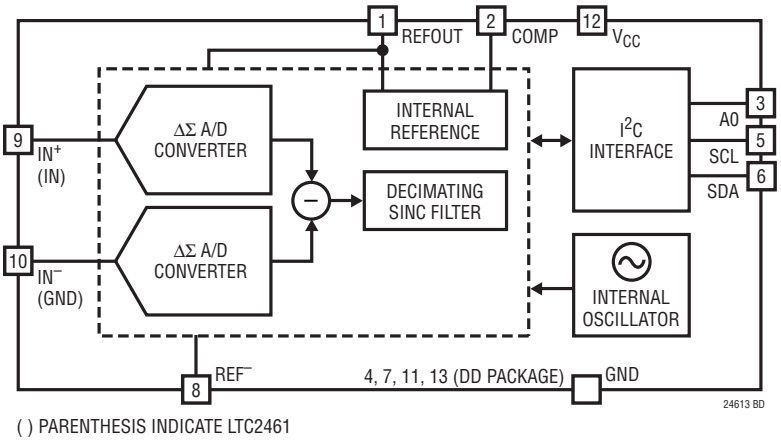
IN^+ (LTC2463), IN (LTC2461) (Pin 9): Positive input voltage for the LTC2463 differential device. ADC input for the LTC2461 single-ended device.

IN^- (LTC2463), GND (LTC2461) (Pin 10): Negative input voltage for the LTC2463 differential device. GND for the LTC2461 single-ended device.

V_{CC} (Pin 12): Positive Supply Voltage. Bypass to GND with a 10µF capacitor in parallel with a low-series-inductance 0.1µF capacitor located as close to pin 12 as possible.

Exposed Pad (Pin 13 – DFN Package): Ground. Connect directly to the ground plane through a low impedance connection.

BLOCK DIAGRAM



( ) PARENTHESIS INDICATE LTC2461

Figure 1. Functional Block Diagram

APPLICATIONS INFORMATION

CONVERTER OPERATION

Converter Operation Cycle

The LTC2461/LTC2463 are low power, delta sigma, analog to digital converters with a simple I²C interface (see Figure 1). The LTC2463 has a fully differential input while the LTC2461 is single-ended. Both are pin and software compatible. Their operation is composed of three distinct states: CONVERT, SLEEP/NAP, and DATA INPUT/OUTPUT (see Figure 2). The operation begins with the CONVERT state. Once the conversion is finished, the converter automatically powers down (NAP) or, under user control, both the converter and reference are powered down (SLEEP). The conversion result is held in a static register while the device is in this state. The cycle concludes with the DATA INPUT/OUTPUT state. Once all 16-bits are read the device begins a new conversion.

The CONVERT state duration is determined by the LTC2461/LTC2463 conversion time (nominally 16.6 milliseconds). Once started, this operation can not be aborted except by a low power supply condition (V_{CC} < 2.1V) which generates an internal power-on reset signal.

After the completion of a conversion, the LTC2461/LTC2463 enters the SLEEP/NAP state and remains there until a valid read/write is acknowledged. Following this condition, the ADC transitions into the DATA INPUT/OUTPUT state.

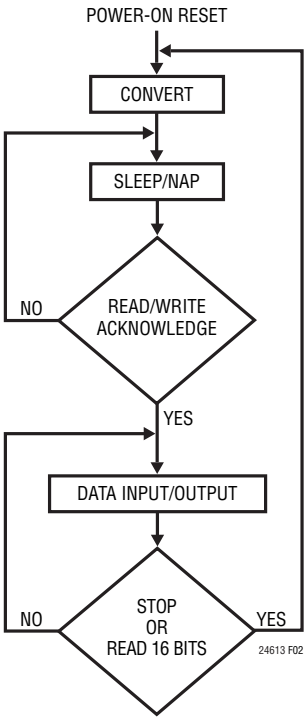


Figure 2. LTC2461/LTC2463 State Transition Diagram

While in the SLEEP/NAP state, the LTC2461/LTC2463's converters are powered down. This reduces the supply

APPLICATIONS INFORMATION

current by approximately 50%. While in the Nap state, the reference remains powered up. To power down the reference in addition to the converter, the user can select the SLEEP mode during the DATA INPUT/OUTPUT state. Once the next conversion is complete, SLEEP state is entered and power is reduced to 200nA. The reference is powered up once a valid read/write is acknowledged. The reference startup time is 12ms (if the reference and compensation capacitor values are both 0.1µF).

Power-Up Sequence

When the power supply voltage (V_{CC}) applied to the converter is below approximately 2.1V, the ADC performs a power-on reset. This feature guarantees the integrity of the conversion result.

When V_{CC} rises above this critical threshold, the converter generates an internal power-on reset (POR) signal for approximately 0.5ms. The POR signal clears all internal registers. Following the POR signal, the LTC2461/LTC2463 start a conversion cycle and follow the succession of states shown in Figure 2. The reference startup time following a POR is 12ms ($C_{COMP} = C_{REFOUT} = 0.1\mu F$). The first conversion following power-up will be invalid since the reference voltage has not completely settled. The first conversion following power up can be discarded using the data abort command or simply read and ignored. The following conversions are accurate to the device specifications.

Ease of Use

The LTC2461/LTC2463 data output has no latency, filter settling delay or redundant results associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog input voltages requires no special actions.

The LTC2461/LTC2463 perform offset calibrations every conversion cycle. This calibration is transparent to the user and has no effect upon the cyclic operation described previously. The advantage of continuous calibration is stability of the ADC performance with respect to time and temperature.

The LTC2461/LTC2463 include a proprietary input sampling scheme that reduces the average input current by several orders of magnitude when compared to traditional delta-sigma architectures. This allows external filter networks to interface directly to the LTC2461/LTC2463. Since the average input sampling current is 50nA, an external RC lowpass filter using 1kΩ and 0.1µF results in <1LSB additional error. Additionally, there is negligible leakage current between IN^+ and IN^-.

Input Voltage Range (LTC2461)

Ignoring offset and full-scale errors, the LTC2461 will theoretically output an "all zero" digital result when the input is at ground (a zero scale input) and an "all one" digital result when the input is at V_{REF} ($V_{REFOUT} = 1.25V$). In an underrange condition, for all input voltages below zero scale, the converter will generate the output code 0. In an overrange condition, for all input voltages greater than V_{REF}, the converter will generate the output code 65535. For applications that require an input range greater than 0V to 1.25V, please refer to the LTC2451.

Input Voltage Range (LTC2463)

As mentioned in the Output Data Format section, the output code is given as $32768 \bullet (V_{IN}^+ - V_{IN}^-)/V_{REF} + 32768$. For $(V_{IN}^+ - V_{IN}^-) \geq V_{REF}$, the output code is clamped at 65535 (all ones). For $(V_{IN}^+ - V_{IN}^-) \leq -V_{REF}$, the output code is clamped at 0 (all zeroes).

The LTC2463 includes a proprietary architecture that can, typically, digitize each input up to 8 LSBs above

APPLICATIONS INFORMATION

V_{REF} and below GND, if the differential input is within $\pm V_{REF}$. As an example (Figure 3), if the user desires to measure a signal slightly below ground, the user could set V_{IN}^- = GND. If V_{IN}^+ = GND, the output code would be approximately 32768. If V_{IN}^+ = GND – 8LSB = –0.305mV, the output code would be approximately 32760. For applications that require an input range greater than ±1.25V, please refer to the LTC2453.

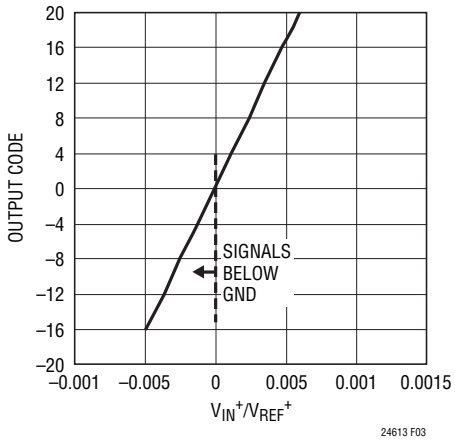


Figure 3. Output Code vs V_{IN}^+ with V_{IN}^- = 0 (LTC2463)

I²C INTERFACE

The LTC2461/LTC2463 communicate through an I²C interface. The I²C interface is a 2-wire open-drain interface supporting multiple devices and masters on a single bus. The connected devices can only pull the data line (SDA) LOW and can never drive it HIGH. SDA must be externally connected to the supply through a pull-up resistor. When the data line is free, it is HIGH. Data on the I²C bus can be transferred at rates up to 100kbits/s in the Standard-Mode and up to 400kbits/s in the Fast-Mode.

Upon entering the DATA INPUT/OUTPUT state, SDA outputs the sign (D15) of the conversion result. During this state, the ADC shifts the conversion result serially through the SDA output pin under the control of the SCL input pin. There is no latency in generating this data and the result corresponds to the last completed conversion. A new bit of data appears at the SDA pin following each falling edge detected at the SCL input pin and appears from MSB to LSB. The user can reliably latch this data on every rising edge of the external serial clock signal driving the SCL pin.

Each device on the I²C bus is recognized by a unique address stored in that device and can operate either as a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. Devices addressed by the master are considered a slave. The address of the LTC2461/LTC2463 is 0010100 (if A0 is tied to GND) or 1010100 (if A0 is tied to V_{CC}).

The LTC2461/LTC2463 can only be addressed as a slave. It can only transmit the last conversion result. The serial clock line, SCL, is always an input to the LTC2461/LTC2463 and the serial data line SDA is bidirectional. Figure 4 shows the definition of the I²C timing.

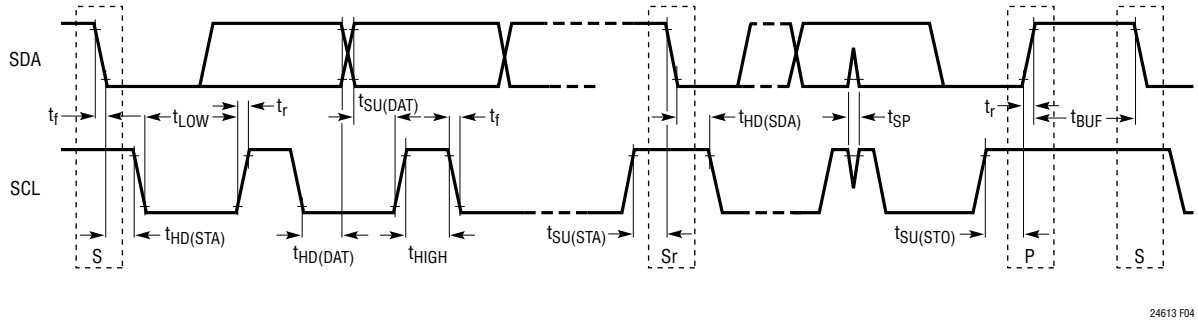


Figure 4. Definition of Timing for Fast/Standard Mode Devices on the I²C Bus

APPLICATIONS INFORMATION

The START and STOP Conditions

A START (S) condition is generated by transitioning SDA from HIGH to LOW while SCL is HIGH. The bus is considered to be busy after the START condition. When the data transfer is finished, a STOP (P) condition is generated by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus is free after a STOP is generated. START and STOP conditions are always generated by the master.

When the bus is in use, it stays busy if a repeated START (Sr) is generated instead of a STOP condition. The repeated START timing is functionally identical to the START and is used for reading from the device before the initiation of a new conversion.

Data Transferring

After the START condition, the I^2C bus is busy and data transfer can begin between the master and the addressed slave. Data is transferred over the bus in groups of nine bits, one byte followed by one acknowledge (ACK) bit. The master releases the SDA line during the ninth SCL clock cycle. The slave device can issue an ACK by pulling SDA LOW or issue a Not Acknowledge (NAK) by leaving the SDA line HIGH impedance (the external pull-up resistor will hold the line HIGH). Change of data only occurs while the clock line (SCL) is LOW.

Output Data Format

After a START condition, the master sends a 7-bit address followed by a read request (R) bit. The bit R is 1 for a Read Request. If the 7-bit address matches the LTC2461/LTC2463's address (0010100 or 1010100, depending on the state of the pin A0) the ADC is selected. When the device is addressed during the conversion state, it does not accept the request and issues a NAK by leaving the SDA line HIGH. If the conversion is complete, the LTC2461/LTC2463 issue an ACK by pulling the SDA line LOW.

Following the ACK, the LTC2461/LTC2463 can output data. The data output stream is 16 bits long and is shifted out on the falling edges of SCL (see Figure 5a).

The DATA INPUT/OUTPUT state is concluded once all 16 data bits have been read or after a STOP condition.

The LTC2463 (differential input) output code is given by $32768 \bullet (V_{IN}^+ - V_{IN}^-)/V_{REF} + 32768$. The first bit output by the LTC2463, D15, is the MSB, which is 1 for $V_{IN}^+ \geq V_{IN}^-$ and 0 for $V_{IN}^+ < V_{IN}^-$. This bit is followed by successively less significant bits (D14, D13, …) until the LSB is output by the LTC2463, see Table 1.

The LTC2461 (single-ended input) output code is a direct binary encoded result, see Table 1.

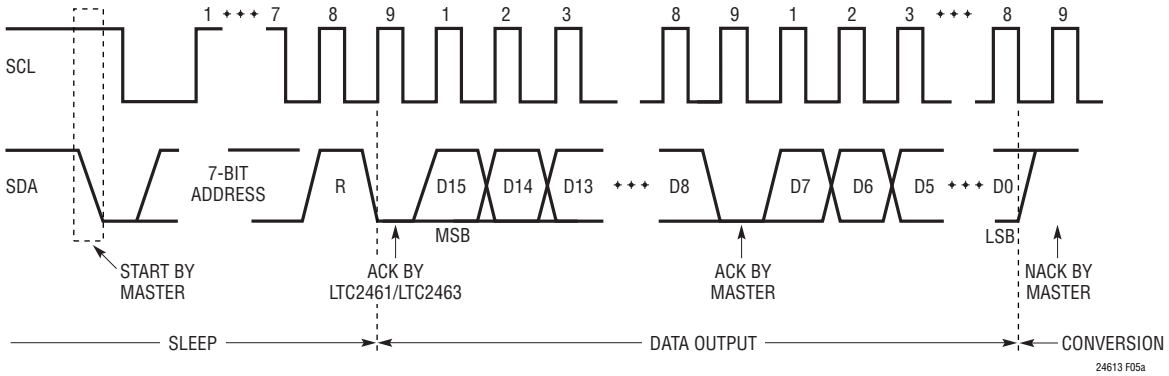


Figure 5a. Read Sequence Timing Diagram

APPLICATIONS INFORMATION

Data Input Format

After a START condition, the master sends a 7-bit address followed by a read/write request (R/$\overline{W}$) bit. The R/$\overline{W}$ bit is 0 for a write. The data input word is 4 bits long and consists of two enable bits (EN1 and EN2) and two programming bits (SPD and SLP), see Figure 5b. EN1 is applied to the first rising edge of SCL after a valid write address is acknowledged. Programming is enabled by setting EN1 = 1 and EN2 = 0.

The speed bit (SPD) is only used by the LTC2461. In the default mode, SPD = 0, the output rate is 60Hz and continuous background offset calibration is not performed. By changing the SPD bit to 1, background offset calibration is performed and the output rate is reduced to 30Hz. The LTC2463 data output rate is always 60Hz and background offset calibration is performed (SPD = don't care).

The sleep bit (SLP) is used to power down the on chip reference. In the default mode, the reference remains powered up even when the ADC is powered down. If the SLP bit is set HIGH, the reference will power down after the next conversion is complete. It will remain powered down until a valid address is acknowledged. The reference startup time is approximately 12ms. In order to ensure a stable reference for the following conversions, either the data input/output time should be delayed 12ms after an address acknowledge or the first conversion following a reference start up should be discarded.

Table 1. LTC2461/LTC2463 Output Data Format

SINGLE ENDED INPUT V_{IN} (LTC2461)	DIFFERENTIAL INPUT VOLTAGE $V_{IN}^+ - V_{IN}^-$ (LTC2463)	D15 (MSB)	D14	D13	D12…D2	D1	D0 (LSB)	CORRESPONDING DECIMAL VALUE
$\geq V_{REF}$	$\geq V_{REF}$	1	1	1	1	1	1	65535
V_{REF} – 1LSB	V_{REF} – 1LSB	1	1	1	1	1	0	65534
0.75 • V_{REF}	0.5 • V_{REF}	1	1	0	0	0	0	49152
0.75 • V_{REF} – 1LSB	0.5 • V_{REF} – 1LSB	1	0	1	1	1	1	49151
0.5 • V_{REF}	0	1	0	0	0	0	0	32768
0.5 • V_{REF} – 1LSB	–1LSB	0	1	1	1	1	1	32767
0.25 • V_{REF}	–0.5 • V_{REF}	0	1	0	0	0	0	16384
0.25 • V_{REF} – 1LSB	–0.5 • V_{REF} – 1LSB	0	0	1	1	1	1	16383
0	$\leq -V_{REF}$	0	0	0	0	0	0	0

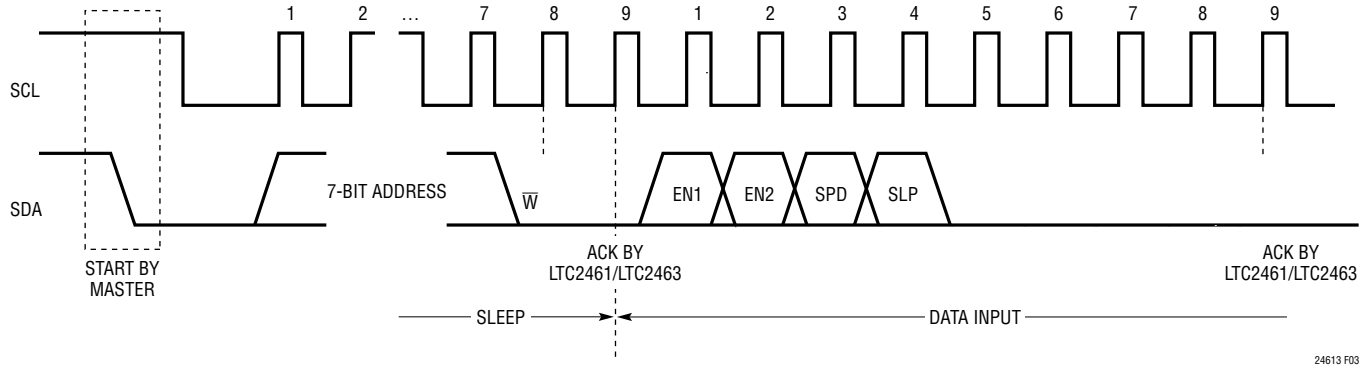


Figure 5b. Timing Diagram for Writing to the LTC2461/LTC2463

APPLICATIONS INFORMATION

OPERATION SEQUENCE

Continuous Read

Conversions from the LTC2461/LTC2463 can be continuously read, see Figure 6. The R/$\overline{W}$ is 1 for a read. At the end of a read operation, a new conversion automatically begins. At the conclusion of the conversion cycle, the next result may be read using the method described above. If the conversion cycle is not complete and a valid address selects the device, the LTC2461/LTC2463 generate a NAK signal indicating the conversion cycle is in progress. See Figure 7a for an example state diagram.

Discarding a Conversion Result and Initiating a New Conversion

It is possible to start a new conversion without reading the old result, as shown in Figure 7b. Following a valid 7-bit address, a read request (R/$\overline{W}$) bit, and a valid ACK, a STOP command will start a new conversion.

Synchronizing the LTC2461/LTC2463 with the Global Address Call

The LTC2461/LTC2463 can also be synchronized with the global address call (see Figure 7c). To achieve this, the LTC2461/LTC2463 must first have completed the

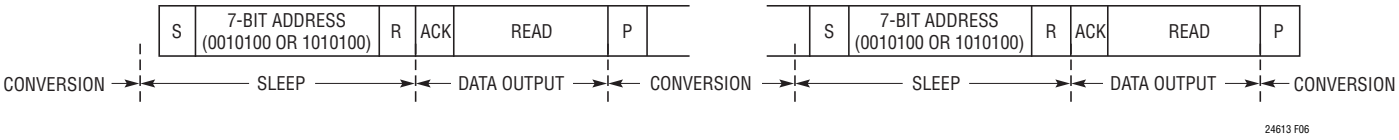


Figure 6. Consecutive Reading

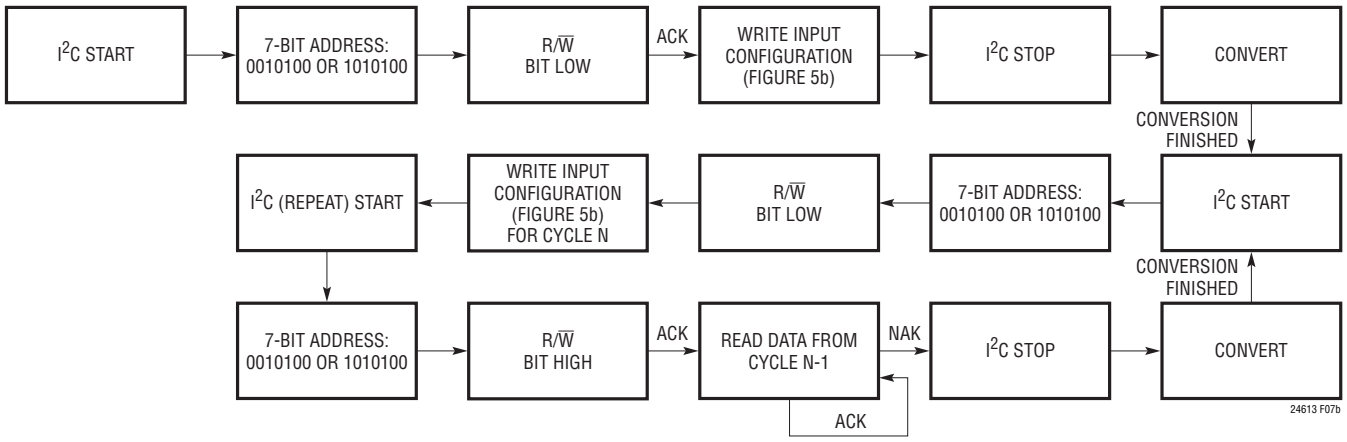


Figure 7a. I²C State Diagram

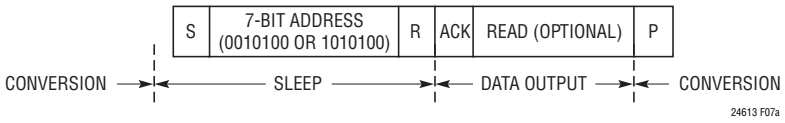


Figure 7b. Start a New Conversion without Reading Old Conversion Result

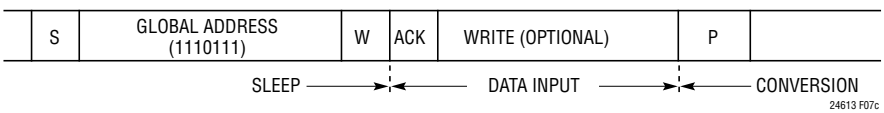


Figure 7c. Synchronize the LTC2461/LTC2463 with the Global Address Call

APPLICATIONS INFORMATION

conversion cycle. The master issues a START, followed by the LTC2461/LTC2463 global address 1110111, and a write request. The LTC2461/LTC2463 will be selected and acknowledge the request. If desired, the master then sends the write byte to program the 30Hz or 60Hz mode. After the optional write byte, the master ends the write operation with a STOP. This will update the configuration registers (if a write byte was sent) and initiate a new conversion on the LTC2461/LTC2463, as shown in Figure 7c. In order to synchronize the start of the conversion without affecting the configuration registers, the write operation can be aborted with a STOP. This initiates a new conversion on the LTC2461/LTC2463 without changing the configuration registers.

PRESERVING THE CONVERTER ACCURACY

The LTC2461/LTC2463 are designed to minimize the conversion result's sensitivity to device decoupling, PCB layout, antialiasing circuits, line and frequency perturbations. Nevertheless, in order to preserve the high accuracy capability of this part, some simple precautions are desirable.

Digital Signal Levels

Due to the nature of CMOS logic, it is advisable to keep input digital signals near GND or V_{CC}. Voltages in the range of 0.5V to V_{CC} – 0.5V may result in additional current leakage from the part. Undershoot and overshoot should also be minimized, particularly while the chip is converting. Excessive noise on the digital lines could degrade the ADC performance.

Driving V_{CC} and GND

In relation to the V_{CC} and GND pins, the LTC2461/LTC2463 combines internal high frequency decoupling with damping elements, which reduce the ADC performance sensitivity to PCB layout and external components. Nevertheless, the very high accuracy of this converter is best preserved by careful low and high frequency power supply decoupling.

A 0.1µF, high quality, ceramic capacitor in parallel with a 10µF low ESR ceramic capacitor should be connected between the V_{CC} and GND pins, as close as possible to the package. The 0.1µF capacitor should be placed closest to the ADC package. It is also desirable to avoid any via in the circuit path, starting from the converter V_{CC} pin, passing through these two decoupling capacitors, and returning to the converter GND pin. The area encompassed by this circuit path, as well as the path length, should be minimized.

As shown in Figure 8, REF^- is used as the negative reference voltage input to the ADC. This pin can be tied directly to ground or Kelvined to sensor ground. In the case where REF^- is used as a sense input, it should be bypassed to ground with a 0.1µF ceramic capacitor in parallel with a 10µF low ESR ceramic capacitor.

Very low impedance ground and power planes, and star connections at both V_{CC} and GND pins, are preferable. The V_{CC} pin should have two distinct connections: the first to the decoupling capacitors described above, and the second to the ground return for the power supply voltage source.

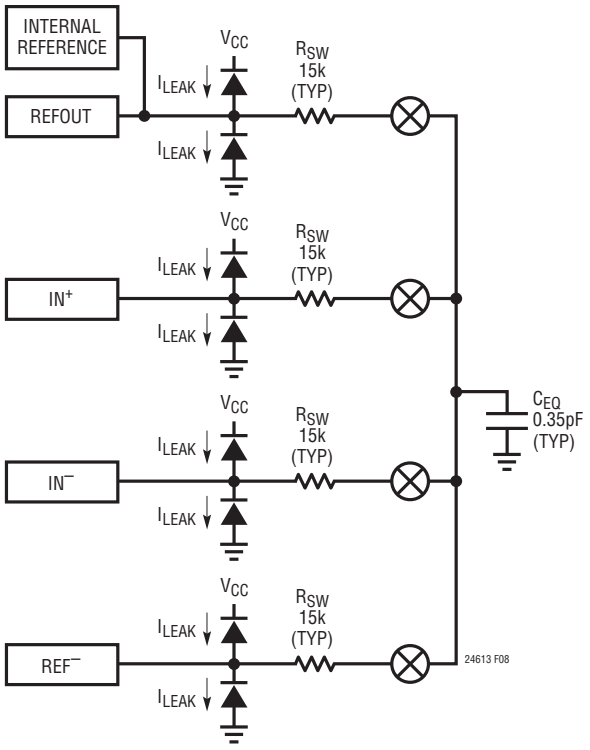


Figure 8. LTC2461/LTC2463 Analog Input/Reference Equivalent Circuit

APPLICATIONS INFORMATION

REFOUT and COMP

The on-chip 1.25V precision reference is internally tied to the LTC2461/LTC2463 converter's reference input and its output to the REFOUT pin. A 0.1µF capacitor should be placed on the REFOUT pin. It is possible to reduce this capacitor, but the transition noise increases. A 0.1µF capacitor should also be placed on the COMP pin. This pin is tied to an internal point in the reference and is used for stability. In order for the reference to remain stable the capacitor placed on the COMP pin must be greater than or equal to the capacitor tied to the REFOUT pin. The REFOUT pin should not be overridden by an external voltage. If a reference voltage greater than 1.25V is required, the LTC2451/LTC2453 should be used.

The internal reference has a corresponding start up time depending on the size of the capacitors tied to the REFOUT and COMP pins. This start up time is typically 12ms when 0.1µF capacitors are used. At initial power up, the first conversion result can be aborted or ignored. At the completion of this first conversion, the reference has settled and all subsequent conversions are valid.

If the reference is put to sleep (program SLP = 1) the reference is powered down after the next conversion. This last conversion result is valid. On a valid address acknowledge, the reference is powered back up. In order to ensure the reference output has settled before the next conversion, the power up time can be extended by delaying the data read 12ms. Once all 16 bits are read from the device, the next conversion automatically begins. In the default operation, the reference remains powered up at the conclusion of the conversion cycle.

Driving V_{IN}^+ and V_{IN}^-

The input drive requirements can best be analyzed using the equivalent circuit of Figure 9. The input signal V_{SIG} is connected to the ADC input pins (IN^+ and IN^-) through an equivalent source resistance R_S. This resistor includes both the actual generator source resistance and any additional optional resistors connected to the input pins. Optional input capacitors C_{IN} are also connected to the ADC input pins. This capacitor is placed in parallel with the input parasitic capacitance C_{PAR}. This parasitic capacitance

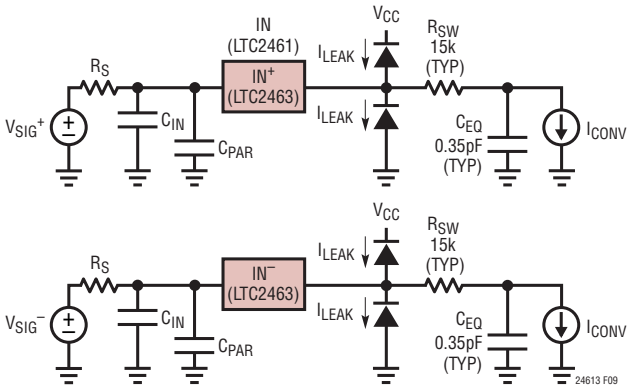


Figure 9. LTC2461/LTC2463 Input Drive Equivalent Circuit

includes elements from the printed circuit board (PCB) and the associated input pin of the ADC. Depending on the PCB layout, C_{PAR} has typical values between 2pF and 15pF. In addition, the equivalent circuit of Figure 9 includes the converter equivalent internal resistor R_{SW} and sampling capacitor C_{EQ}.

There are some immediate trade-offs in R_S and C_{IN} without needing a full circuit analysis. Increasing R_S and C_{IN} can give the following benefits:

1) Due to the LTC2461/LTC2463's input sampling algorithm, the input current drawn by IN^+, IN^- or IN over a conversion cycle is typically 50nA. A high $R_S \bullet C_{IN}$ attenuates the high frequency components of the input current, and R_S values up to 1k result in <1LSB error.
2) The bandwidth from V_{SIG} is reduced at the input pins (IN^+, IN^- or IN). This bandwidth reduction isolates the ADC from high frequency signals, and as such provides simple antialiasing and input noise reduction.
3) Switching transients generated by the ADC are attenuated before they go back to the signal source.
4) A large C_{IN} gives a better AC ground at the input pins, helping reduce reflections back to the signal source.
5) Increasing R_S protects the ADC by limiting the current during an outside-the-rails fault condition.

There is a limit to how large $R_S \bullet C_{IN}$ should be for a given application. Increasing R_S beyond a given point increases the voltage drop across R_S due to the input current,

APPLICATIONS INFORMATION

to the point that significant measurement errors exist. Additionally, for some applications, increasing the $R_S \bullet C_{IN}$ product too much may unacceptably attenuate the signal at frequencies of interest.

For most applications, it is desirable to implement C_{IN} as a high-quality 0.1µF ceramic capacitor and to set $R_S \leq 1k$. This capacitor should be located as close as possible to the actual IN^+, IN^- or IN package pin. Furthermore, the area encompassed by this circuit path, as well as the path length, should be minimized.

In the case of a 2-wire sensor that is not remotely grounded, it is desirable to split R_S and place series resistors in the ADC input line as well as in the sensor ground return line, which should be tied to the ADC GND pin using a star connection topology.

Figure 10 shows the measured LTC2463 INL vs Input Voltage as a function of R_S value with an input capacitor $C_{IN} = 0.1\mu F$.

In some cases, R_S can be increased above these guidelines. The input current is zero when the ADC is either in sleep or I/O modes. Thus, if the time constant of the input RC circuit $\tau = R_S \bullet C_{IN}$, is of the same order of magnitude or longer than the time periods between actual conversions, then one can consider the input current to be reduced correspondingly.

These considerations need to be balanced out by the input signal bandwidth. The 3dB bandwidth $\approx 1/(2\pi R_S C_{IN})$.

Finally, if the recommended choice for C_{IN} is unacceptable for the user's specific application, an alternate strategy is to eliminate C_{IN} and minimize C_{PAR} and R_S. In practical terms, this configuration corresponds to a low impedance sensor directly connected to the ADC through minimum length traces. Actual applications include current measurements through low value sense resistors, temperature measurements, low impedance voltage source monitoring, and so on. The resultant INL vs V_{IN} is shown in Figure 11. The measurements of Figure 11 include a capacitor C_{PAR} corresponding to a minimum sized layout pad and a minimum width input trace of about 1 inch length.

Signal Bandwidth, Transition Noise and Noise Equivalent Input Bandwidth

The LTC2461/LTC2463 include a $sinc^1$ type digital filter with the first notch located at f_0 = 60Hz. As such, the 3dB input signal bandwidth is 26.54Hz. The calculated LTC2461/LTC2463 input signal attenuation vs frequency over a wide frequency range is shown in Figure 12. The calculated LTC2461/LTC2463 input signal attenuation vs frequency at low frequencies is shown in Figure 13. The converter noise level is about $2.2\mu V_{RMS}$ and can be modeled by a white noise source connected at the input of a noise-free converter.

On a related note, the LTC2463 uses two separate A/D converters to digitize the positive and negative inputs. Each of these A/D converters has $2.2\mu V_{RMS}$ transition noise. If one of the input voltages is within this small transition noise band, then the output will fluctuate one bit, regardless of the value of the other input voltage. If both of the input voltages are within their transition noise bands, the output can fluctuate 2 bits.

For a simple system noise analysis, the V_{IN} drive circuit can be modeled as a single-pole equivalent circuit characterized by a pole location f_i and a noise spectral density n_i. If the converter has an unlimited bandwidth, or at least a bandwidth substantially larger than f_i, then the total noise contribution of the external drive circuit would be:

$$V_n = n_i \sqrt{\pi / 2 \bullet f_i}$$

Then, the total system noise level can be estimated as the square root of the sum of (V_n^2) and the square of the LTC2461/LTC2463 noise floor (~$2.2\mu V^2$).

APPLICATIONS INFORMATION

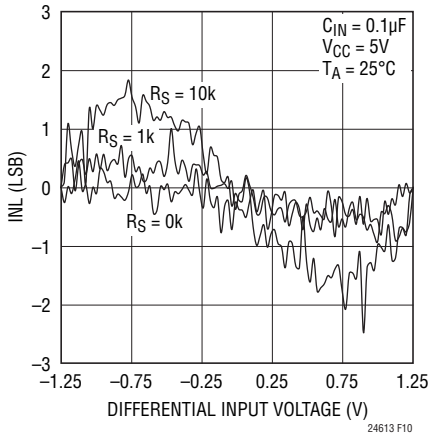


Figure 10. Measured INL vs Input Voltage (C_{IN} = 0.1µF)

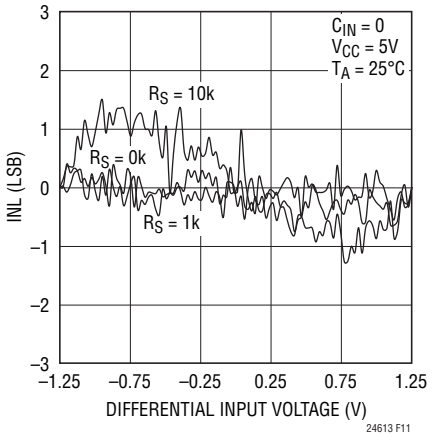


Figure 11. Measured INL vs Input Voltage (C_{IN} = 0)

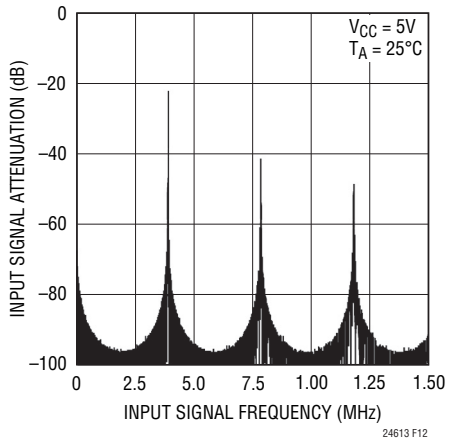


Figure 12. LTC2463 Input Signal Attentuation vs Frequency

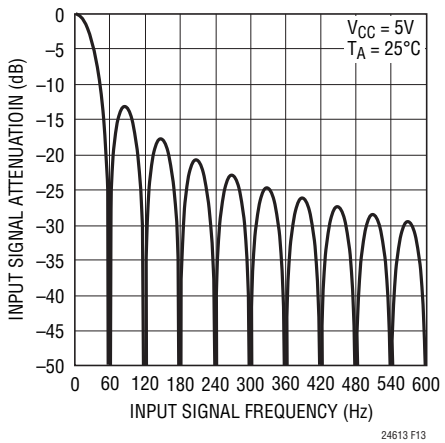
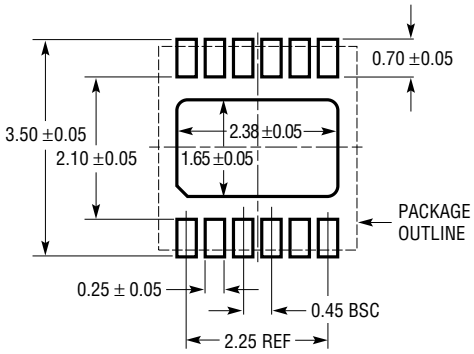


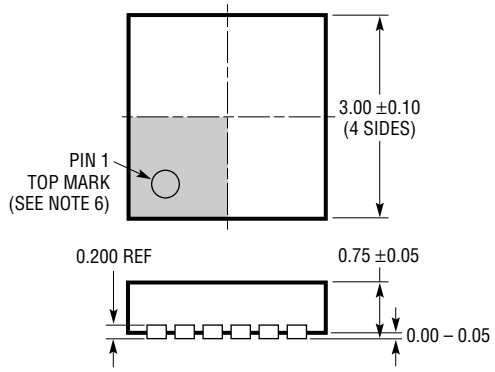
Figure 13. LTC2463 Input Signal Attenuation vs Frequency (Low Frequencies)

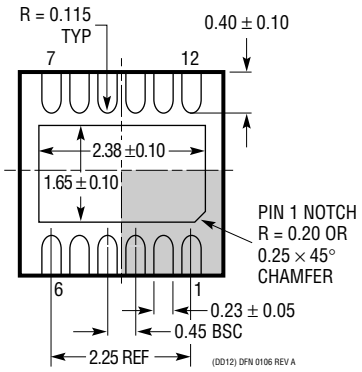
PACKAGE DESCRIPTION

DD Package
12-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1725 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



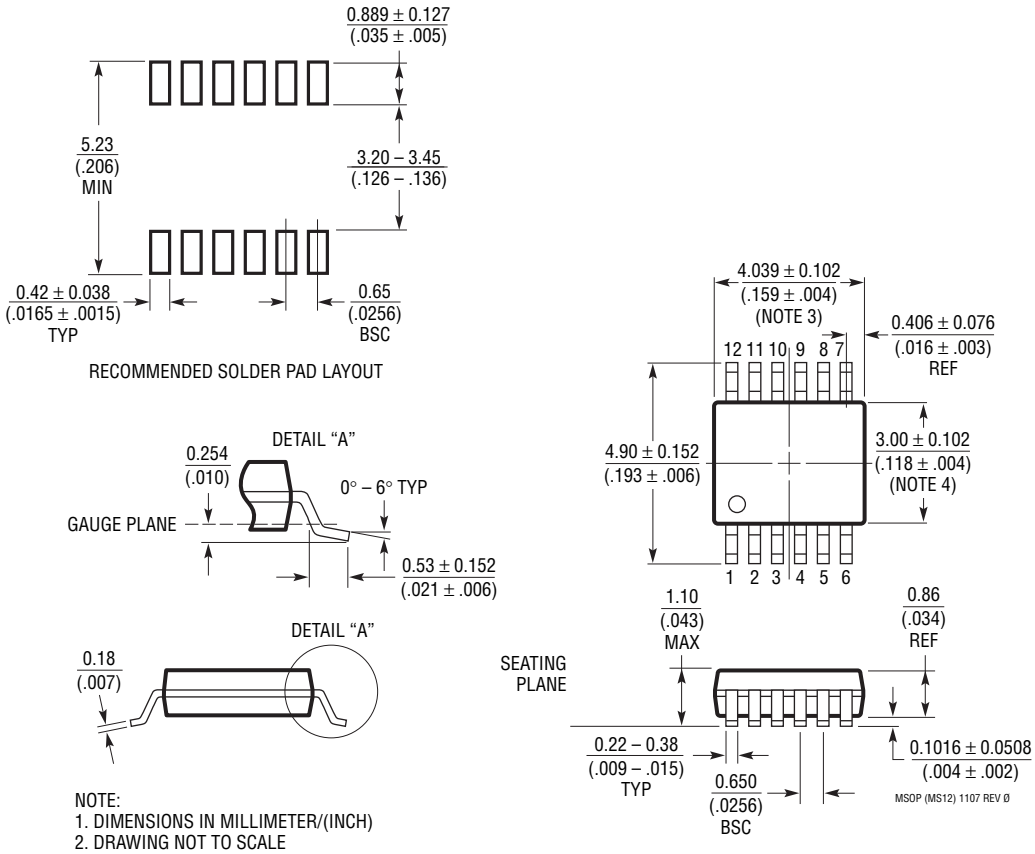


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD AND TIE BARS SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS Package
12-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1668 Rev Ø)

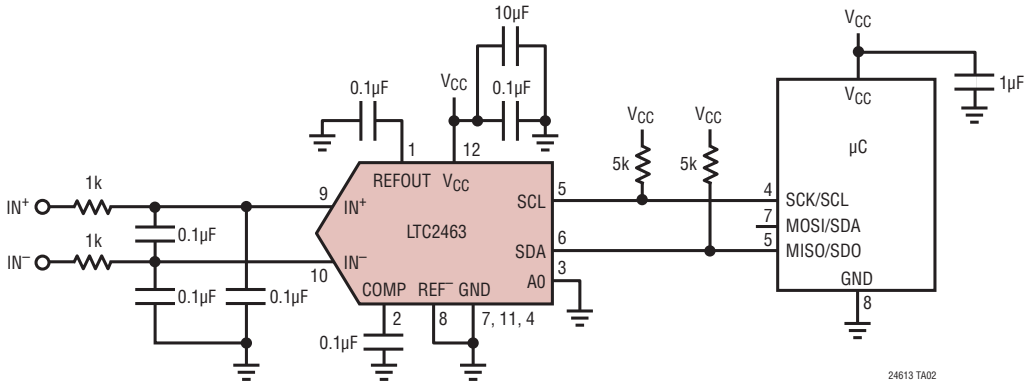


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	5/11	Added “Synchronizing the LTC2461/LTC2463 with the Global Address Call” to the Applications Information section	12-13

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1860/LTC1861	12-Bit, 5V, 1-/2-Channel 250ksps SAR ADC in MSOP	850µA at 250ksps, 2µA at 1ksps, SO-8 and MSOP Packages
LTC1860L/LTC1861L	12-Bit, 3V, 1-/2-Channel 150ksps SAR ADC	450µA at 150ksps, 10µA at 1ksps, SO-8 and MSOP Packages
LTC1864/LTC1865	16-Bit, 5V, 1-/2-Channel 250ksps SAR ADC in MSOP	850µA at 250ksps, 2µA at 1ksps, SO-8 and MSOP Packages
LTC1864L/LTC1865L	16-bit, 3V, 1-/2-Channel 150ksps SAR ADC	450µA at 150ksps, 10µA at 1ksps, SO-8 and MSOP Packages
LTC2360	12-Bit, 100ksps SAR ADC	3V Supply, 1.5mW at 100ksps, TSOT 6-pin/8-pin Packages
LTC2440	24-Bit No Latency ΔΣ™ ADC	200nV$_{RMS}$ Noise, 4kHz Output Rate, 15ppm INL
LTC2480	16-Bit, Differential Input, No Latency ΔΣ ADC, with PGA, Temp. Sensor, SPI	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2481	16-Bit, Differential Input, No Latency ΔΣ ADC, with PGA, Temp. Sensor, I^{2}C	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2482	16-Bit, Differential Input, No Latency ΔΣ ADC, SPI	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2483	16-Bit, Differential Input, No Latency ΔΣ ADC, I^{2}C	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2484	24-Bit, Differential Input, No Latency ΔΣ ADC, SPI with Temp. Sensor	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC2485	24-Bit, Differential Input, No Latency ΔΣ ADC, I^{2}C with Temp. Sensor	Easy-Drive Input Current Cancellation, 600nV$_{RMS}$ Noise, Tiny 10-Lead DFN Package
LTC6241	Dual, 18MHz, Low Noise, Rail-to-Rail Op Amp	550nV$_{P-P}$ Noise, 125µV Offset Max
LTC2450	Easy-to-Use, Ultra-Tiny 16-Bit ADC, SPI, 0V to 5.5V Input Range	2 LSB INL, 50nA Sleep current, Tiny 2mm × 2mm DFN-6 Package, 30Hz Output Rate
LTC2450-1	Easy-to-Use, Ultra-Tiny 16-Bit ADC, SPI, 0V to 5.5V Input Range	2 LSB INL, 50nA Sleep Current, Tiny 2mm × 2mm DFN-6 Package, 60Hz Output Rate
LTC2451	Easy-to-Use, Ultra-Tiny 16-Bit ADC, I^{2}C, 0V to 5.5V Input Range	2 LSB INL, 50nA Sleep Current, Tiny 3mm × 2mm DFN-8 or TSOT Package, Programmable 30Hz/60Hz Output Rates
LTC2452	Easy-to-Use, Ultra-Tiny 16-Bit Differential ADC, SPI, ±5.5V Input Range	2 LSB INL, 50nA Sleep Current, Tiny 3mm × 2mm DFN-8 or TSOT Package
LTC2453	Easy-to-Use, Ultra-Tiny 16-Bit Differential ADC, I^{2}C, ±5.5V Input Range	2 LSB INL, 50nA Sleep Current, Tiny 3mm × 2mm DFN-8 or TSOT Package
LTC2460	16-Bit, ΔΣ SPI ADC with 10ppm Max Reference	Single-Ended, Tiny 12-Lead 3mm × 3mm DFN and MSOP Packages
LTC2462	16-Bit, ΔΣ SPI ADC with 10ppm Max Reference	Differential Input, Tiny 12-Lead 3mm × 3mm DFN and MSOP Packages

No Latency ΔΣ is a trademark of Linear Technology Corporation.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0511 REV A • PRINTED IN USA