ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 18V
Input Voltage at Any Pin .... $-0.3V \leq V_{IN} \leq V^+ + 0.3V$
Operating Temperature Range
    LTC1043C .... $-40°C \leq T_A \leq 85°C$
    LTC1043M **(OBSOLETE)**.............$-55°C \leq T_A \leq 125°C$
Storage Temperature Range .... $-65°C$ to $150°C$
Lead Temperature (Soldering, 10 sec)................. $300°C$

PACKAGE/ORDER INFORMATION

TOP VIEW

Pin	Name		Pin	Name
1	SH$_B$		18	S3B
2	C$_B$$^+$		17	V$^-$
3	C$_B$$^-$		16	C$_{OSC}$
4	V$^+$		15	S4B
5	S2B		14	S4A
6	S1B		13	S3A
7	S1A		12	C$_A$$^-$
8	S2A		11	C$_A$$^+$
9	NC		10	SH$_A$

N PACKAGE
18-LEAD PDIP

SW PACKAGE
18-LEAD PLASTIC SO

$T_{JMAX} = 100°C$, $\theta_{JA} = 100°C/W$ PACKAGE (N)
$T_{JMAX} = 150°C$, $\theta_{JA} = 85°C/W$ PACKAGE (SW)

	ORDER PART NUMBER
	LTC1043CN LTC1043CSW
D PACKAGE 18-LEAD SIDE BRAZED (HERMETIC) **OBSOLETE PACKAGE** Consider the N18 Package as an Alternate Source	LTC1043MD

LTC1043 • POI01

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $V^+ = 10V$, $V^- = 0V$, LTC1043M operates from $-55°C \leq T_A \leq 125°C$; LTC1043C operates from $-40°C \leq T_A \leq 85°C$, unless otherwise noted.

| SYMBOL	PARAMETER	CONDITIONS		LTC1043M MIN	TYP	MAX	LTC1043C MIN	TYP	MAX	UNITS
I$_S$	Power Supply Current	Pin 16 Connected High or Low	●		0.25	0.4 0.7		0.25	0.4 0.7	mA mA
		C$_{OSC}$ (Pin 16 to V$^-$) = 100pF	●		0.4	0.65 1		0.4	0.65 1	mA mA
I$_I$	OFF Leakage Current	Any Switch, Test Circuit 1 (Note 2)	●		6 6	100 500		6 6	100	pA nA
R$_{ON}$	ON Resistance	Test Circuit 2, V$_{IN}$ = 7V, 1 = ±0.5mA V$^+$ = 10V, V$^-$ = 0V	●		240	400 700		240	400 700	Ω Ω
R$_{ON}$	ON Resistance	Test Circuit 2, V$_{IN}$ = 3.1V, 1 = ±0.5mA V$^+$ = 5V, V$^-$ = 0V	●		400	700 1		400	700 1	Ω kΩ
f$_{OSC}$	Internal Oscillator Frequency	C$_{OSC}$ (Pin 16 to V$^-$) = 0pF C$_{OSC}$ (Pin 16 to V$^-$) = 100pF Test Circuit 3	●	20 15	185 34	50 75	20 15	185 34	50 75	kHz kHz kHz
I$_{OSC}$	Pin Source or Sink Current	Pin 16 at V$^+$ or V$^-$	●		40	70 100		40	70 100	µA µA
	Break-Before-Make Time				25			25		ns
	Clock to Switching Delay	C$_{OSC}$ Pin Externally Driven			75			75		ns
f$_M$	Max External CLK Frequency	C$_{OSC}$ Pin Externally Driven with CMOS Levels			5			5		MHz
CMRR	Common Mode Rejection Ratio	V$^+$ = 5V, V$^-$ = $-5V$, $-5V < V_{CM} < 5V$ DC to 400Hz			120			120		dB

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

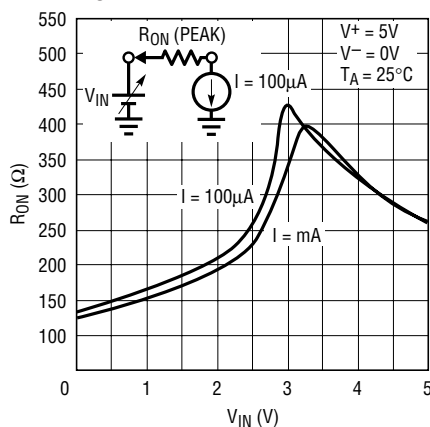**Note 2:** OFF leakage current is guaranteed but not tested at 25°C.

1043fa

2

LINEAR TECHNOLOGY

TYPICAL PERFORMANCE CHARACTERISTICS (Test Circuits 2 through 4)

Power Supply Current vs Power Supply Voltage
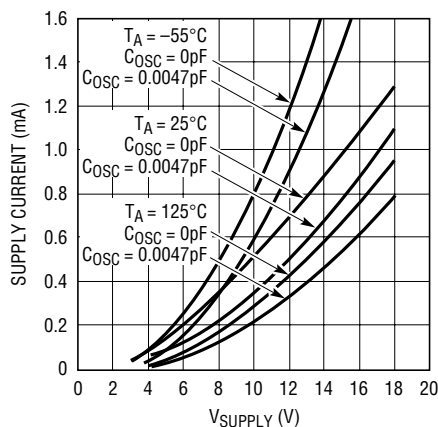
LTC1043 • TPC01
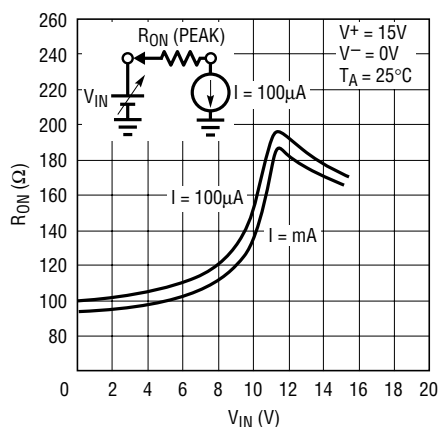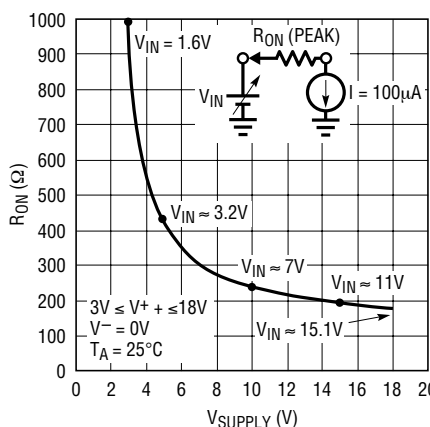
R_{ON} vs V_{IN}

LTC1043 • TPC02

R_{ON} vs V_{IN}
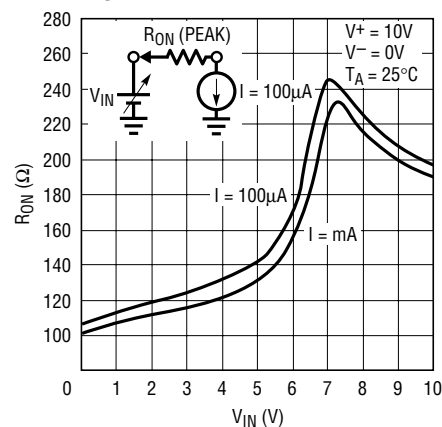
LTC1043 • TPC03
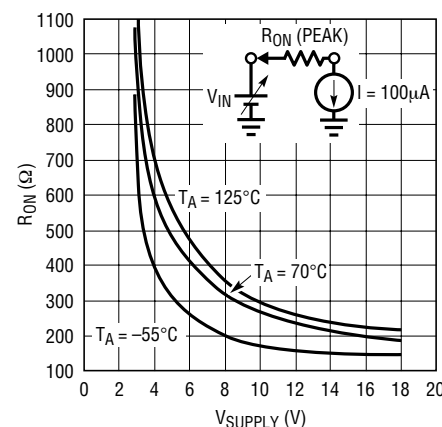
R_{ON} vs V_{IN}

LTC1043 • TPC04

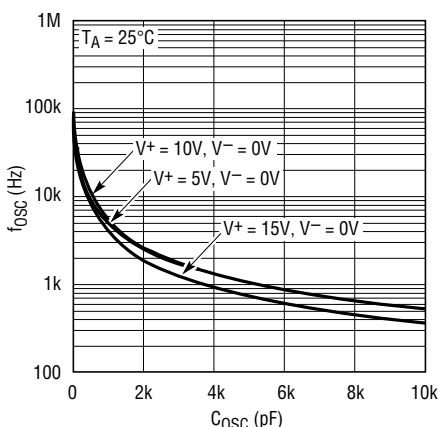**R_{ON} (Peak) vs Power Supply Voltage**

LTC1043 • TPC05

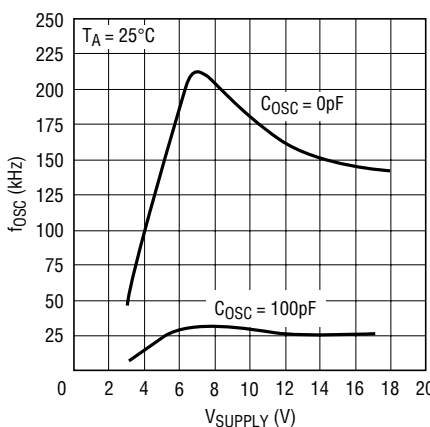**R_{ON} (Peak) vs Power Supply Voltage and Temperature**

LTC1043 • TPC06
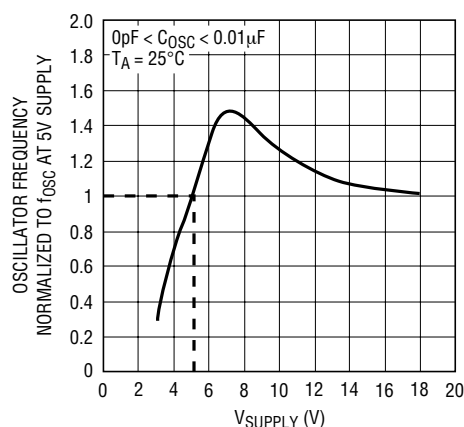
Oscillator Frequency, f_{OSC} vs C_{OSC}

LTC1043 • TPC07

Oscillator Frequency, f_{OSC} vs Supply Voltage
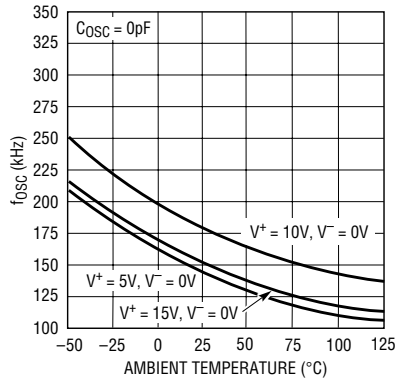

LTC1043 • TPC08

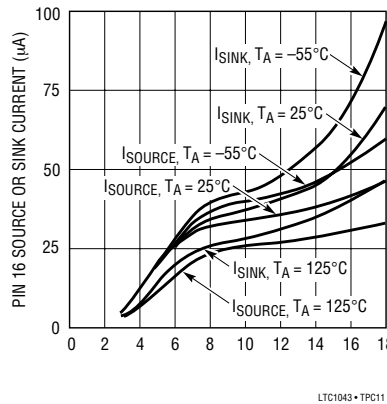**Normalized Oscillator Frequency, f_{OSC} vs Supply Voltage**

LTC1043 • TPC09

1043fa

3

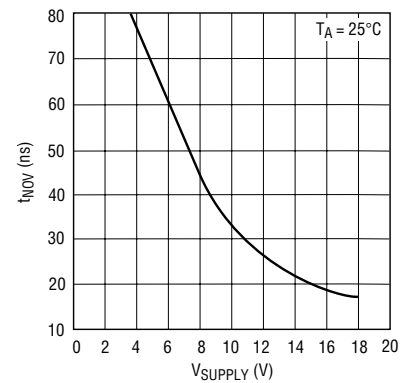# TYPICAL PERFORMANCE CHARACTERISTICS (Test Circuits 2 through 4)

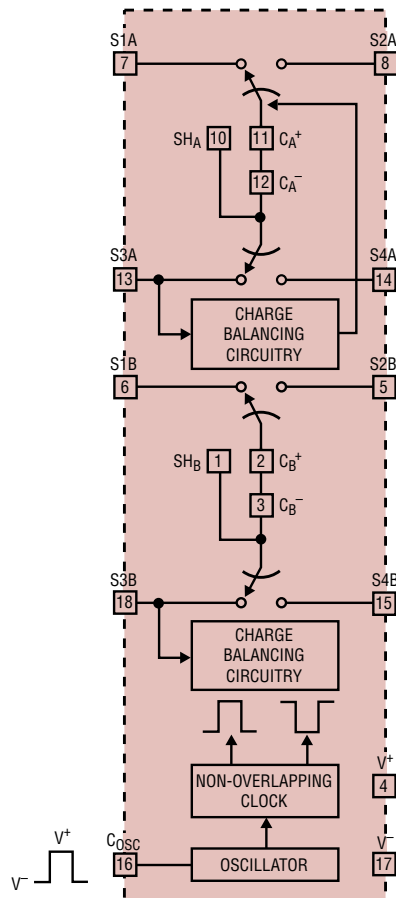**Oscillator Frequency, f_{OSC} vs Ambient Temperature, T_A**

LTC1043 • TPC10

C_{OSC} Pin I_{SINK}, I_{SOURCE} vs Supply Voltage

LTC1043 • TPC11

Break-Before-Make Time, t_{NOV}, vs Supply Voltage

LTC1043 • TPC12

BLOCK DIAGRAM

THE CHARGE BALANCING CIRCUITRY SAMPLES THE VOLTAGE AT S3 WITH RESPECT TO S4 (PIN 16 HIGH) AND INJECTS A SMALL CHARGE AT THE C^+ PIN (PIN 16 LOW). THIS BOOSTS THE CMRR WHEN THE LTC1043 IS USED AS AN INSTRUMENTATION AMPLIFIER FRONT END. FOR MINIMUM CHARGE INJECTION IN OTHER TYPES OF APPLICATIONS, S3A AND S3B SHOULD BE GROUNDED
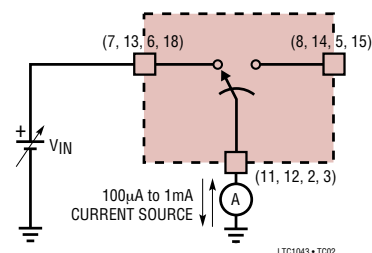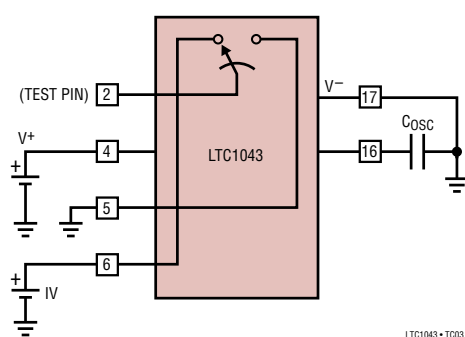
THE SWITCHES ARE TIMED AS SHOWN WITH PIN 16 HIGH

LTC1043 • BD01

1043fa

4

TEST CIRCUITS

Test Circuit 1. Leakage Current Test

(7, 13, 6, 18)   (8, 14, 5, 15)

A

0V TO 10V

(11, 12, 2, 3)

NOTE: TO OPEN SWITCHES,
S1 AND S3
SHOULD BE CONNECTED
TO V⁻. TO OPEN S2, S4,
C_{OSC} PIN SHOULD BE
TO V⁺ C_{OSC}

LTC1043 • TC01

Test Circuit 2. R$_{ON}$ Test

(7, 13, 6, 18)   (8, 14, 5, 15)

V_{IN}

(11, 12, 2, 3)

100µA to 1mA
CURRENT SOURCE

A

LTC1043 • TC02
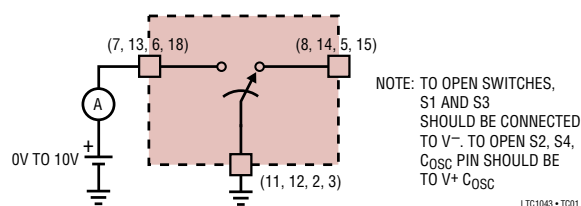
Test Circuit 3. Oscillator Frequency, f$_{OSC}$

(TEST PIN) 2

V⁺ 4

5

6

LTC1043

V⁻ 17

16 C_{OSC}

IV

LTC1043 • TC03

Test Circuit 4. CMRR Test

7   8 V_{OUT}

10   11

1µF

12

1µF   CAPACITORS ARE
NOT ELECTROLYTIC

13   14

V⁻ ≤ V_{CM} ≤ V⁺

$$CMRR = 20 \; LOG \left(\frac{V_{CM}}{V_{OUT}} \right)$$

NOTE: FOR OPTIMUM CMRR, THE C$_{OSC}$ SHOULD
BE LARGER THAN 0.0047µF, AND
THE SAMPLING CAPACITOR ACROSS
PINS 11 AND 12 SHOULD BE PLACED
OVER A SHIELD TIED TO PIN 10

LTC1043 • TC04
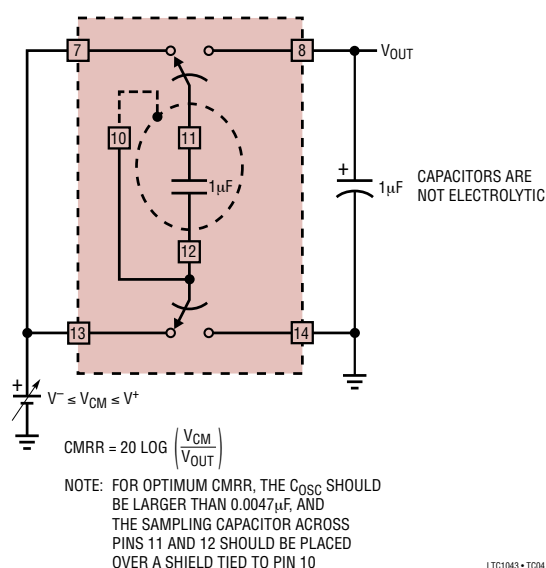
APPLICATIONS INFORMATION

Common Mode Rejection Ratio (CMRR)

The LTC1043, when used as a differential to single-ended converter rejects common mode signals and preserves differential voltages (Figure 1). Unlike other techniques, the LTC1043's CMRR does not degrade with increasing common mode voltage frequency. During the sampling mode, the impedance of Pins 2, 3 (and 11, 12) should be reasonably balanced, otherwise, common mode signals will appear differentially. The value of the CMRR depends on the value of the sampling and holding capacitors (C_S, C_H) and on the sampling frequency. Since the common mode voltages are not sampled, the common mode signal frequency can well exceed the sampling frequency without experiencing aliasing phenomena. The CMRR of Figure 1 is measured by
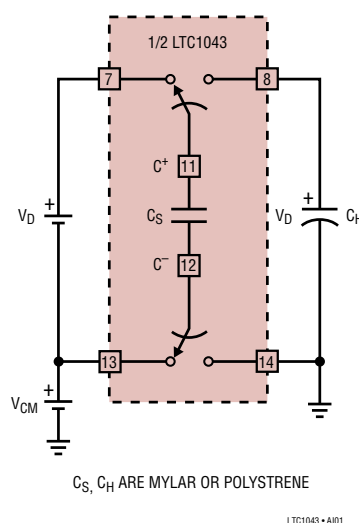
1/2 LTC1043

7   8

C^+ 11

V_D C_S V_D C_H

C^- 12

13   14

V_{CM}

C_S, C_H ARE MYLAR OR POLYSTRENE

LTC1043 • AI01

Figure 1. Differential to Single-Ended Converter

APPLICATIONS INFORMATION

shorting Pins 7 and 13 and by observing, with a precision DVM, the change of the voltage across C_H with respect to an input CM voltage variation. During the sampling and holding mode, charges are being transferred and minute voltage transients will appear across the holding capacitor. Although the R_{ON} on the switches is low enough to allow fast settling, as the sampling frequency increases, the rate of charge transfer increases and the average voltage measured with a DVM across it will increase proportionally; this causes the CMRR of the sampled data system, as seen by a "continuous" instrument (DVM), to decrease (Figure 2).

Switch Charge Injection

Figure 3 shows one out of the eight switches of the LTC1043, configured as a basic sample-and-hold circuit. When the switch opens, a "hold step" is observed and its magnitude depends on the value of the input voltage. Figure 4 shows charge injected into the hold capacitor. For instance, a 2pCb of charge injected into a 0.01μF capacitor causes a 200μV hold step. As shown in Figure 4, there is a predictable and repeatable charge injection cancellation when the input voltage is close to half the supply voltage of the LTC1043. This is a unique feature of this product, containing charge-balanced switches fabricated with a self-aligning gate CMOS process. Any switch of the LTC1043, when powered with symmetrical dual supplies, will sample-and-hold small signals around ground without any significant error.
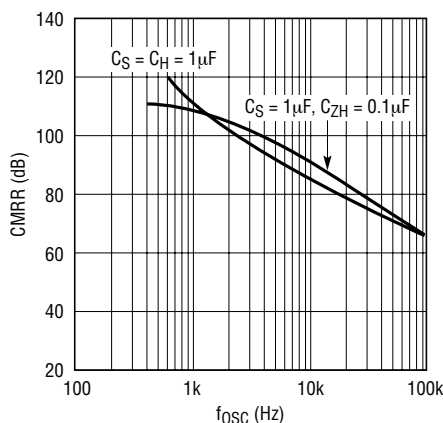
Shielding the Sampling Capacitor for Very High CMRR

Internal or external parasitic capacitors from the C^+ pin(s) to ground affect the CMRR of the LTC1043 (Figure 1). The common mode error due to the internal junction capacitances of the C^+ Pin(s) 2 and 11 is cancelled through internal circuitry. The C^+ pin, therefore, should be used as the top plate of the sampling capacitor. The interpin capacitance between pin 2 and dummy Pin 1 (11 and 10) appears in parallel with the sampling capacitor so it does not degrade the CMRR. A shield placed underneath the sampling capacitor and connected to either Pin 1 or 3 helps to boost the CMRR in excess of 120dB (Figure 5).

Excessive external parasitic capacitance between the C^- pins and ground indirectly degrades CMRR; this becomes visible especially when the LTC1043 is used with clock frequencies above 2kHz. Because of this, if a shield is used, the parasitic capacitance between the shield and circuit ground should be minimized.

It is recommended that the outer plate of the sampling capacitor be connected to the C^- pin(s).

Input Pins, SCR Sensitivity

An internal 60Ω resistor is connected in series with the input of the switches (Pins 5, 6, 7, 8, 13, 14, 15, 18) and it is included in the R_{ON} specification. When the input voltage exceeds the power supply by a diode drop, current will flow into the input pin(s). The LTC1043 will not latch until the input current reaches 2mA–3mA. The device will
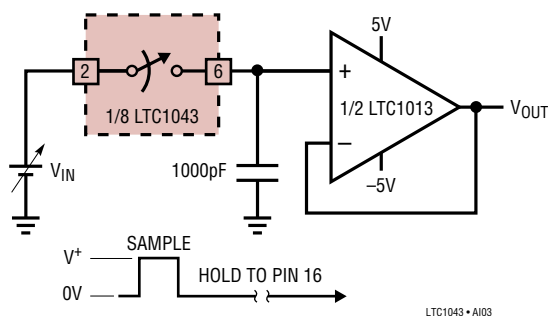

Figure 2. CMRR vs Sampling Frequency

Figure 3

1043fa

6

APPLICATIONS INFORMATION

recover from the latch mode when the input drops 3V to 4V below the voltage value which caused the latch. For instance, if an external resistor of 200Ω is connected in series with an input pin, the input can be taken 1.3V above the supply without latching the IC. The same applies for the C^+ and C^- pins.

C_{OSC} Pin (16), Figure 6

The Cosc pin can be used with an external capacitor, Cosc, connected from Pin 16 to Pin 17, to modify the internal oscillator frequency. If Pin 16 is floating, the internal 24pF capacitor, plus any external interpin capacitance, set the oscillator frequency around 190kHz with ±5V supply. The typical performance characteristics curves provide the necessary information to set the oscillator frequency for various power supply ranges. Pin 16 can also be driven with an external clock to override the internal oscillator. Although standard 7400 series CMOS gates do not guarantee CMOS levels with the current source and sink requirements of Pin 16, they will in reality drive the Cosc pin. CMOS gates conforming to standard B series output drive have the appropriate voltage levels and more than enough output current to simultaneously drive several LTC1043 C_{OSC} pins. The typical trip levels of the Schmitt trigger (Figure 6) are given below.

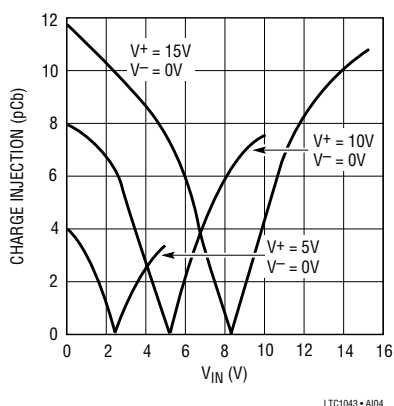| SUPPLY	TRIP LEVELS
$V^+ = 5V$, $V^- = 0V$	$V_H = 3.4V$ $V_L = 1.35V$
$V^+ = 10V$, $V^- = 0V$	$V_H = 6.5V$ $V_L = 2.8V$
$V^+ = 15V$, $V^- = 0V$	$V_H = 9.5V$ $V_L = 4.1V$

Figure 4. Individual Switch Charge Injection vs Input Voltage

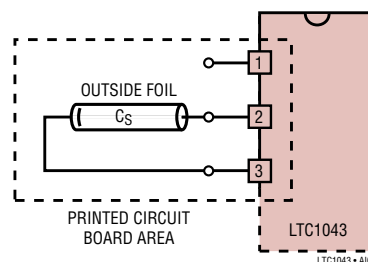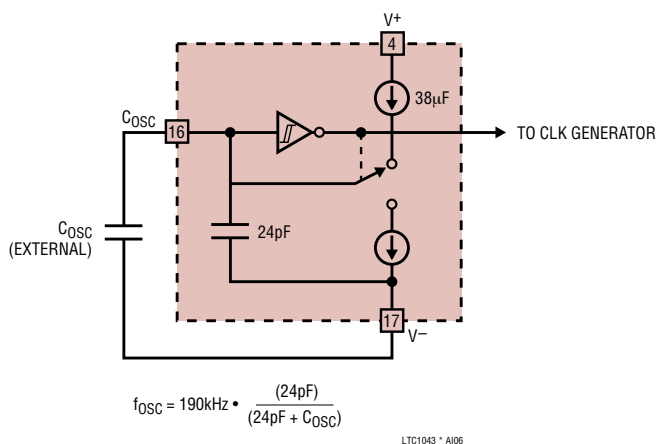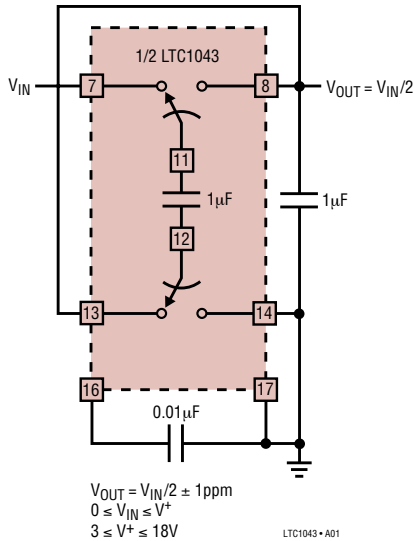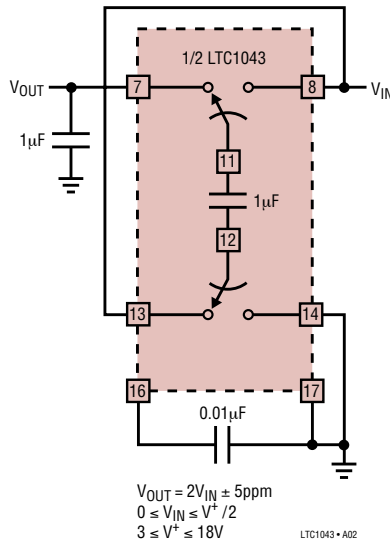**Figure 5. Printed Circuit Board Layout Showing Shielding the Sampling Capacitor**

$$f_{OSC} = 190kHz \cdot \frac{(24pF)}{(24pF + C_{OSC})}$$

Figure 6. Internal Oscillator

1043fa

LTC1043

TYPICAL APPLICATIONS

Divide by 2

$V_{OUT} = V_{IN}/2 \pm 1ppm$
$0 \leq V_{IN} \leq V^+$
$3 \leq V^+ \leq 18V$

LTC1043 • A01

Multiply by 2

$V_{OUT} = 2V_{IN} \pm 5ppm$
$0 \leq V_{IN} \leq V^+/2$
$3 \leq V^+ \leq 18V$

LTC1043 • A02

Ultra Precision Voltage Inverter

$V_{OUT} = -V_{IN} \pm 2ppm$
$V^- < V_{IN} < V^+$
$V^+ = +5V, V^- = -5V$

LTC1043 * A03

Precision Multiply by 3

$V_{OUT} = 3V_{IN} \pm 10ppm$
$0 < V_{IN} < V^+/3$
$3V < V^+ < 18V$

LTC1043 • A04

Precision Multiply by 4

$V_{OUT} = 4V_{IN} \pm 40ppm$
$0 \leq V_{IN} \leq V^+/4$
$3V < V^+ < 18V$

LTC1043 • A05

Divide by 3

$V_{OUT} = V_{IN}/3 \pm 3ppm$
$0 \leq V_{IN} \leq V^+$

LTC1043 • A06

1043fa

8

LINEAR TECHNOLOGY

TYPICAL APPLICATIONS

Divide by 4

$0 \le V_{IN} \le V^+$
$V_{OUT} = V_{IN}/4 \pm 5ppm$

LTC1043 • A07

0.005% V/F Converter

f_{OUT}: 0kHz TO 30kHz

LTC1043 • A08

0.01% Analog Multiplier

OPERATE LTC1043 FROM ±5V
† POLYSTYRENE, MOUNT CLOSE
*1% FILM RESISTOR
  ADJUST OUTPUT TRIM
  SO X • Y = OUTPUT ±0.01%

OUTPUT
XY ±0.01%

LTC1043 • A09

TYPICAL APPLICATIONS

Single 5V Supply, Ultra Precision Instrumentation Amplifier

INPUT AND OUTPUT VOLTAGE RANGE INCLUDES GROUND.
INPUT REFERRED OFFSET ERRORS ARE TYPICALLY 3µV WITH
1µV OF NOISE
CMRR ≈ 120dB

LTC1043 • A10

Voltage Controlled Current Source with Ground Referred Input and Output
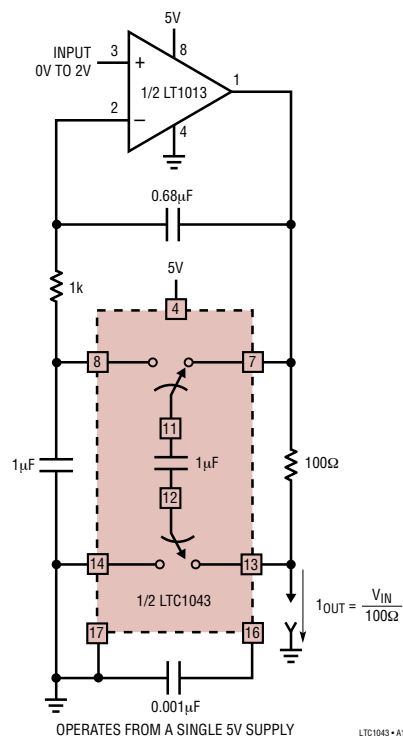
$$I_{OUT} = \frac{V_{IN}}{100\Omega}$$

OPERATES FROM A SINGLE 5V SUPPLY

LTC1043 • A11

Precision Instrumentation Amplifier

CHOPPER

AC AMPLIFIER

PHASE
SENSITIVE
DEMODULATOR

DC
OUTPUT AMPLIFIER

OFFSET = 10µV
DRIFT = 0.1µV/°C
FULL DIFFERENTIAL INPUT
CMRR = 140dB
OPEN LOOP GAIN > 10^8
GAIN = R2/R1 + 1
I_{BIAS} = 1nA

LTC1043 • A12

TYPICAL APPLICATIONS

Lock-In Amplifier (= Extremely Narrow-Band Amplifier)

THERMISTOR BRIDGE IS THE SIGNAL SOURCE

SYNCHRONOUS DEMODULATOR

500Hz SINE DRIVE

T1 = TF5SX17ZZ, TOROTEL
R$_T$ = YSI THERMISTOR 44006
  ≈ 6.19k AT 37.5°C
*MATCH 0.05%
6.19k = VISHAY S-102
OPERATE LTC1043 WITH
±5V SUPPLIES

LOCK-IN AMPLIFIER TECHNIQUE USED TO EXTRACT VERY SMALL SIGNALS BURIED INTO NOISE

V$_{OUT}$ = 1000 • DC BRIDGE SIGNAL

PHASE TRIM

ZERO CROSSING DETECTOR
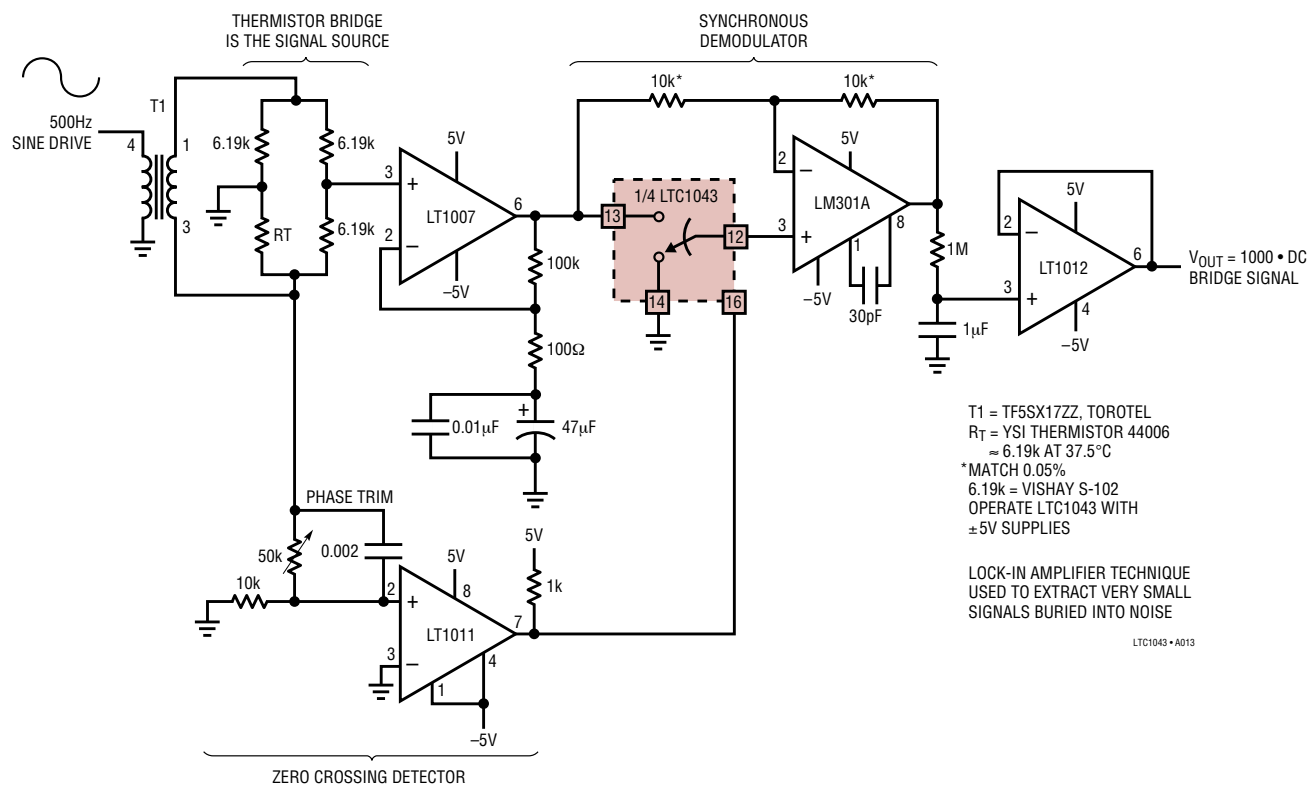
LTC1043 • A013

50MHz Termal RMS/DC Converter

CALIBRATION ADJUST

DC OUTPUT 0V TO 3.5V

300mV
10V$_{RMS}$
INPUT

2% ACCURACY DC 50MHZ
100:1 CREST FACTOR CAPABILITY
T1 TO T2 = YELLOW SPRINGS INST. CO.
THERMISTOR COMPOSITE
ENCLOSE T1 AND T2 IN STYROFOAM

*1% RESISTOR
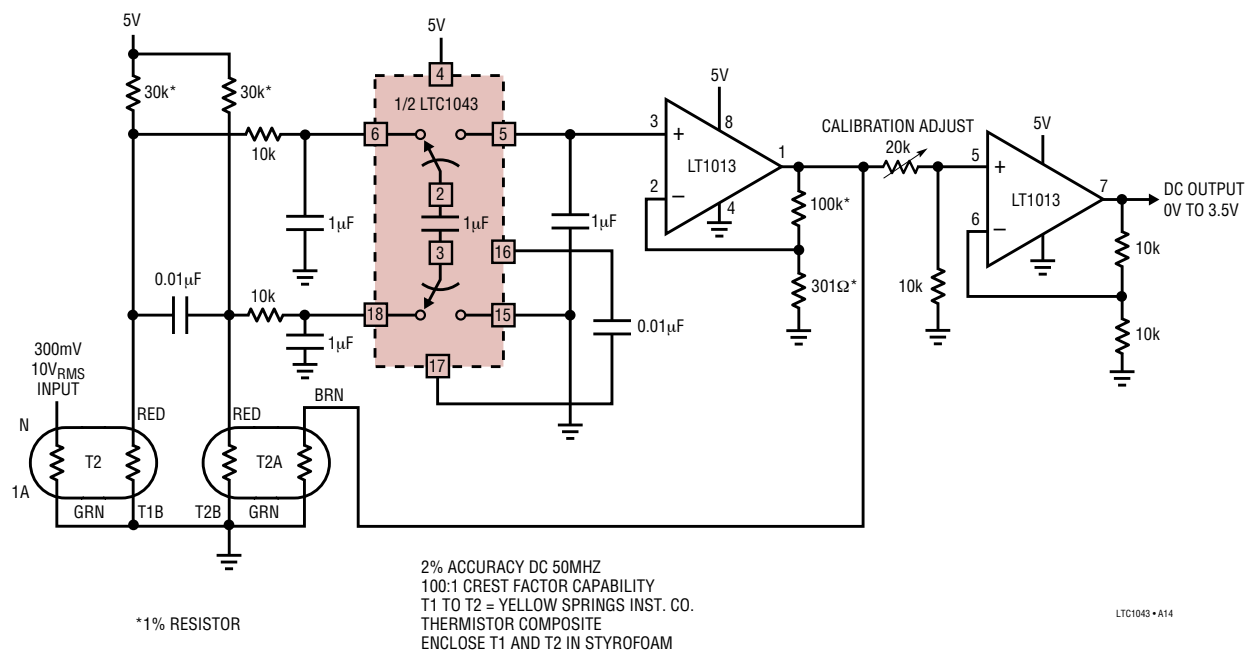
LTC1043 • A14

TYPICAL APPLICATIONS

Quad Single 5V Supply, Low Hold Step, Sample-and-Hold

LTC1043 • A15

FOR 1V ≤ V$_{IN}$ ≤ 4V, THE HOLD STEP IS ≤ 300µV
ACQUISITION TIME ~ 8 • R$_{ON}$ C$_H$ FOR 10-BIT ACCURACY
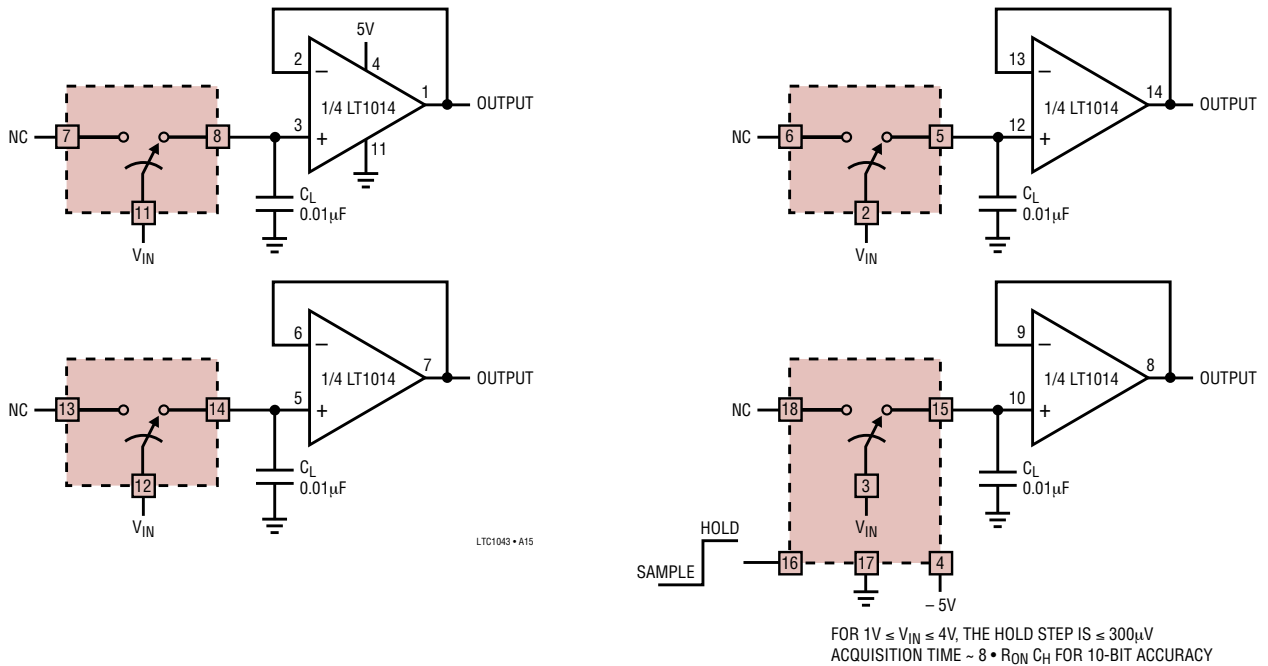
LTC1043 • A16

Single Supply Precision Linearized Platinum RTD Signal Conditioner
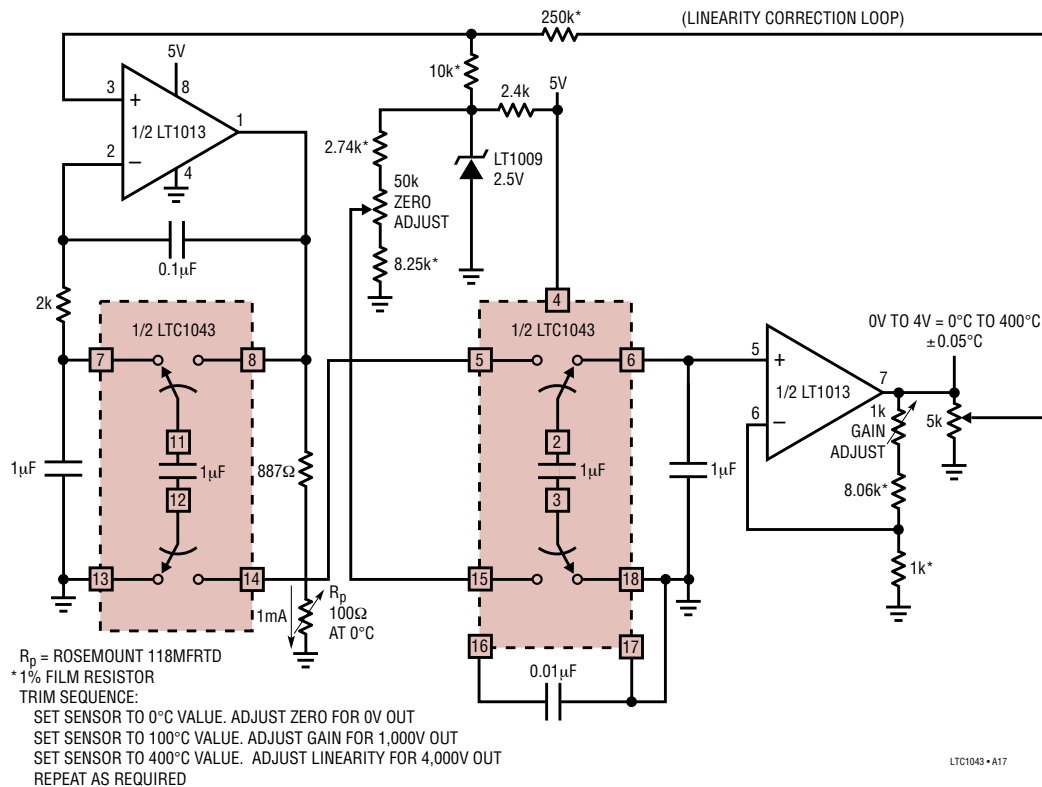
R$_p$ = ROSEMOUNT 118MFRTD
*1% FILM RESISTOR
TRIM SEQUENCE:
    SET SENSOR TO 0°C VALUE. ADJUST ZERO FOR 0V OUT
    SET SENSOR TO 100°C VALUE. ADJUST GAIN FOR 1,000V OUT
    SET SENSOR TO 400°C VALUE. ADJUST LINEARITY FOR 4,000V OUT
    REPEAT AS REQUIRED

LTC1043 • A17

1043fa

TYPICAL APPLICATIONS

0.005% F/V Converter

*75k = TRW # MTR-5/120ppm

LTC1043 • A18

High Frequency Clock Tunable Bandpass Filter

BANDPASS CENTER FREQUENCY $f_O = \dfrac{f_{CLK}}{31.4} \cdot \sqrt{\dfrac{R2}{R1}}$

BANDPASS GAIN AT f_O IS: R_Q/R_{IN}
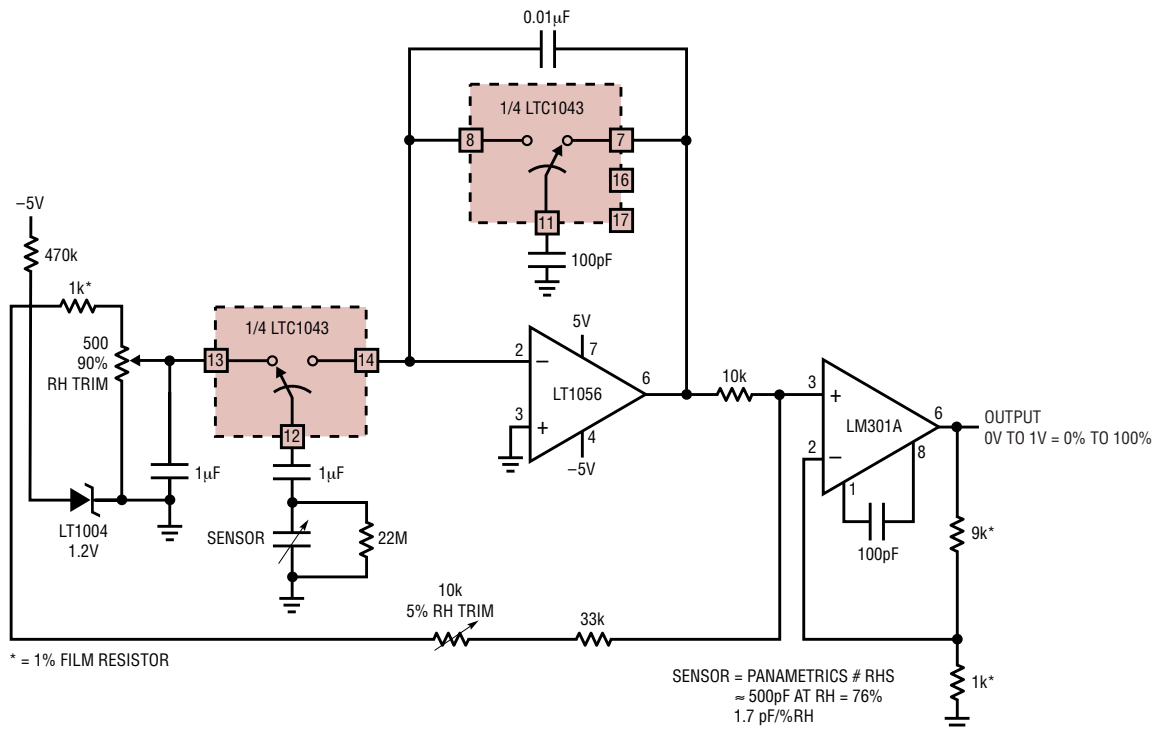
$Q = \dfrac{R_Q}{R2} \sqrt{\dfrac{R2}{R1}}$

f_O MAX ≤ 100kHz

Q_{MAX} AT 100kHz f_O IS ≤10

$(f_O \cdot Q)$ MAX ≤ 1MHz

f_{CLK} MAX ≤ 3MHz, Q < 2

LTC1043 • A19

LTC1043

TYPICAL APPLICATIONS

Frequency-Controlled Gain Amplifier

GAIN CONTROL
0kHz TO 10kHz = GAIN 0 TO 1000

FOR DIFFERENTIAL INPUT, GROUND PIN 8A AND USE PINS 13A AND 7A FOR INPUTS

$$GAIN = \frac{f_{IN} \cdot 0.01\mu F}{1kHz \cdot 100pF}; \text{ GAIN IS NEGATIVE AS SHOWN}$$

FOR SINGLE-ENDED INPUT AND POSITIVE GAIN, GROUND PIN 8A AND USE PIN 7A FOR INPUT
USE ±5V SUPPLIES FOR LTC1043

LTC1043 • A20
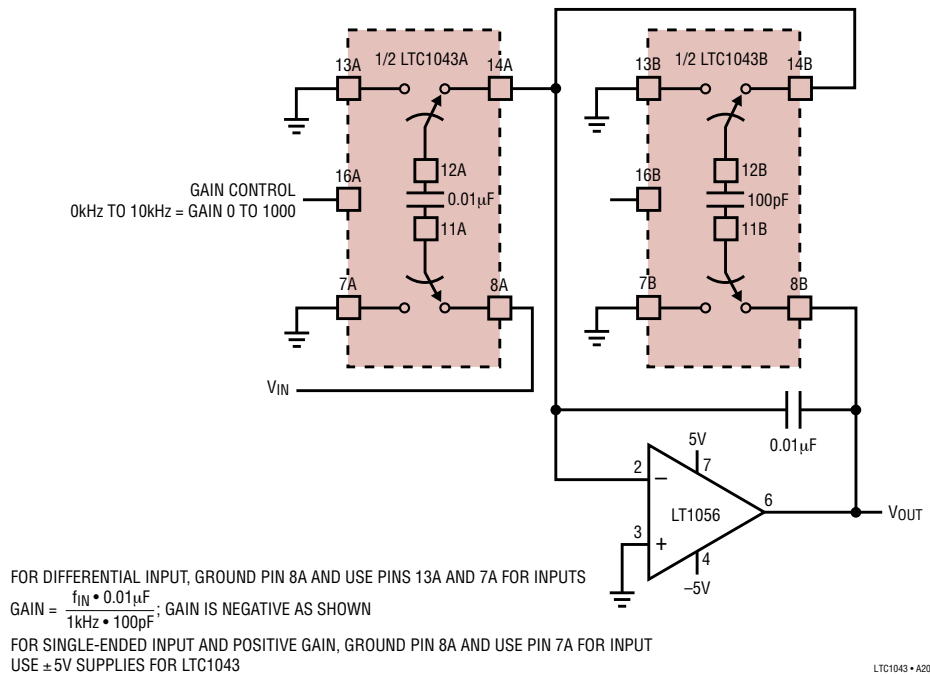
Relative Humidity Sensor Signal Conditioner

OUTPUT
0V TO 1V = 0% TO 100%

* = 1% FILM RESISTOR

SENSOR = PANAMETRICS # RHS
≈ 500pF AT RH = 76%
1.7 pF/%RH

LTC1043 • A21

TYPICAL APPLICATIONS

Linear Variable Differential Transformer (LVDT), Signal Conditioner

LTC1043 • A22

Precision Current Sensing in Supply Rails

LTC1043 • A23

PACKAGE DESCRIPTION

**D Package
18-Lead Side Brazed (Hermetic)**
(Reference LTC DWG # 05-08-1210)

.485
(12.319)
MAX

.165
(4.191)
MAX

.020 – .060
(0.508 – 1.524)

.008 – .015
(0.203 – 0.381)

.300
(7.620)
REF

.125
(3.175)
MIN

.100
(2.54)
BSC

.015 – .023
(0.381 – 0.584)

.054
(1.372)
TYP

.005
(0.127)
MIN

.910
(23.114)
MAX

.290
(7.366)
TYP

PIN NO. 1
IDENT

D18 0801
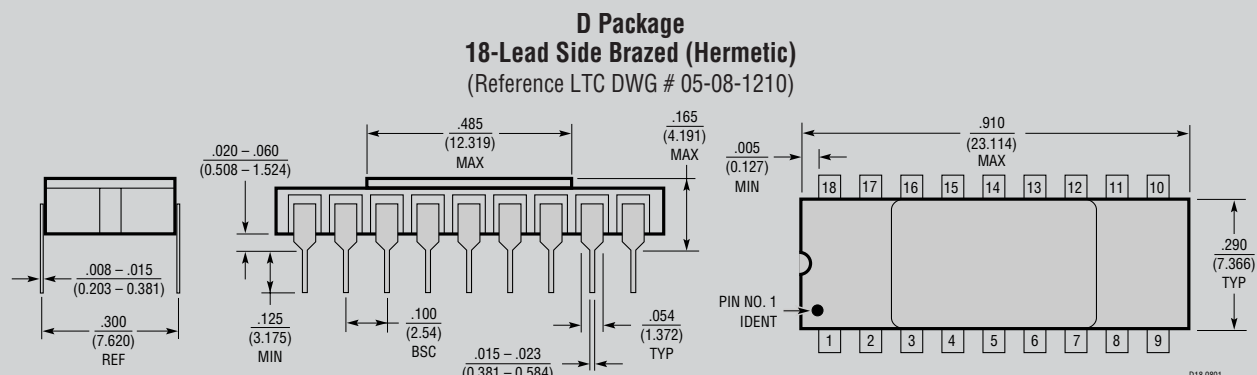
OBSOLETE PACKAGE

**N Package
18-Lead PDIP (Narrow .300 Inch)**
(Reference LTC DWG # 05-08-1510)

.900*
(22.860)
MAX

.255 ± .015*
(6.477 ± 0.381)

.300 – .325
(7.620 – 8.255)

.020
(0.508)
MIN

.008 – .015
(0.203 – 0.381)

.325 +.035 –.015
(8.255 +0.889 –0.381)

.130 ± .005
(3.302 ± 0.127)

.120
(3.048)
MIN

.005
(0.127)
MIN

.100
(2.54)
BSC

.045 – .065
(1.143 – 1.651)

.065
(1.651)
TYP

.018 ± .003
(0.457 ± 0.076)
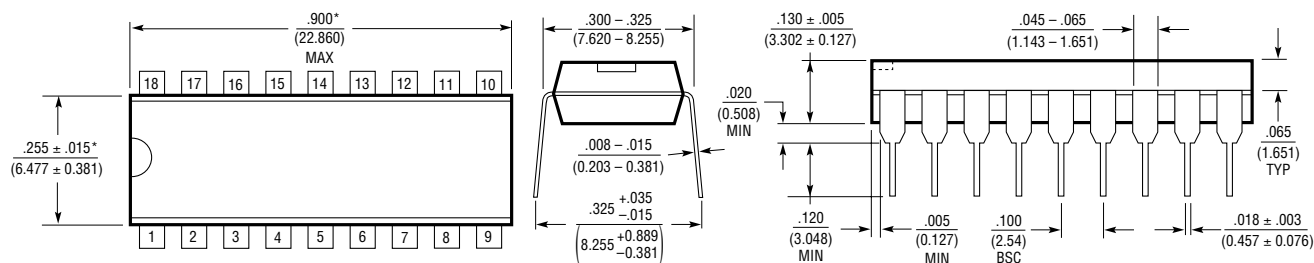
NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

N18 1002

**SW Package
18-Lead Plastic Small Outline (Wide .300 Inch)**
(Reference LTC DWG # 05-08-1620)

.030 ±.005
TYP

.050 BSC

.045 ±.005

.420
MIN

.325 ±.005

RECOMMENDED SOLDER PAD LAYOUT

.291 – .299
(7.391 – 7.595)
NOTE 4

.010 – .029
(0.254 – 0.737) × 45°

.005
(0.127)
RAD MIN

0° – 8° TYP

.009 – .013
(0.229 – 0.330)

NOTE 3

.016 – .050
(0.406 – 1.270)

.447 – .463
(11.354 – 11.760)
NOTE 4

.394 – .419
(10.007 – 10.643)

NOTE 3

.093 – .104
(2.362 – 2.642)

.050
(1.270)
BSC

.014 – .019
(0.356 – 0.482)
TYP

.037 – .045
(0.940 – 1.143)

.004 – .012
(0.102 – 0.305)
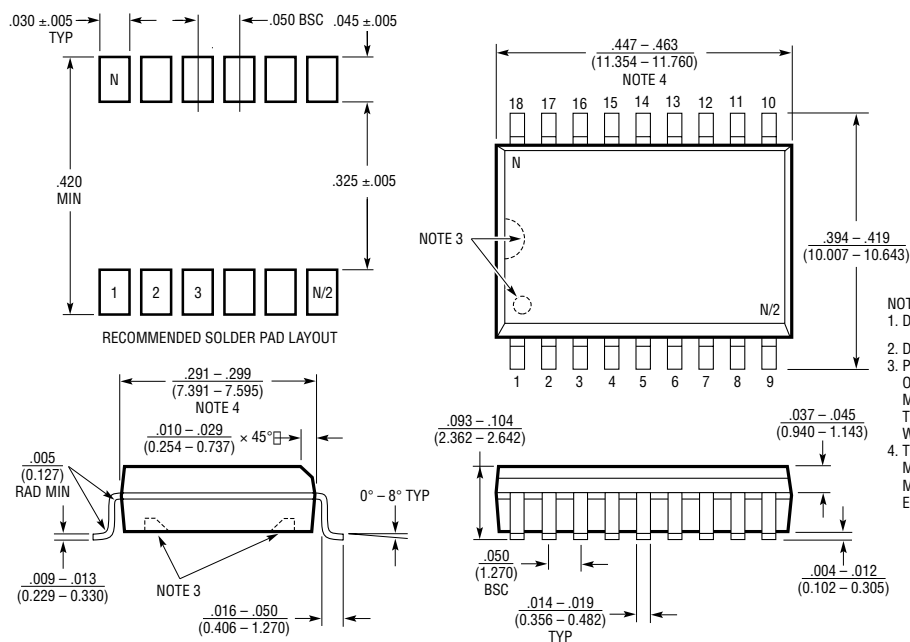
NOTE:
1. DIMENSIONS IN INCHES / (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S18 (WIDE) 0502

1043fa