ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V_S^- to V_S^+) 12.6V
Input Voltage (Note 2) ....±V_S
Input Current (Note 2) .... ±10mA
Output Short Circuit Duration (Note 3) .... Indefinite
Operating Temperature Range (Note 4) ...−40°C to 85°C
Specified Temperature Range (Note 5) ....−40°C to 85°C

Maximum Junction Temperature .... 150°C
   (DD Package) .... 125°C
Storage Temperature ....−65°C to 150°C
   (DD Package) ....−65°C to 125°C
Lead Temperature (Soldering, 10 sec.)................ 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

S5 PACKAGE
5-LEAD PLASTIC TSOT-23

T_{JMAX} = 150°C, $θ_{JA}$ = 250°C/W (NOTE 10)

ORDER PART NUMBER
LT6220CS5 LT6220IS5
S5 PART* MARKING
LTAFP

TOP VIEW

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, $θ_{JA}$ = 190°C/W

ORDER PART NUMBER
LT6220CS8 LT6220IS8
S8 PART MARKING
6220 6220I

TOP VIEW

DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, $θ_{JA}$ = 160°C/W (NOTE 10)
EXPOSED PAD INTERNALLY CONNECTED TO V_S^-
(PCB CONNECTION OPTIONAL)

TOP VIEW

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, $θ_{JA}$ = 190°C/W

TOP VIEW

GN PACKAGE
16-LEAD NARROW PLASTIC SSOP

T_{JMAX} = 150°C, $θ_{JA}$ = 135°C/W

ORDER PART NUMBER	DD PART* MARKING	ORDER PART NUMBER	S8 PART MARKING	ORDER PART NUMBER	SSOP PART MARKING
LT6221CDD LT6221IDD	LADZ	LT6221CS8 LT6221IS8	6221 6221I	LT6222CGN LT6222IGN	6222 6222I

Consult LTC Marketing for parts specified with wider operating temperature ranges.
*The temperature grades are identified by a label on the shipping container.

622012fa

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = 5V$, 0V; $V_S = 3V$, 0V; $V_{CM} = V_{OUT}$ = half supply, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = 0V$		70	350	μV
		$V_{CM} = 0V$ (DD Package)		150	700	μV
		$V_{CM} = 0V$ (S5 Package)		200	850	μV
		$V_{CM} = V_S$		0.5	2.5	mV
		$V_{CM} = V_S$ (S5 Package)		0.5	3	mV
ΔV_{OS}	Input Offset Voltage Shift	$V_S = 5V$, $V_{CM} = 0V$ to 3.5V		30	195	μV
		$V_S = 3V$, $V_{CM} = 0V$ to 1.5V		15	120	μV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	$V_{CM} = 0V$		100	600	μV
		$V_{CM} = 0V$ (DD Package)		150	1100	μV
I_B	Input Bias Current	$V_{CM} = 1V$		15	150	nA
		$V_{CM} = V_S$		250	600	nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	$V_{CM} = 1V$		15	175	nA
		$V_{CM} = V_S$		20	250	nA
I_{OS}	Input Offset Current	$V_{CM} = 1V$		15	100	nA
		$V_{CM} = V_S$		15	100	nA
	Input Noise Voltage	0.1Hz to 10Hz		0.5		μV$_{P-P}$
e_n	Input Noise Voltage Density	f = 10kHz		10		nV/$\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz		0.8		pA/$\sqrt{Hz}$
C_{IN}	Input Capacitance			2		pF
A_{VOL}	Large Signal Voltage Gain	$V_S = 5V$, $V_O = 0.5V$ to 4.5V, $R_L = 1k$ at $V_S/2$	35	100		V/mV
		$V_S = 5V$, $V_O = 1V$ to 4V, $R_L = 100\Omega$ at $V_S/2$	3.5	10		V/mV
		$V_S = 3V$, $V_O = 0.5V$ to 2.5V, $R_L = 1k$ at $V_S/2$	30	90		V/mV
CMRR	Common Mode Rejection Ratio	$V_S = 5V$, $V_{CM} = 0V$ to 3.5V	85	102		dB
		$V_S = 3V$, $V_{CM} = 0V$ to 1.5V	82	102		dB
	CMRR Match (Channel-to-Channel) (Note 9)	$V_S = 5V$, $V_{CM} = 0V$ to 3.5V	79	100		dB
		$V_S = 3V$, $V_{CM} = 0V$ to 1.5V	76	100		dB
	Input Common Mode Range		0		V_S	V
PSRR	Power Supply Rejection Ratio	$V_S = 2.5V$ to 10V, $V_{CM} = 0V$	84	105		dB
	PSRR Match (Channel-to-Channel) (Note 9)		79	105		dB
	Minimum Supply Voltage (Note 6)			2.2	2.5	V
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load		5	40	mV
		$I_{SINK} = 5mA$		100	200	mV
		$I_{SINK} = 20mA$		325	650	mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load		5	40	mV
		$I_{SOURCE} = 5mA$		130	250	mV
		$I_{SOURCE} = 20mA$		475	900	mV
I_{SC}	Short-Circuit Current	$V_S = 5V$	20	45		mA
		$V_S = 3V$	20	35		mA
I_S	Supply Current Per Amplifier			0.9	1	mA
GBW	Gain-Bandwidth Product	$V_S = 5V$, Frequency = 1MHz	35	60		MHz
SR	Slew Rate	$V_S = 5V$, $A_V = -1$, $R_L = 1k$, $V_O = 4V$	10	20		V/μs
FPBW	Full Power Bandwidth	$V_S = 5V$, $A_V = 1$, $V_O = 4V_{p-p}$		1.6		MHz
HD	Harmonic Distortion	$V_S = 5V$, $A_V = 1$, $R_L = 1k$, $V_O = 2V_{P-P}$, $f_C = 500kHz$		-77.5		dBc
t_S	Settling Time	0.01%, $V_S = 5V$, $V_{STEP} = 2V$, $A_V = 1$, $R_L = 1k$		300		ns
ΔG	Differential Gain (NTSC)	$V_S = 5V$, $A_V = 2$, $R_L = 1k$		0.3		%
$\Delta\theta$	Differential Phase (NTSC)	$V_S = 5V$, $A_V = 2$, $R_L = 1k$		0.3		Deg

622012fa

3

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the 0°C ≤ T_A ≤ 70°C temperature range. V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 0V	●		90	500	µV
		V_{CM} = 0V (DD Package)	●		180	850	µV
		V_{CM} = 0V (S5 Package)	●		230	1250	µV
		V_{CM} = V_S	●		0.5	3	mV
		V_{CM} = V_S (S5 Package)	●		0.5	3.5	mV
ΔV_{OS}	Input Offset Voltage Shift	V_S = 5V, V_{CM} = 0V to 3.5V	●		30	280	µV
		V_S = 3V, V_{CM} = 0V to 1.5V	●		15	190	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = 0V	●		110	850	µV
		V_{CM} = 0V (DD Package)	●		180	1400	µV
V_{OS} TC	Input Offset Voltage Drift (Note 8)		●		1.5	5	µV/°C
		(S5 Package)	●		3.5	10	µV/°C
I_B	Input Bias Current	V_{CM} = 1V	●		20	175	nA
		V_{CM} = V_S – 0.2V	●		275	800	nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = 1V	●		15	200	nA
		V_{CM} = V_S – 0.2V	●		20	300	nA
I_{OS}	Input Offset Current	V_{CM} = 1V	●		15	125	nA
		V_{CM} = V_S – 0.2V	●		15	125	nA
A_{VOL}	Large Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k at V_S/2	●	30	90		V/mV
		V_S = 5V, V_O = 1V to 4V, R_L = 100Ω at V_S/2	●	3	9		V/mV
		V_S = 3V, V_O = 0.5V to 2.5V, R_L = 1k at V_S/2	●	25	80		V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 0V to 3.5V	●	82	100		dB
		V_S = 3V, V_{CM} = 0V to 1.5V	●	78	100		dB
	CMRR Match (Channel-to-Channel) (Note 9)	V_S = 5V, V_{CM} = 0V to 3.5V	●	77	100		dB
		V_S = 3V, V_{CM} = 0V to 1.5V	●	73	100		dB
	Input Common Mode Range		●	0		V_S	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	●	81	104		dB
	PSRR Match (Channel-to-Channel) (Note 9)		●	76	104		dB
	Minimum Supply Voltage (Note 6)		●		2.2	2.5	V
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load	●		8	50	mV
		I_{SINK} = 5mA	●		110	220	mV
		I_{SINK} = 20mA	●		375	750	mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load	●		8	50	mV
		I_{SOURCE} = 5mA	●		150	300	mV
		I_{SOURCE} = 20mA	●		600	1100	mV
I_{SC}	Short-Circuit Current	V_S = 5V	●	20	40		mA
		V_S = 3V	●	20	30		mA
I_S	Supply Current Per Amplifier		●		1	1.4	mA
GBW	Gain-Bandwidth Product	V_S = 5V, Frequency = 1MHz	●	30	60		MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 4V_{P-P}	●	9	18		V/µs

622012fa

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the −40°C ≤ T_A ≤ 85°C temperature range. V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 0V	●		125	700	µV
		V_{CM} = 0V (DD Package)	●		300	1300	µV
		V_{CM} = 0V (S5 Package)	●		350	2000	µV
		V_{CM} = V_S	●		0.75	3.5	mV
		V_{CM} = V_S (S5 Package)	●		1	4.5	mV
ΔV_{OS}	Input Offset Voltage Shift	V_S = 5V, V_{CM} = 0V to 3.5V	●		30	300	µV
		V_S = 3V, V_{CM} = 0V to 1.5V	●		30	210	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = 0V	●		175	1200	µV
		V_{CM} = 0V (DD Package)	●		300	2200	µV
V_{OS} TC	Input Offset Voltage Drift (Note 8)		●		1.5	7.5	µV/°C
		(S5 Package)	●		3.5	15	µV/°C
I_B	Input Bias Current	V_{CM} = 1V	●		25	200	nA
		V_{CM} = V_S − 0.2V	●		300	900	nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = 1V	●		15	250	nA
		V_{CM} = V_S − 0.2V	●		20	350	nA
I_{OS}	Input Offset Current	V_{CM} = 1V	●		20	150	nA
		V_{CM} = V_S − 0.2V	●		20	150	nA
A_{VOL}	Large Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k at V_S/2	●	25	70		V/mV
		V_S = 5V, V_O = 1.5V to 3.5V, R_L = 100Ω at V_S/2	●	2.5	8		V/mV
		V_S = 3V, V_O = 0.5V to 2.5V, R_L= 1k at V_S/2	●	20	60		V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 0V to 3.5V	●	81	100		dB
		V_S = 3V, V_{CM} = 0V to 1.5V	●	77	100		dB
	CMRR Match (Channel-to-Channel) (Note 9)	V_S = 5V, V_{CM} = 0V to 3.5V	●	76	100		dB
		V_S = 3V, V_{CM} = 0V to 1.5V	●	72	100		dB
	Input Common Mode Range		●	0		V_S	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	●	79	104		dB
	PSRR Match (Channel-to-Channel) (Note 9)		●	74	104		dB
	Minimum Supply Voltage (Note 6)		●		2.2	2.5	V
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load	●		10	60	mV
		I_{SINK} = 5mA	●		120	240	mV
		I_{SINK} = 10mA	●		220	450	mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load	●		10	60	mV
		I_{SOURCE} = 5mA	●		160	325	mV
		I_{SOURCE} = 10mA	●		325	650	mV
I_{SC}	Short-Circuit Current	V_S = 5V	●	12.5	30		mA
		V_S = 3V	●	12.5	25		mA
I_S	Supply Current Per Amplifier		●		1.1	1.5	mA
GBW	Gain-Bandwidth Product	V_S = 5V, Frequency = 1MHz	●	25	50		MHz
SR	Slew Rate	V_S = 5V, A_V = −1, R_L = 1k, V_O = 4V	●	8	15		V/µs

622012fa

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = ±5V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = -5V$		80	500	μV
		$V_{CM} = -5V$ (DD Package)		150	750	μV
		$V_{CM} = -5V$ (S5 Package)		200	900	μV
		$V_{CM} = 5V$		0.7	2.5	mV
		$V_{CM} = 5V$ (S5 Package)		0.7	3	mV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = -5V$ to 3.5V		70	675	μV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = -5V$		100	850	μV
		$V_{CM} = -5V$ (DD Package)		150	1300	μV
I_B	Input Bias Current	$V_{CM} = -4V$		20	150	nA
		$V_{CM} = 5V$		250	700	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = -4V$		15	175	nA
		$V_{CM} = 5V$		20	250	nA
I_{OS}	Input Offset Current	$V_{CM} = -4V$		15	100	nA
		$V_{CM} = 5V$		15	100	nA
	Input Noise Voltage	0.1Hz to 10Hz		0.5		μV_{P-P}
e_n	Input Noise Voltage Density	f = 10kHz		10		nV/√Hz
i_n	Input Noise Current Density	f = 10kHz		0.8		pA/√Hz
C_{IN}	Input Capacitance	f = 100kHz		2		pF
A_{VOL}	Large Signal Voltage Gain	$V_O = -4V$ to 4V, $R_L = 1k$	35	95		V/mV
		$V_O = -2V$ to 2V, $R_L = 100\Omega$	3.5	10		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = -5V$ to 3.5V	82	102		dB
	CMRR Match (Channel-to-Channel)		77	100		dB
	Input Common Mode Range		V_S^-		V_S^+	V
PSRR	Power Supply Rejection Ratio	$V_S^+ = 2.5V$ to 10V, $V_S^- = 0V$, $V_{CM} = 0V$	84	105		dB
	PSRR Match (Channel-to-Channel)		79	105		dB
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load		5	40	mV
		$I_{SINK} = 5mA$		100	200	mV
		$I_{SINK} = 20mA$		325	650	mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load		5	40	mV
		$I_{SOURCE} = 5mA$		130	250	mV
		$I_{SOURCE} = 20mA$		475	900	mV
I_{SC}	Short-Circuit Current		25	50		mA
I_S	Supply Current Per Amplifier			1	1.5	mA
GBW	Gain-Bandwidth Product	Frequency = 1MHz		60		MHz
SR	Slew Rate	$A_V = -1$, $R_L = 1k$, $V_O = ±4V$, Measure at $V_O = ±2V$		20		V/μs
FPBW	Full Power Bandwidth	$V_O = 8V_{P-P}$		0.8		MHz
HD	Harmonic Distortion	$A_V = 1$, $R_L = 1k$, $V_O = 2V_{p-p}$, $f_c = 500kHz$		−77.5		dBc
t_S	Settling Time	0.01%, $V_{STEP} = 5V$, $A_V = 1$, $R_L = 1k$		375		ns
ΔG	Differential Gain (NTSC)	$A_V = 2$, $R_L = 1k$		0.15		%
$\Delta\theta$	Differential Phase (NTSC)	$A_V = 2$, $R_L = 1k$		0.6		Deg

622012fa

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the 0°C ≤ T_A ≤ 70°C temperature range. V_S = ±5V, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = −5V	●		100	650	µV
		V_{CM} = −5V (DD Package)	●		180	900	µV
		V_{CM} = −5V (S5 Package)	●		230	1300	µV
		V_{CM} = 5V	●		0.75	3	mV
		V_{CM} = 5V (S5 Package)	●		0.75	3.5	mV
ΔV_{OS}	Input Offset Voltage Shift	V_{CM} = −5V to 3.5V	●		90	850	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = −5V	●		90	1100	µV
		V_{CM} = −5V (DD Package)	●		180	1500	µV
V_{OS} TC	Input Offset Voltage Drift (Note 8)		●		1.5	5	µV/°C
		(S5 Package)	●		3.5	10	µV/°C
I_B	Input Bias Current	V_{CM} = −4V	●		20	175	nA
		V_{CM} = 4.8V	●		275	800	nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = −4V	●		15	200	nA
		V_{CM} = 4.8V	●		20	300	nA
I_{OS}	Input Offset Current	V_{CM} = −4V	●		15	125	nA
		V_{CM} = 4.8V	●		15	125	nA
A_{VOL}	Large Signal Voltage Gain	V_O = −4V to 4V, R_L = 1k	●	30	90		V/mV
		V_O = −2V to 2V, R_L =100Ω	●	3	9		V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = −5V to 3.5V	●	80	100		dB
	CMRR Match (Channel-to-Channel) (Note 9)		●	75	100		dB
	Input Common Mode Range		●	V_S^-		V_S^+	V
PSRR	Power Supply Rejection Ratio	V_S^+ = 2.5V to 10V, V_S^- = 0V, V_{CM} = 0V	●	81	104		dB
	PSRR Match (Channel-to-Channel) (Note 9)		●	76	104		dB
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load	●		8	50	mV
		I_{SINK} = 5mA	●		110	220	mV
		I_{SINK} = 20mA	●		375	750	mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load	●		8	50	mV
		I_{SOURCE} = 5mA	●		150	300	mV
		I_{SOURCE} = 20mA	●		600	1100	mV
I_{SC}	Short-Circuit Current		●	20	40		mA
I_S	Supply Current Per Amplifier		●		1.2	2	mA
GBW	Gain-Bandwidth Product	Frequency = 1MHz	●		60		MHz
SR	Slew Rate	A_V = −1, R_L = 1k, V_O = ±4V, Measure at V_O = ±2V	●		18		V/µs

622012fa

7

LT6220/LT6221/LT6222

ELECTRICAL CHARACTERISTICS
The ● denotes the specifications which apply over the −40°C ≤ T_A ≤ 85°C temperature range. V_S = ±5V, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = −5V	●		150	800	µV
		V_{CM} = −5V (DD Package)	●		300	1300	µV
		V_{CM} = −5V (S5 Package)	●		350	2000	µV
		V_{CM} = 5V	●		0.75	3.5	mV
		V_{CM} = 5V (S5 Package)	●		1	4.5	mV
ΔV_{OS}	Input Offset Voltage Shift	V_{CM} = −5V to 3.5V	●		90	950	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = −5V	●		175	1350	µV
		V_{CM} = −5V (DD Package)	●		300	2200	µV
V_{OS} TC	Input Offset Voltage Drift (Note 8)		●		1.5	7.5	µV/°C
		(S5 Package)	●		3.5	15	µV/°C
I_B	Input Bias Current	V_{CM} = −4V	●		25	200	nA
		V_{CM} = 4.8V	●		300	900	nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = −4V	●		15	250	nA
		V_{CM} = 4.8V	●		20	350	nA
I_{OS}	Input Offset Current	V_{CM} = −4V	●		20	150	nA
		V_{CM} = 4.8V	●		20	150	nA
A_{VOL}	Large Signal Voltage Gain	V_O = −4V to 4V, R_L = 1k	●	25	70		V/mV
		V_O = −1V to 1V, R_L = 100Ω	●	2.5	8		V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = −5V to 3.5V	●	79	100		dB
	CMRR Match (Channel-to-Channel) (Note 9)		●	74	100		dB
	Input Common Mode Range		●	−5		5	V
PSRR	Power Supply Rejection Ratio	V_S^+ = 2.5V to 10V, V_S^- = 0V, V_{CM} = 0V	●	79	104		dB
	PSRR Match (Channel-to-Channel) (Note 9)		●	74	104		dB
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load	●		10	60	mV
		I_{SINK} = 5mA	●		120	240	mV
		I_{SINK} = 10mA	●		220	450	mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load	●		10	60	mV
		I_{SOURCE} = 5mA	●		160	325	mV
		I_{SOURCE} = 10mA	●		325	650	mV
I_{SC}	Short-Circuit Current		●	12.5	30		mA
I_S	Supply Current		●		1.4	2.25	mA
GBW	Gain-Bandwidth Product	Frequency = 1MHz	●		50		MHz
SR	Slew Rate	A_V = −1, R_L = 1k, V_O = ±4V, Measure at V_O = ±2V	●		15		V/µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The inputs are protected by back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LT6220C/LT6221C/LT6222C and LT6220I/LT6221I/LT6222I are guaranteed functional over the temperature range of −40°C and 85°C.

Note 5: The LT6220C/LT6221C/LT6222C are guaranteed to meet specified performance from 0°C to 70°C. The LT6220C/LT6221C/LT6222C are designed, characterized and expected to meet specified performance from −40°C to 85°C but is not tested or QA sampled at these temperatures. The

LT6220I/LT6221I/LT6222I are guaranteed to meet specified performance from −40°C to 85°C.

Note 6: Minimum supply voltage is guaranteed by power supply rejection ratio test.

**Note 7:** Output voltage swings are measured between the output and power supply rails.

Note 8: This parameter is not 100% tested.

Note 9: Matching parameters are the difference between amplifiers A and D and between B and C on the LT6222; between the two amplifiers on the LT6221.

Note 10: Thermal resistance (θ_{JA}) varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads. If desired, the thermal resistance can be substantially reduced by connecting Pin 2 of the LT6220CS5/LT6220IS5 or the underside metal of DD packages to a larger metal area (V_S^- trace).
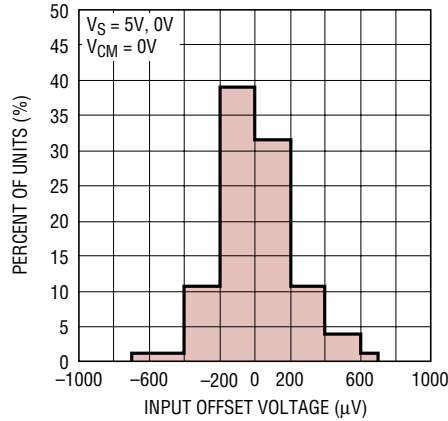
622012fa

8

LINEAR TECHNOLOGY

TYPICAL PERFORMANCE CHARACTERISTICS
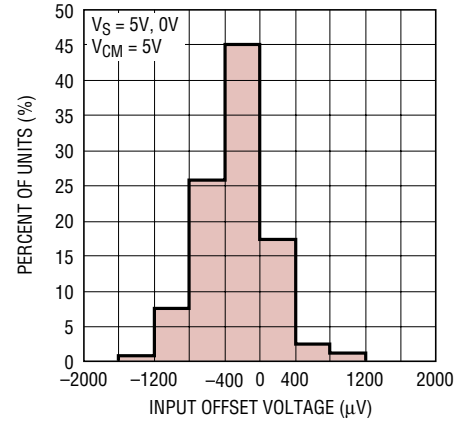
V_OS Distribution, V_CM = 0V (S8, PNP Stage)
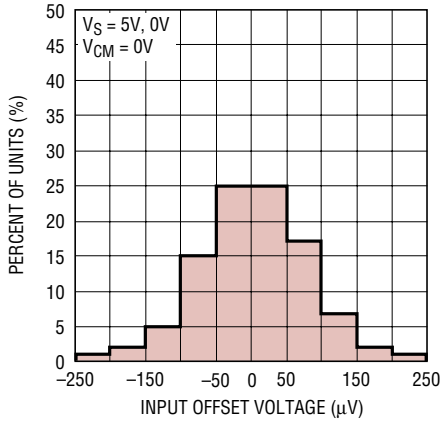
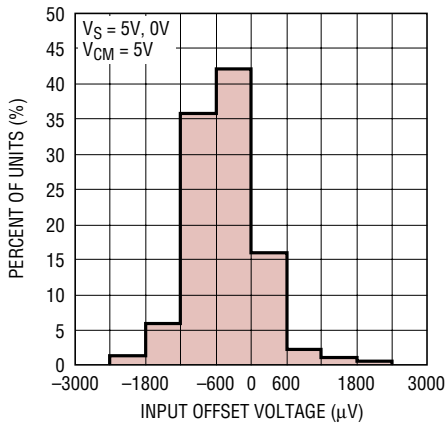622012 G01

V_OS Distribution, V_CM = 0V (SOT5, PNP Stage)

622012 G02

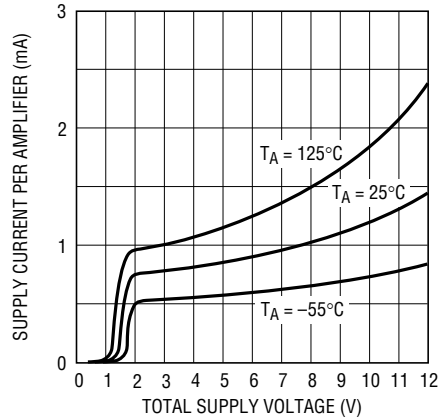**V_OS Distribution, V_CM = 5V (S8, NPN Stage)**

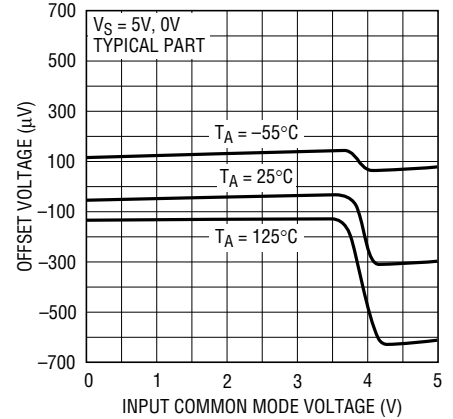622012 G03

V_OS Distribution, V_CM = 5V (SOT5, NPN Stage)

622012 G04

Supply Current vs Supply Voltage
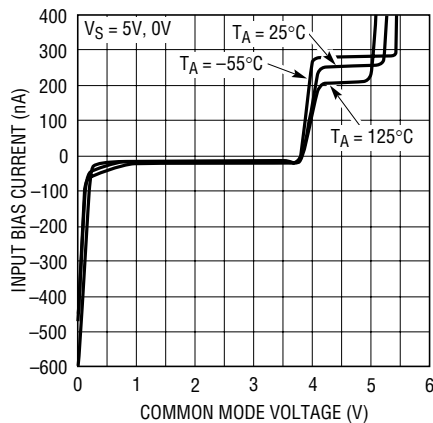

622012 G05

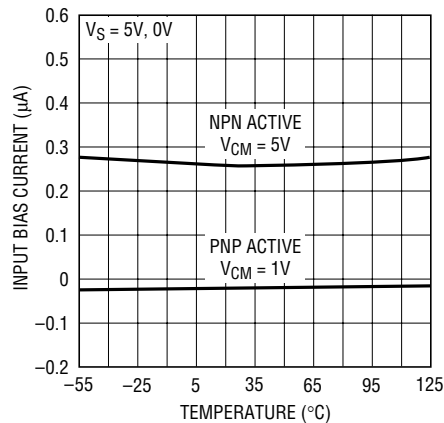**Offset Voltage vs Input Common Mode Voltage**
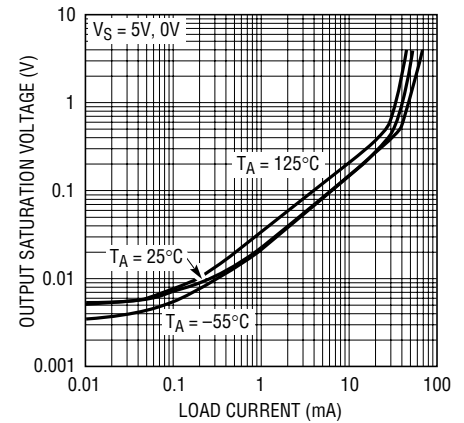

622012 G06

Input Bias Current vs Common Mode Voltage

622012 G07

Input Bias Current vs Temperature

622012 G08

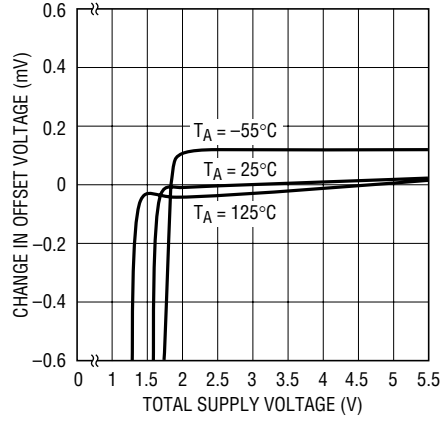**Output Saturation Voltage vs Load Current (Output Low)**

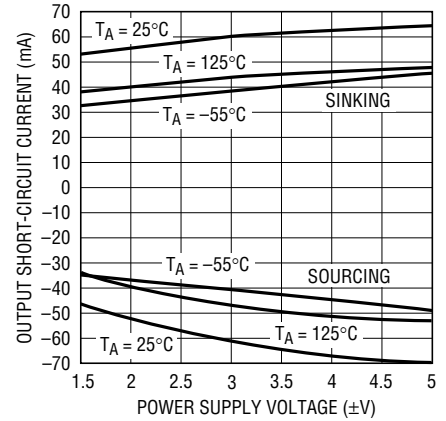622012 G09

622012fa

TYPICAL PERFORMANCE CHARACTERISTICS

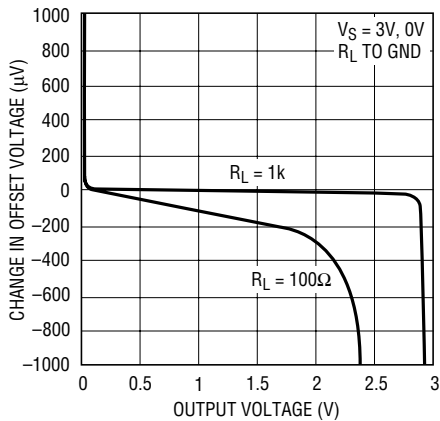**Output Saturation Voltage
vs Load Current (Output High)**

622012 G10

Minimum Supply Voltage

622012 G11
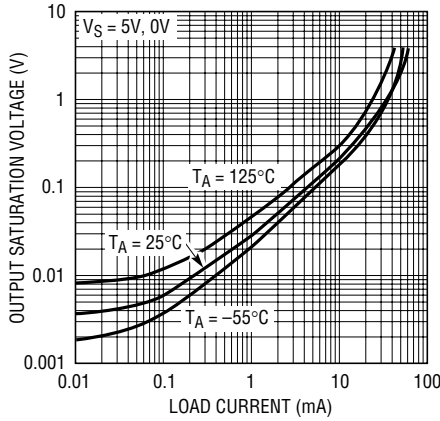
**Output Short-Circuit Current
vs Power Supply Voltage**

622012 G12

Open-Loop Gain

622012 G13

Open-Loop Gain

622012 G14

Open-Loop Gain

622012 G15
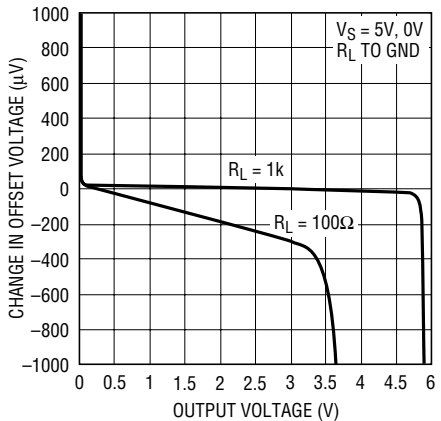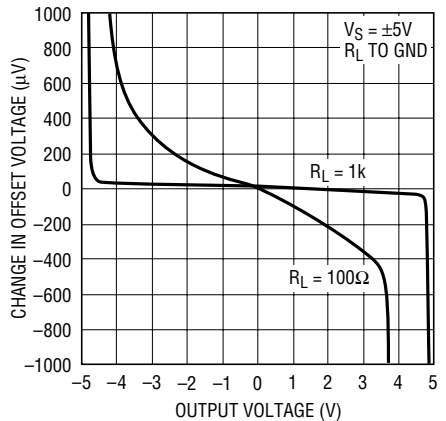
Offset Voltage vs Output Current

622012 G16
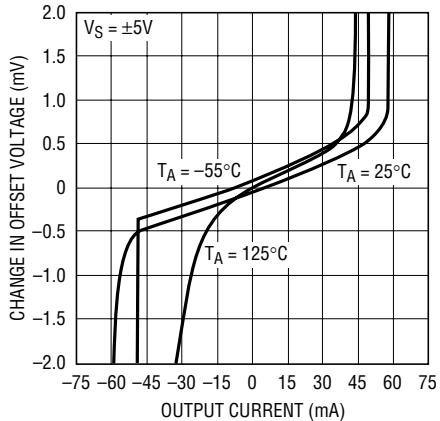
Warm-Up Drift vs Time

622012 G17
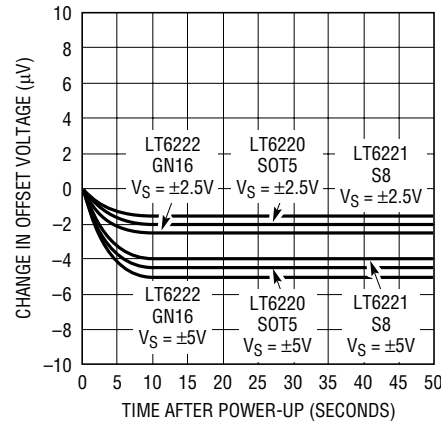
Input Noise Voltage vs Frequency

622012 G18

622012fa

10
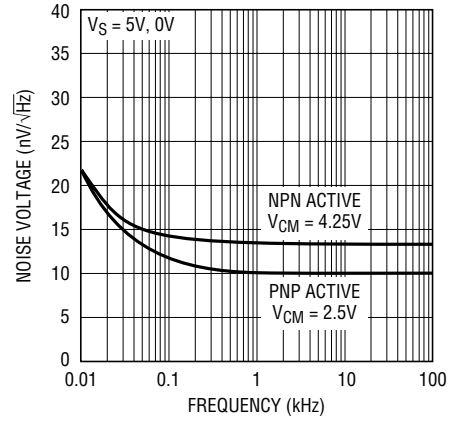
TYPICAL PERFORMANCE CHARACTERISTICS

Input Current Noise vs Frequency

622012 G19
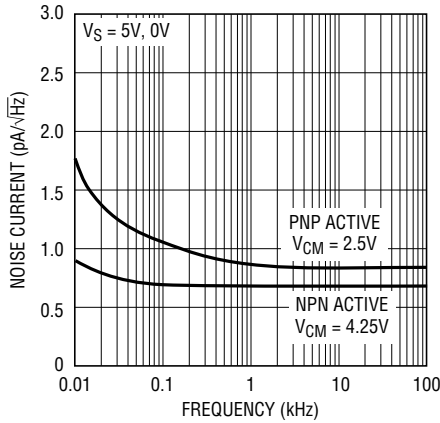
0.1Hz to 10Hz Output Voltage Noise

622012 G20
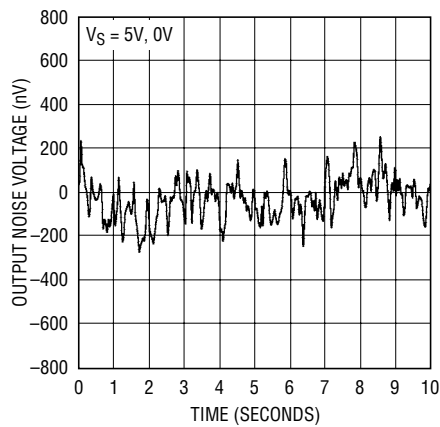
Gain Bandwidth and Phase Margin vs Supply Voltage

622012 G21
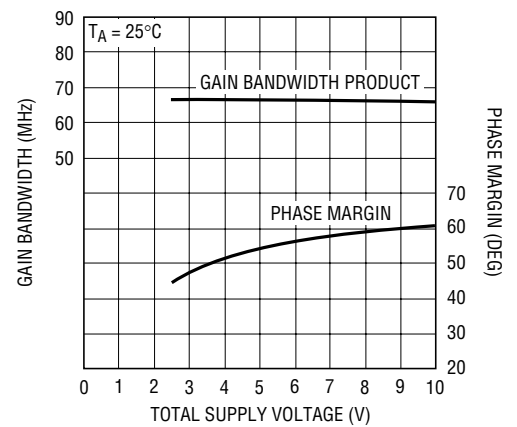
Gain Bandwidth and Phase Margin vs Temperature
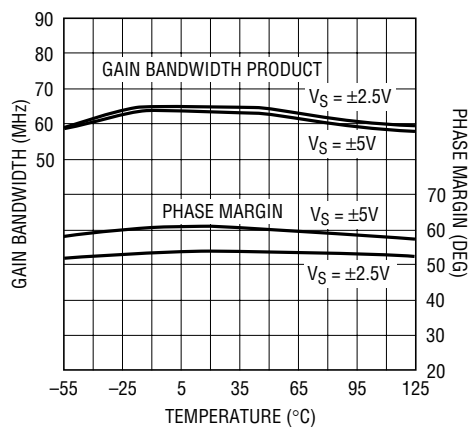
622012 G22

Gain and Phase vs Frequency
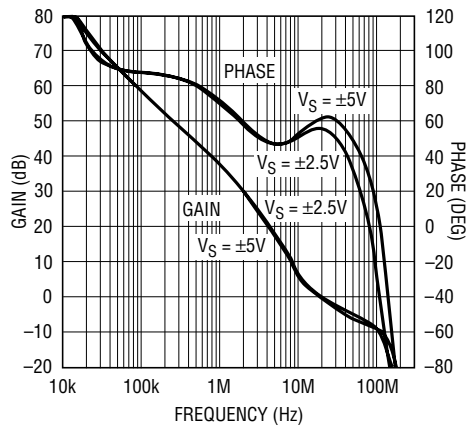
622012 G23

Slew Rate vs Temperature
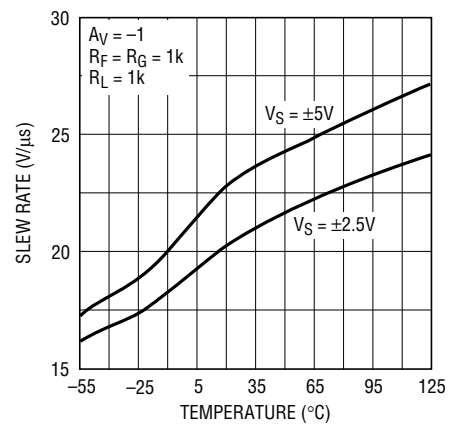
622012 G24

Gain vs Frequency ($A_V = 1$)
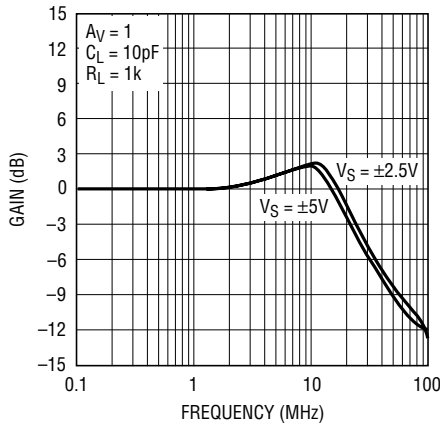
622012 G25

Gain vs Frequency ($A_V = 2$)
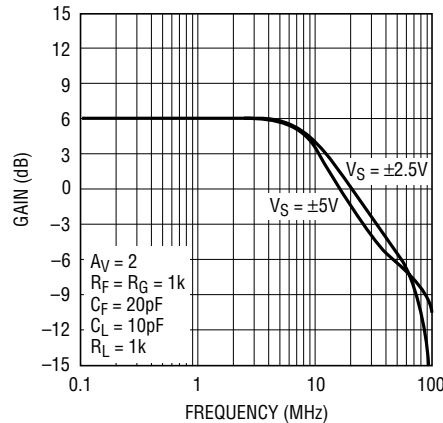
622012 G26

Output Impedance vs Frequency

620012 G27

622012fa

11
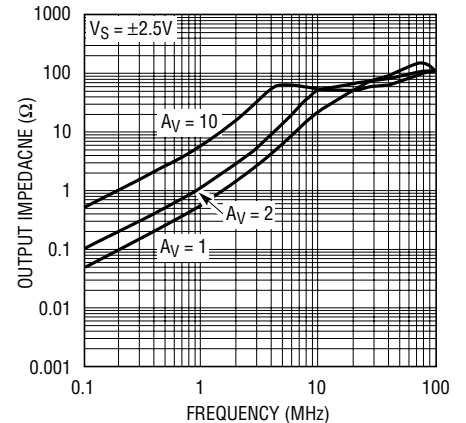
TYPICAL PERFORMANCE CHARACTERISTICS

Common Mode Rejection Ratio vs Frequency
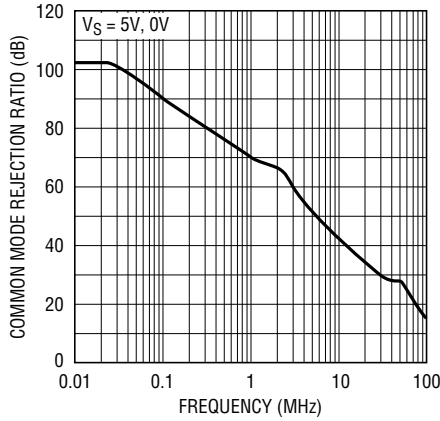
622012 G28

Power Supply Rejection Ratio vs Frequency
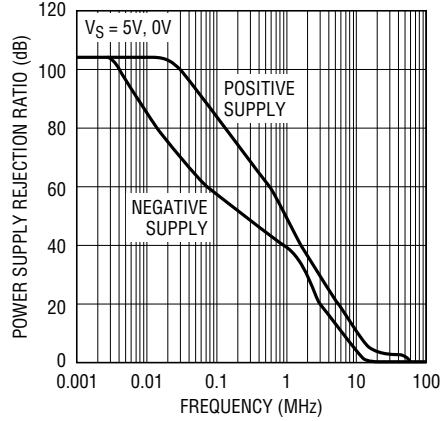
622012 G29

Series Output Resistor vs Capacitive Load
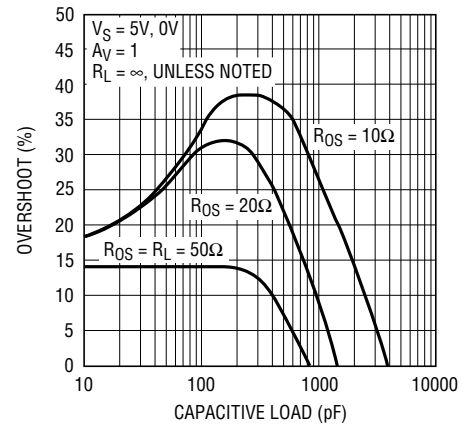
622012 G31

Series Output Resistor vs Capacitive Load
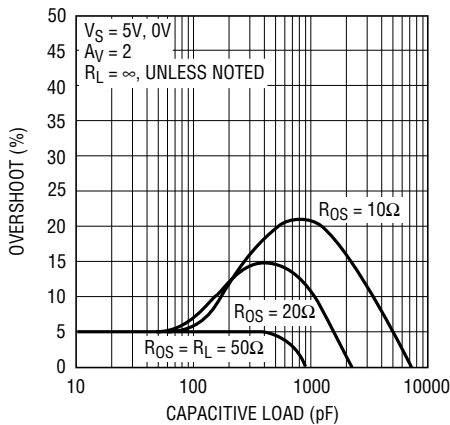
622012 G32

Distortion vs Frequency
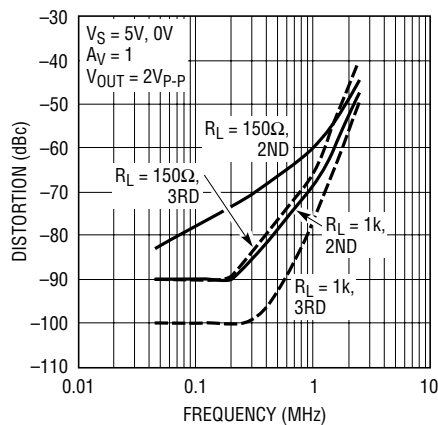
622012 G33

Distortion vs Frequency
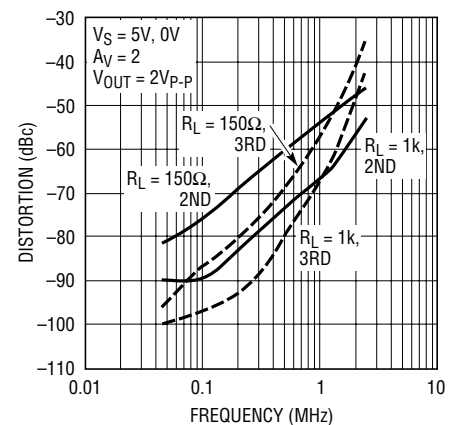
622012 G34

Maximum Undistorted Output Signal vs Frequency
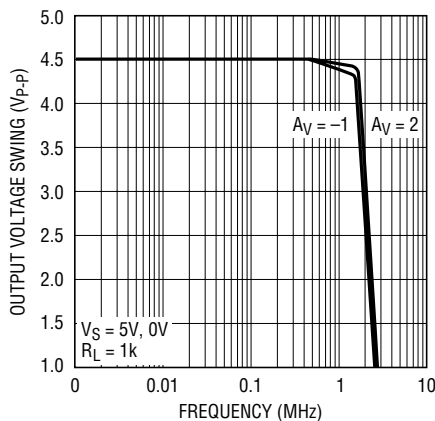
622012 G35

5V Large-Signal Response

$V_S = 5V, 0V$
$A_V = 1$
$R_L = 1k$

100ns/DIV
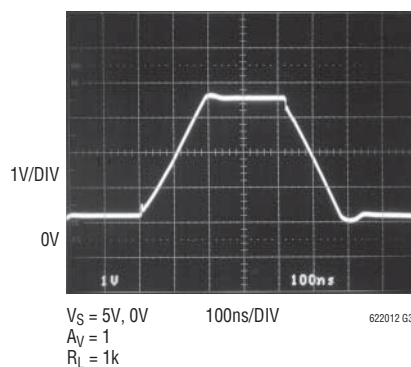
622012 G36

5V Small-Signal Response

$V_S = 5V, 0V$
$A_V = 1$
$R_L = 1k$

50ns/DIV

622012 G37

622012fa

12
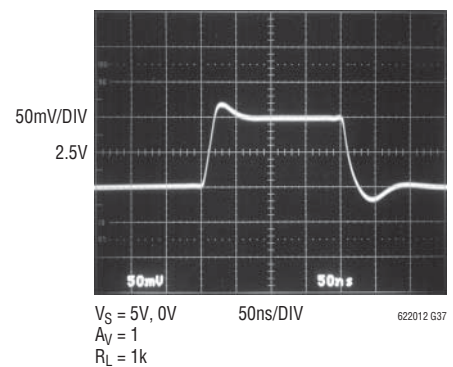
TYPICAL PERFORMANCE CHARACTERISTICS

±5V Large-Signal Response

2V/DIV

0V

2V   200ns

$V_S = \pm5V$
$A_V = 1$
$R_L = 1k$

200ns/DIV   622012 G38

±5V Small-Signal Response

50mV/DIV

0V

50mV   50ns

$V_S = \pm5V$
$A_V = 1$
$R_L = 1k$

50ns/DIV   622012 G39
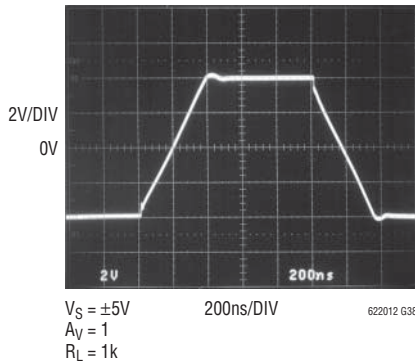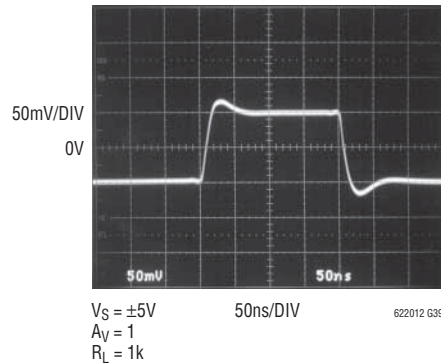
Output Overdriven Recovery

V_{IN}
1V/DIV

0V

V_{OUT}
2V/DIV

0V

2V   1V   200ns

$V_S = 5V, 0V$
$A_V = 2$
$R_L = 1k$

200ns/DIV   622012 G40
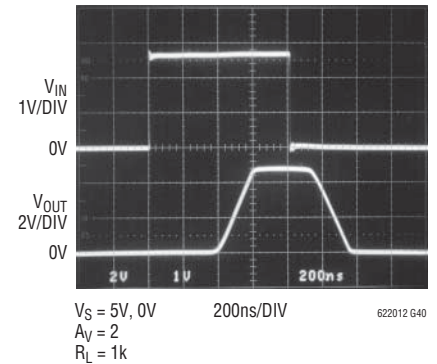
APPLICATIONS INFORMATION

Circuit Description

The LT6220/LT6221/LT6222 have an input and output signal range that covers from the negative power supply to the positive power supply. Figure 1 depicts a simplified schematic of the amplifier. The input stage comprises two differential amplifiers, a PNP stage, Q1/Q2, and an NPN stage, Q3/Q4, that are active over different ranges of common mode input voltage. The PNP stage is active between the negative supply to approximately 1.2V below the positive supply. As the input voltage moves closer toward the positive supply, the transistor Q5 will steer the tail current, I_1, to the current mirror, Q6/Q7, activating the NPN differential pair and the PNP pair becomes inactive for the rest of the input common mode range up to the positive supply. Also, at the input stage, devices Q17 to Q19 act to cancel the bias current of the PNP input pair. When Q1/Q2 are active, the current in Q16 is controlled to be the same as the current Q1/Q2. Thus, the base current of Q16 is nominally equal to the base current of the input devices. The base current of Q16 is then mirrored by devices Q17-Q19 to cancel the base current of the input devices Q1/Q2.
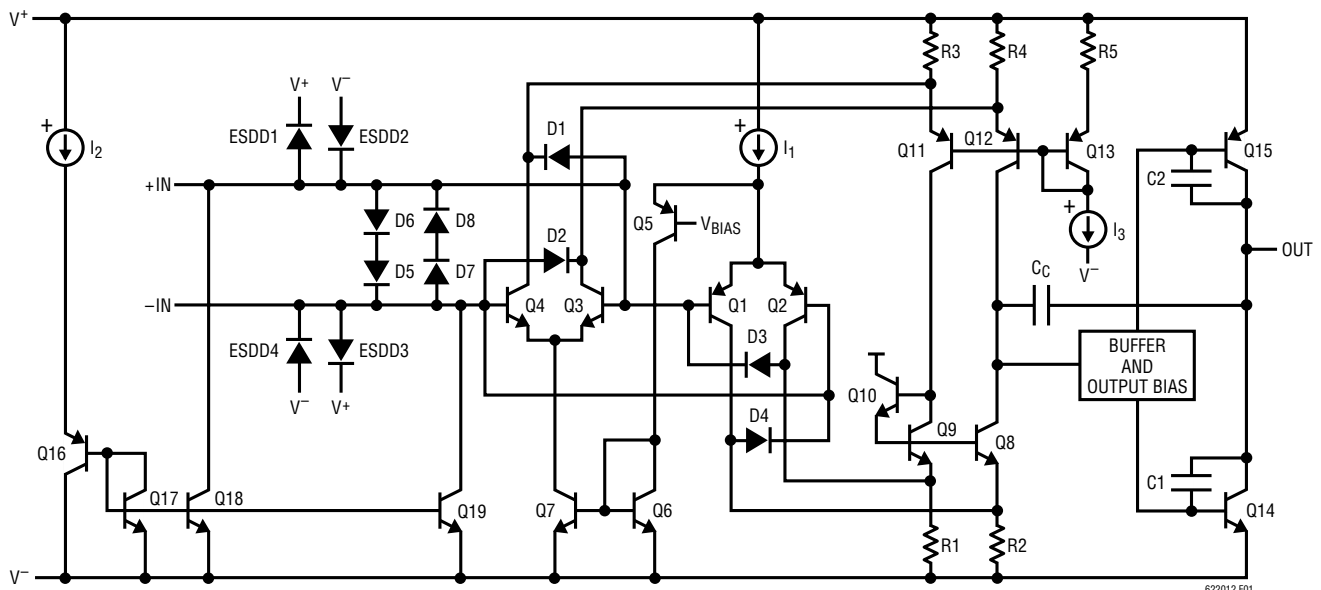
Figure 1. LT6220/LT6221/LT6222 Simplified Schematic Diagram

622012 F01

622012fa

13

APPLICATIONS INFORMATION

A pair of complementary common emitter stages Q14/Q15 that enable the output to swing from rail-to-rail construct the output stage. The capacitors C2 and C3 form the local feedback loops that lower the output impedance at high frequency. These devices are fabricated by Linear Technology's proprietary high speed complementary bipolar process.

Power Dissipation

The LT6222, with four amplifiers, is housed in a small 16-lead SSOP package and typically has a thermal resistance (θ_{JA}) of 135°C/W. It is necessary to ensure that the die's junction temperature does not exceed 150°C. The junction temperature, T_J, is calculated from the ambient temperature, T_A, power dissipation, P_D, and thermal resistance, θ_{JA}:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

The power dissipation in the IC is the function of the supply voltage, output voltage and the load resistance. For a given supply voltage, the worst-case power dissipation $P_{D(MAX)}$ occurs when the maximum supply current and the output voltage is at half of either supply voltage for a given load resistance. $P_{D(MAX)}$ is given by:

$$P_{D(MAX)} = \left(V_S \bullet I_{S(MAX)}\right) + \left(\frac{V_S}{2}\right)^2 / R_L$$

Example: For an LT6222 in a 16-lead SSOP package operating on ±5V supplies and driving a 100Ω load, the worst-case power dissipation is given by:

$$P_{D(MAX)}/Amp = (10 \bullet 1.8mA) + (2.5)^2 / 100$$
$$= 0.018 + 0.0625 = 80.5mW$$

If all four amplifiers are loaded simultaneously, then the total power dissipation is 322mW.

The maximum ambient temperature at which the part is allowed to operate is:

$$T_A = T_J - (P_{D(MAX)} \bullet 135°C/W)$$
$$= 150°C - (0.322W \bullet 135°C/W) = 106.5°C$$

Input Offset Voltage

The offset voltage will change depending upon which input stage is active. The PNP input stage is active from the negative supply rail to 1.2V below the positive supply rail, then the NPN input stage is activated for the remaining input range up to the positive supply rail during which the PNP stage remains inactive. The offset voltage is typically less than 70µV in the range that the PNP input stage is active.

Input Bias Current

The LT6220/LT6221/LT6222 employ a patent pending technique to trim the input bias current to less than 150nA for the input common mode voltage of 0.2V above the negative supply rail to 1.2V below the positive rail. The low input offset voltage and low input bias current of the LT6220/LT6221/LT6222 provide precision performance especially for high source impedance applications.

Output

The LT6220/LT6221/LT6222 can deliver a large output current, so the short-circuit current limit is set around 50mA to prevent damage to the device. Attention must be paid to keep the junction temperature of the IC below the absolute maximum rating of 150°C (refer to the Power Dissipation section) when the output is in continuous short circuit. The output of the amplifier has reverse-biased diodes connected to each supply. If the output is forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to several hundred milliamperes, no damage will occur to the device.

Overdrive Protection

When the input voltage exceeds the power supplies, two pair of crossing diodes, D1 to D4, will prevent the output from reversing polarity. If the input voltage exceeds either power supply by 700mV, diode D1/D2 or D3/D4 will turn on to keep the output at the proper polarity. For the phase reversal protection to perform properly, the input current must be limited to less than 5mA. If the amplifier is

APPLICATIONS INFORMATION

severely overdriven, an external resistor should be used to limit the overdriven current.

The LT6220/LT6221/LT6222's input stages are also protected against a large differential input voltage of 1.4V or higher by a pair of back-to-back diodes, D5/D8, to prevent the emitter-base breakdown of the input transistors. The current in these diodes should be limited to less than 10mA when they are active. The worse-case differential input voltage usually occurs when the input is driven while the output is shorted to ground in a unity-gain configuration. In addition, the amplifier is protected against ESD strikes up to 3kV on all pins by a pair of protection diodes on each pin that are connected to the power supplies as shown in Figure 1.

Capacitive Load

The LT6220/LT6221/LT6222 are optimized for high bandwidth, low power and precision applications. They can drive a capacitive load up to 100pF in a unity-gain configuration and more for higher gain. When driving a larger capacitive load, a resistor of 10Ω to 50Ω should be connected between the output and the capacitive load to avoid ringing or oscillation. The feedback should still be taken from the output so that the resistor will isolate the capacitive load to ensure stability. Graphs on capacitive loads show the transient response of the amplifier when driving capacitive load with specified series resistors.

Feedback Components

When feedback resistors are used to set up gain, care must be taken to ensure that the pole formed by the feedback resistors and the total capacitance at the inverting input does not degrade stability. For instance, the LT6220/LT6221/LT6222, set up with a noninverting gain of 2, two 5k resistors and a capacitance of 5pF (part plus PC board), will probably oscillate. The pole is formed at 12.7MHz that will reduce phase margin by 52 degrees when the crossover frequency of the amplifier is around 10MHz. A capacitor of 10pF or higher connecting across the feedback resistor will eliminate any ringing or oscillation.

TYPICAL APPLICATIONS

Stepped-Gain Photodiode Amplifier

The circuit of Figure 2 is a stepped gain transimpedance photodiode amplifier. At low signal levels, the circuit has a high 100kΩ gain, but at high signal levels the circuit automatically and smoothly changes to a low 3.2kΩ gain. The benefit of a stepped gain approach is that it maximizes dynamic range, which is very useful on limited supplies. Put another way, in order to get 100kΩ sensitivity and still handle a 1mA signal level without resorting to gain reduction, the circuit would need a 100V negative voltage supply.

The operation of the circuit is quite simple. At low photodiode currents (below 10μA) the output and inverting input of the op amp will be no more than 1V below ground. The LT1634 in parallel with R3 and Q2 keep a constant current though Q2 of about 20μA. R4 maintains quiescent current through the LT1634 and pulls Q2's emitter above

ground, so Q1 is reverse biased and no current flows through R2. So for small signals, the only feedback path is R1 (and C1) and the circuit is a simple transimpedance amplifier with 100kΩ gain.
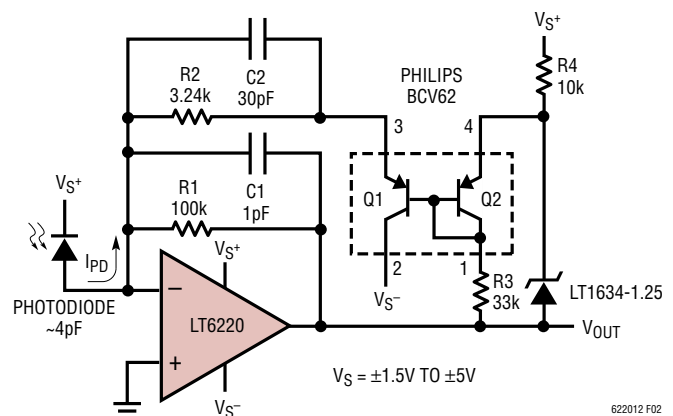
Figure 2. Stepped-Gain Photodiode Amplifier

622012fa

PACKAGE DESCRIPTION

As the signal level increases though, the output of the op amp goes more negative. At 12.5µA of photodiode current, the 100kΩ gain dictates that the LT6220 output will be about 1.25V below ground. However, at that point the emitter of Q2 will be at ground, and the base of Q1 will be 1V below ground. Thus, Q1 turns on and photodiode current starts to flow through R2. The transimpedance gain is therefore now reduced to R1||R2, or about 3.1kΩ. The circuit response is shown in Figure 3. Note the smooth transition between the two operating gains, as well as the linearity.
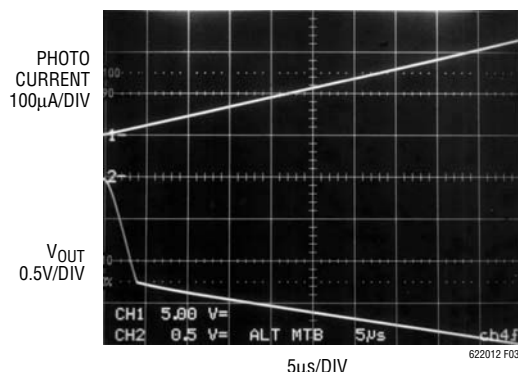
Figure 3. Stepped-Gain Photodiode Amplifier Response

Single 3V Supply, 1MHz, 4th Order Butterworth Filter

The circuit shown in Figure 4 makes use of the low voltage operation and the wide bandwidth of the LT6221 to create a DC accurate 1MHz 4th order lowpass filter powered from a 3V supply. The amplifiers are configured in the inverting mode for the lowest distortion and the output can swing rail-to-rail for maximum dynamic range. Figure 5 displays the frequency response of the filter. Stopband attenuation is greater than 100dB at 50MHz.

Figure 5. Frequency Response of Filter

Differential-In/Differential-Out Amplifier

The circuit of Figure 6 shows the LT6222 applied as a buffered differential-in differential-out amplifier with a gain of 2. Op amps A and B are configured as simple unity-gain buffers, offering high input impedance to upstream circuitry. Resistors R1 and R2 perform an averaging function on the common mode input voltage and R3 attenuates it by a factor of 2/3 and references it to the voltage source V_{OCM}. The resultant voltage, $V_{MID} = 2/3 \cdot V_{ICM}$, is placed at the noninverting inputs of op amps C and D. The other four resistors set gains of +3 from the noninverting input and –2 through the inverting path. Thus the output voltage of the upper path is:

$$-OUT = 3 \cdot (2/3 \cdot V_{ICM} + 1/3 \cdot V_{OCM}) - 2$$
$$\cdot (V_{ICM} + V_{DIFF}/2)$$
$$= 2V_{ICM} + V_{OCM} - 2V_{ICM} - V_{DIFF}$$
$$= V_{OCM} - V_{DIFF}$$

Figure 4. 3V, 1MHz, 4th Order Butterworth Filter

622012fa

16

PACKAGE DESCRIPTION

and the output of the lower path is:

$$+OUT = 3 \cdot (2/3 \cdot V_{ICM} + 1/3 \cdot V_{OCM}) - 2$$
$$\cdot (V_{ICM} - V_{DIFF}/2)$$
$$= 2V_{ICM} + V_{OCM} - 2V_{ICM} + V_{DIFF}$$
$$= V_{OCM} + V_{DIFF}$$

Note that the input common mode voltage does not appear in the output as either a common mode or a difference mode term. However the voltage V_{OCM} does appear in the output terms, and with the same polarity, so it sets up the output DC level. Also, the differential input voltage V_{DIFF} appears fully at both outputs with opposite polarity, giving rise to the effective differential gain of 2. Calculations show that using 1% resistors gives worst-case input common mode feedthrough better than –31dB, whether looking at the output common mode or difference mode. Considering the 6dB of gain, worst-case common mode rejection ratio is 37dB. (Remember this is assuming 1% resistors. Of course, this can be improved with more precise resistors.) Results achieved on the bench with typical 1% resistors showed 67dB of CMRR at low frequency and 40dB CMRR at 1MHz. Gains other than 2 can be achieved by setting $R3 = \alpha \cdot (R1||R2)$, $R5 = \alpha \cdot R4$ and $R7 = \alpha \cdot R6$ where gain = α.

PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

BOTTOM VIEW—EXPOSED PAD

(DD8) DFN 1203

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

S5 Package
5-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1635)

0.62 MAX

0.95 REF

1.22 REF

3.85 MAX   2.62 REF

1.4 MIN

RECOMMENDED SOLDER PAD LAYOUT
PER IPC CALCULATOR

2.90 BSC
(NOTE 4)

2.80 BSC

1.50 – 1.75
(NOTE 4)

PIN ONE

0.95 BSC

0.30 – 0.45 TYP
5 PLCS (NOTE 3)

0.20 BSC

DATUM 'A'

0.30 – 0.50 REF

0.09 – 0.20
(NOTE 3)

0.80 – 0.90

1.00 MAX

0.01 – 0.10

1.90 BSC

S5 TSOT-23 0302

NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING

4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

622012fa

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

.050 BSC

.045 ±.005

.245 MIN

.160 ±.005

.030 ±.005 TYP

RECOMMENDED SOLDER PAD LAYOUT

.189 – .197
(4.801 – 5.004)
NOTE 3

8 7 6 5

.228 – .244
(5.791 – 6.197)

.150 – .157
(3.810 – 3.988)
NOTE 3

1 2 3 4

.010 – .020
(0.254 – 0.508) × 45°

.008 – .010
(0.203 – 0.254)

0° – 8° TYP

.016 – .050
(0.406 – 1.270)

.053 – .069
(1.346 – 1.752)

.004 – .010
(0.101 – 0.254)

.014 – .019
(0.355 – 0.483)
TYP

.050
(1.270)
BSC

NOTE:
1. DIMENSIONS IN $\frac{INCHES}{(MILLIMETERS)}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)

.045 ±.005

.254 MIN

.150 – .165

.0165 ±.0015

.0250 BSC

RECOMMENDED SOLDER PAD LAYOUT

.189 – .196*
(4.801 – 4.978)

.009
(0.229)
REF

16 15 14 13 12 11 10 9

.229 – .244
(5.817 – 6.198)

.150 – .157**
(3.810 – 3.988)

1 2 3 4 5 6 7 8

.015 ± .004
(0.38 ± 0.10) × 45°

.007 – .0098
(0.178 – 0.249)

0° – 8° TYP

.016 – .050
(0.406 – 1.270)

.0532 – .0688
(1.35 – 1.75)

.004 – .0098
(0.102 – 0.249)

.008 – .012
(0.203 – 0.305)
TYP

.0250
(0.635)
BSC

GN16 (SSOP) 0204

NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{INCHES}{(MILLIMETERS)}$
3. DRAWING NOT TO SCALE
  *DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH
   SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
 **DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD
   FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

622012fa
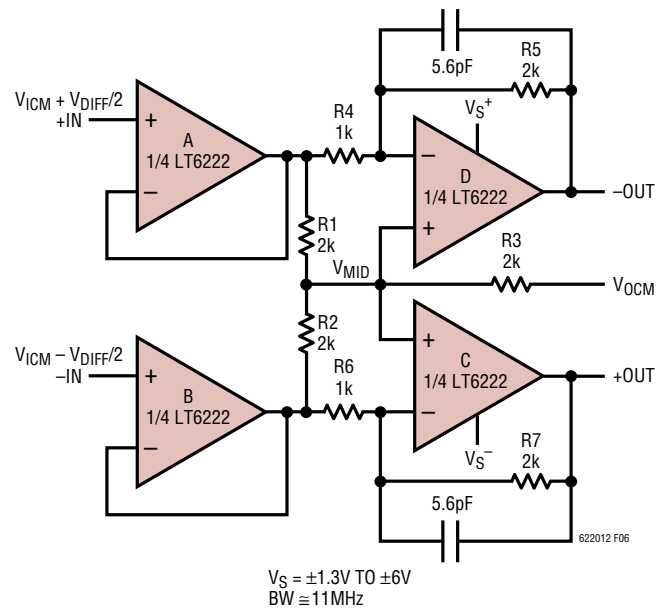
TYPICAL APPLICATION

$V_S = \pm1.3V$ TO $\pm6V$
BW $\cong$ 11MHz

Figure 6. Buffered Gain of 2 Differential-In/Differential-Out Amplifier

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1498/LT1499	Dual/Quad 10MHz, 6V/μs Rail-to-Rail Input/Output C_{LOAD} Op Amps	High DC Accuracy, 475μV $V_{OS(MAX)}$ Max Supply Current 2.2mA/Amp, Wide Supply Range, 2.2V to 30V
LT1800/LT1801/LT1802	Single/Dual/Quad 80MHz, 25V/μs, Low Power Rail-to-Rail Input/Output Precision Op Amps	350μV $V_{OS(MAX)}$, 250nA $I_{BIAS(MAX)}$, Max Supply Current 2mA/Amp
LT1803/LT1804/LT1805	Single/Dual/Quad 85MHz, 100V/μs Rail-to-Rail Input/Output Op Amps	2mV $V_{OS(MAX)}$, Max Supply Current 3mA/Amp
LT1806/LT1807	Single/Dual 325MHz, 140V/μs Rail-to-Rail Input/Output Op Amps	High DC Accuracy, 550μV $V_{OS(MAX)}$ Max Low Noise 3.5nV/$\sqrt{Hz}$ Low Distortion –80dBc at 5MHz, Power Down (LT1806)
LT1809/LT1810	Single/Dual 180MHz, Rail-to-Rail Input/Output Op Amps	350V/μs Slew Rate, Low Distortion –90dBc at 5MHz, Power Down (LT1809)