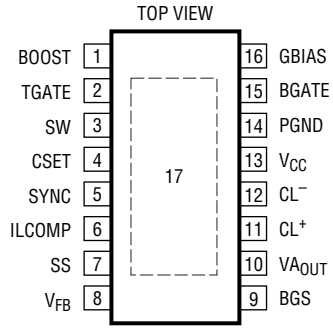
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} Supply Voltage 26V
BOOST Pin Voltage With Respect to SW pin 10V
BOOST Pin Voltage With Respect to GND pin 35V
SYNC Pin Voltage 30V
Operating Junction Temperature Range
(Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Note: If higher than 30V on SYNC pin is needed, add a 10k resistor in series with the pin.

PACKAGE/ORDER INFORMATION



FE PACKAGE
16-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 38°C/W

EXPOSED PAD IS SGND (PIN 17) MUST BE CONNECTED TO PGND AND SOLDERED TO PCB

ORDER PART NUMBER
LT3710EFE
FE PART MARKING
3710EFE

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 11V, operating maximum V_{CC} = 24V, no load on any outputs unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Overall						
Supply Voltage (V_{CC})		●	8		24	V
Supply Current (I_{VCC})	$VA_{OUT} \leq$ 1.2V (Switching Off)			7	12	mA
Boost Pin Current	$V_{BOOST} = V_{SW}$ + 8V, 0V ≤ V_{SW} ≤ 24V TGATE High TGATE Low			 2 2	 3 3	 mA mA
Voltage Amplifier VA						
Reference Voltage (V_{REF})		 ●	0.788 0.780	0.8	0.812 0.820	V V
FB Pin Input Current	$V_{FB} = V_{REF}$			0.2	0.5	µA
VA_{OUT} High				4.5		V
VA_{OUT} Low				0.8		V
VA_{OUT} Source Current		●	100		300	µA
Open-Loop Gain				100		dB
Gain Bandwidth Product				10		MHz
Soft-Start Current			5	12	18	µA
Current Limit Amplifier CA1						
Current Limit Threshold at ($V_{CL}^+ – V_{CL}^–$)	Common Mode Voltage from 0V to V_{CC} – 2.5V	●	50	70	85	mV
BGATE Off Threshold at ($V_{CL}^+ – V_{CL}^–$), BGS Pin Float	Common Mode Voltage from 0V to V_{CC} – 2.5V		0	8	15	mV
Switching Off Threshold at ILCOMP	V_{ILCOMP}				0.15	V
Input Current (CL^+, $CL^–$)	$V_{CL}^+ = V_{CL}^–$			100		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 11V, operating maximum V_{CC} = 24V, no load on any outputs unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator						
Switching Frequency	C_S = 500pF (No SYNC) C_S = 333pF (No SYNC)	● ●	170 240	200 280	240 340	kHz kHz
Synchronization Frequency Range	C_S = 500pF C_S = 333pF	● ●	245 345		400 500	kHz kHz
CSET Ramp Valley Voltage	C_S = 1000pF (No SYNC)		0.90	1.15	1.4	V
CSET Peak-to-Peak Voltage	C_S = 1000pF (No SYNC)			2.4		V
Synchronization Pulse Threshold on SYNC Pin	Falling Edge V_{SYNC}			2.5		V
Maximum Duty Cycle	$V_{FB} = V_{REF} - 5mV$, C_S > 500pF	●	85	90		%
Gate Drivers (TGATE, BGATE)						
V_{GBIAS}	I_{GBIAS} < 25mA	●	7.5	8.0	8.5	V
V_{TGATE} High ($V_{TGATE} - V_{SW}$)	I_{TGATE} < 50mA, $V_{BOOST} = V_{GBIAS} - 0.5V$	●	5	6	7	V
V_{BGATE} High	I_{BGATE} < 50mA	●	5	6	7.5	V
V_{TGATE} Low ($V_{TGATE} - V_{SW}$)	I_{TGATE} < –50mA	●			0.5	V
V_{BGATE} Low	I_{BGATE} < –50mA	●			0.5	V
Peak Gate Drive Current	10nF Load			1		A
Gate Drive Rise and Fall Time	1nF Load			25		ns

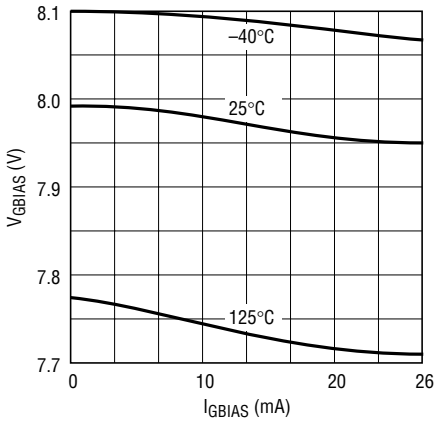
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LT3710E is guaranteed to meet performance specifications from 0°C to 125°C. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

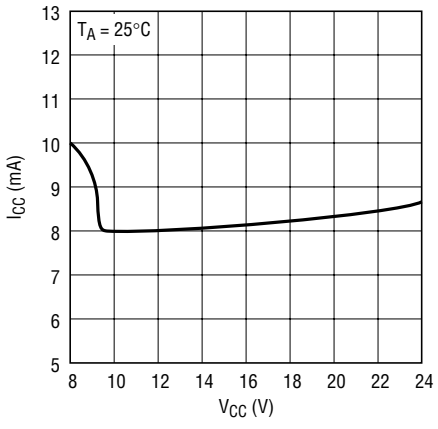
Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

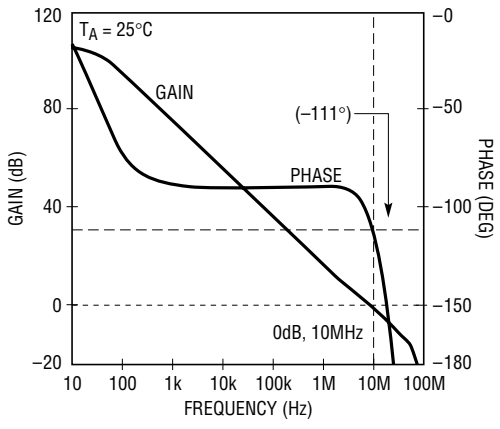
V_{GBIAS} vs I_{GBIAS} over Junction Temperature



I_{CC} vs V_{CC} (Switching Off)

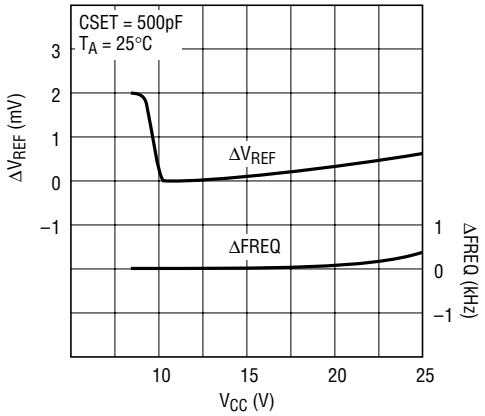


Voltage Amplifier VA Gain and Phase

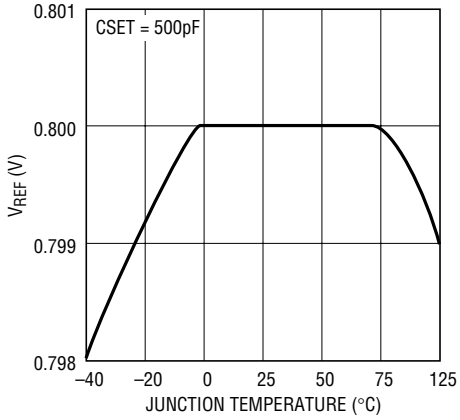


TYPICAL PERFORMANCE CHARACTERISTICS

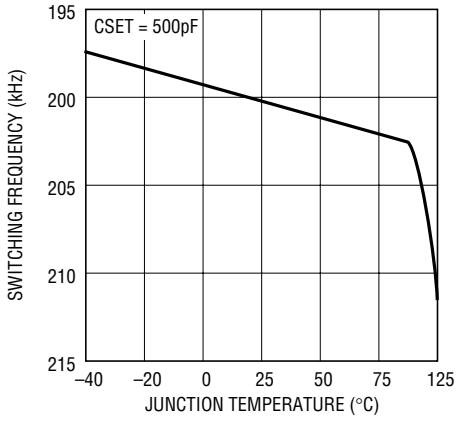
ΔV_{REF} vs V_{CC}, ΔFREQ vs V_{CC}



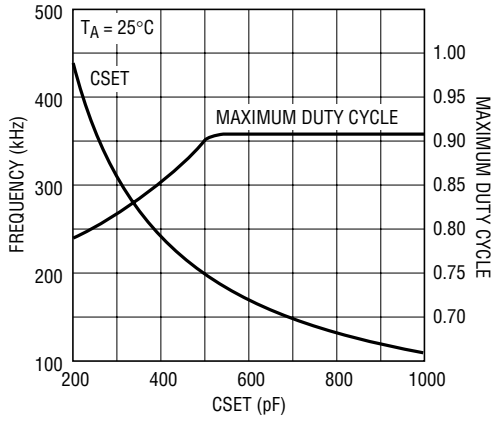
V_{REF} vs Temperature



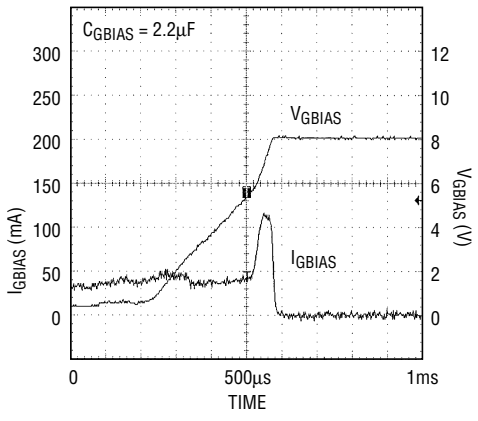
Frequency vs Temperature



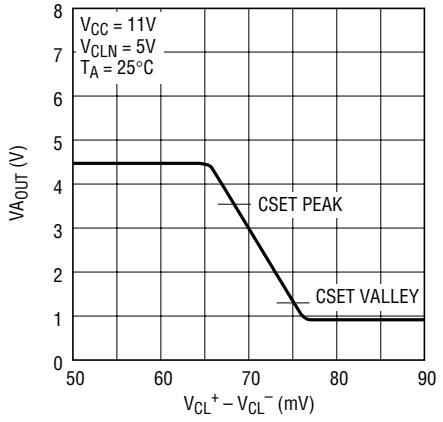
CSET vs Switching Frequency



G_{BIAS} vs I_{GBIAS} (Charging 2.2µF)



Current Limit Amplifier CA1 Gain at V_{CC} = 11V, V_{CL}^- = 5V



PIN FUNCTIONS

BOOST (Pin 1): Topside (Boosted) Driver Supply. This pin is used to bootstrap and supply the topside power switch gate drive circuitry. In normal operation V_{BOOST} is powered from the internally generated 8V GBIAS, $V_{BOOST} = V_{SW} + 8.2V$ when TGATE is on.

TGATE (Pin 2): Topside (Boosted) N-Channel MOSFET Driver. When TGATE is on, the voltage is equal to $V_{SW} + 6V$.

SW (Pin 3): Switch Node Connection to Inductor.

CSET (Pin 4): Oscillator Timing Pin. The capacitor on this pin sets the PWM switching frequency.

SYNC (Pin 5): Synchronization Input. This pin should be connected to the secondary side output of the power transformer with a series resistor. A filtering capacitor of 10pF is recommended.

ILCOMP (Pin 6): Current Limit Amplifier Compensation Node. At current limit, CA1 pulls down on this pin to regulate the output current.

SS (Pin 7): Soft-Start. A capacitor on this pin sets the output ramp up rate. The typical time for SS to reach the programmed level is (C • 0.8V)/10μA.

V_{FB} (Pin 8): Voltage Amplifier Inverting Input. A resistor divider to this pin sets the output voltage. Nominal voltage at this pin is 0.8V.

BGS (Pin 9): Bottom Gate Switching Control. CA2 monitors the inductor current and prohibits BGATE from turning on when the inductor current is low (below 8mV across the current sense resistor RS1) to allow discontinous mode operation. Grounding this pin disables comparator CA2.

VA_{OUT} (Pin 10): Voltage Amplifier Output.

CL^+ (Pin 11): Current Limit Amplifier Positive Input. The threshold is set at 70mV.

CL^- (Pin 12): Current Limit Amplifier Negative Input. When used, CL^- is connected to the output capacitor side of the current + sense resistor and CL^+ is connected to the inductor side of the current sense resistor.

V_{CC} (Pin 13): Supply of the IC. For proper bypassing, a low ESR capacitor is required.

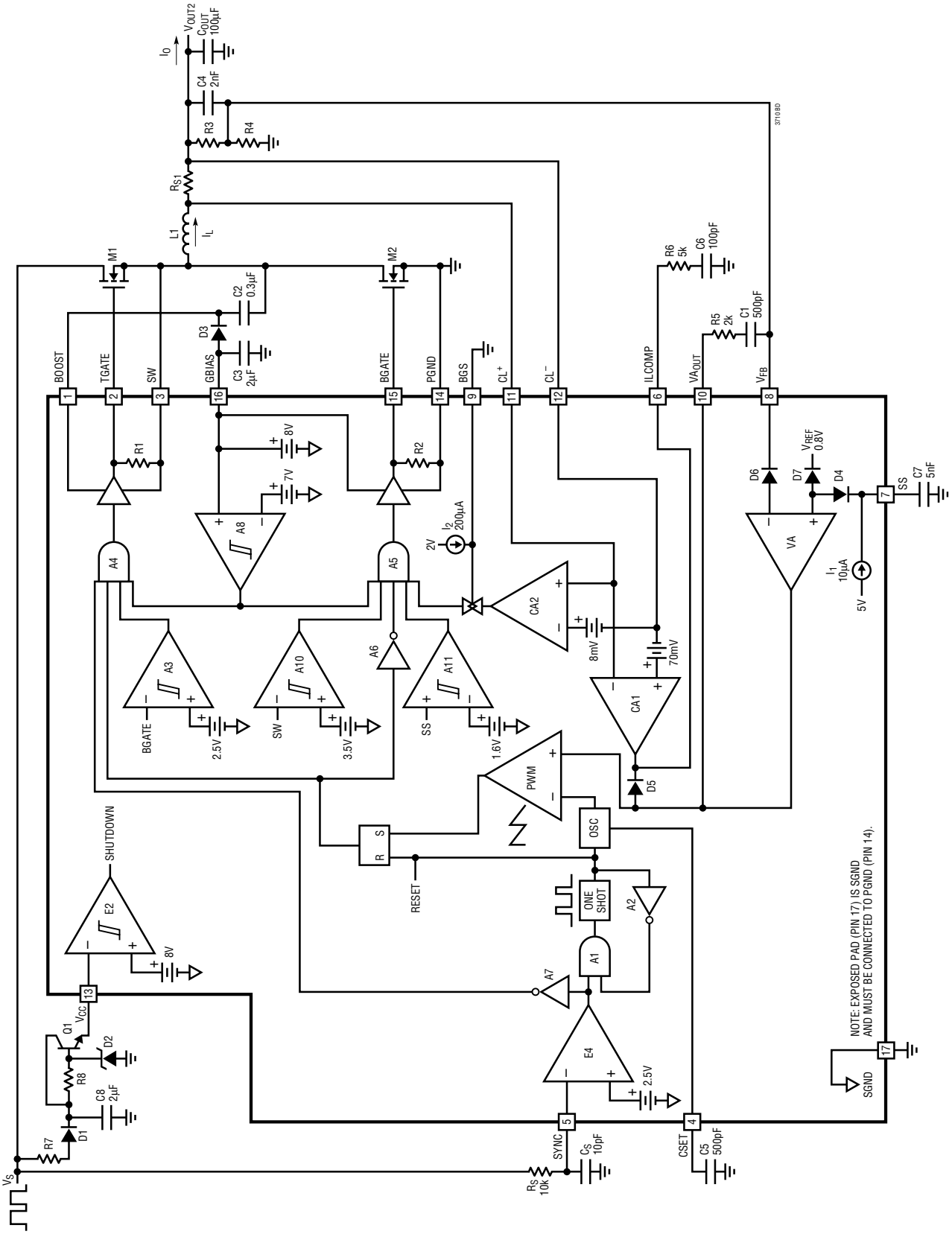
PGND (Pin 14): Ground of the Bottom Side N-Channel MOSFET Driver.

BGATE (Pin 15): Bottom Side N-Channel MOSFET Driver.

GBIAS (Pin 16): 8V Regulator Output for Boostrapping V_{BOOST}. A bypass capacitor of at least 2μF is needed.

Exposed Pad (Pin 17): Connect to PGND (Pin 14).

BLOCK DIAGRAM



OPERATION

To generate isolated multiple outputs, most systems use either multiple secondary windings or cascade regulators for each additional output. Multiple secondary windings sacrifice regulation of the auxiliary outputs. Cascaded regulators require a larger inductor for the main output, because all of the power is processed in series.

By generating the auxiliary output(s) from the secondary winding of the main output, the LT3710 allows for parallel processing of the output power. This minimizes the main output inductor size and directly regulates the auxiliary output. With synchronous rectification, the system efficiency is greatly improved.

Refering to the Block Diagram, the LT3710 basic functions include a voltage amplifier, VA, to regulate the output voltage to within typically 1.5%, a voltage mode PWM with trailing edge synchronization and leading edge modulation, a current limit amplifier, CA1, and high speed synchronous switch drivers.

During normal operation (see Figure 2), a switching cycle begins at the falling edge of the transformer secondary voltage V_S. The internal oscillator is reset, turning off the top MOSFET M1 and turning on the bottom MOSFET M2. During this portion of the cycle, the inductor current is discharged by the output voltage V_{OUT2}. The transformer secondary voltage V_S will go high during this portion of the cycle. Since M1 is off, the switch node voltage V_{SW} remains zero. The inductor current continues to be discharged by the output voltage V_{OUT2}. This condition lasts until the ramp signal intersects the feedback error amplifier output VA_{OUT}. The top MOSFET M1 turns on, pulling the switch node voltage to V_S. The inductor current of the LT3710 circuit is then charged by $V_S - V_{OUT2}$. The effective on time of this buck circuit ends when the secondary voltage becomes zero. The next cycle repeats.

The ideal equation for duty cycle of the LT3710 is:

$$D2 = V_{OUT2}/V_{SP}$$

where V_{OUT2} is the auxiliary output voltage, V_{SP} is the amplitude of the secondary voltage and D2 is the duty cycle of the switching node voltage V_{SW}, as defined in Figure 2.

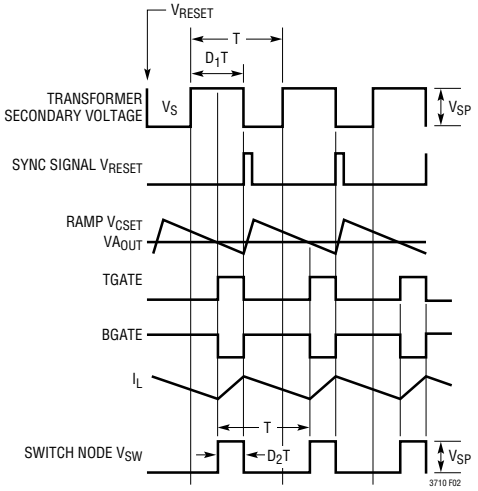


Figure 2. Leading Edge Modulation, Trailing Edge Synchronization

APPLICATIONS INFORMATION

Synchronization and Oscillation Frequency Setting

The switching is synchronized to the secondary winding falling edge and the synchronization threshold is typically 2.5V. The synchronization falling edge triggers an internal inverted ramp (see Figure 2) and starts a new switching cycle for the leading edge voltage mode PWM. The reason for using leading edge modulation is to keep the transformer primary side peak current sensing undisturbed.

For proper synchronization, the oscillator frequency should be set lower than the system switching frequency with tolerances taken into account.

$$f_{OSC} < (f_{SL} \bullet 0.8)$$

f_{SL} is the low limit of the system switching frequency and 0.8 is the tolerance of f_{OSC}.

For example, a system of 200KHz with 15% tolerance, then f_{SL} = 200k • 85% = 170kHz; and f_{OSC} < (170k • 0.8), f_{OSC} should be set below 136kHz.

Once f_{OSC} is determined, CSET can be calculated by CSET = $(107250pf/f_{OSC(kHz)}) - 50pF$.

For f_{OSC} = 100kHz, CSET = 1022.5pF.

APPLICATIONS INFORMATION

Output N-Channel MOSFET Drivers

The LT3710 employs high speed N-channel MOSFET synchronous drivers to achieve high system efficiency. GBIAS is the 8V regulator output to bias and supply the drivers and should be properly bypassed with a low ESR capacitor to ground plane. A Schottky catch diode is required on the switch node.

Light Load Operation

If the BGS pin is grounded, the LT3710 stays in continuous mode independent of load condition except in soft-start operation (see Soft-Start section). If the BGS pin is left open, under light load and V_{RS1} drops below 8mV, BGATE will be turned off(see comparator CA2 of Block Diagram) and the LT3710 goes into discontinous mode operation.

Current Limit

Current limit is set by the 70mV threshold across CL^+ and CL^-, the inputs of the amplifier CA1. By connecting an external resistor RS1(see Block Diagram), the current limit is set for $70mV/R_{S1}$. R6 and C6 stablize the current limit loop. If current limit is not used, both CL^+ and CL^- should be grounded and the BGS pin should also be grounded to disable comparator CA2.

Soft-Start and Shutdown

During soft-start, V_{SS} is the reference voltage that controls the output voltage and the output ramps up following V_{SS}. The effective range of V_{SS} is from 0V to V_{REF}. The typical time for the output to reach the programmed level is $(C \bullet 0.8V)/10\mu A$.

During start up, BGATE will stay off until V_{SS} gets up to 1.6V. This prevents the bottom MOSFET from turning on if the output is precharged.

To shut down the LT3710, the SS pin should be pulled below 50mV by a VN2222 type N-channel transistor. Note that during shutdown BGATE will be locked off when V_{SS} drops below 0.6V. This prevents the bottom MOSFET from discharging the output, which would cause the output to undershoot below ground.

Layout Considerations

For maximum efficiency, the switching rise and fall times are less than 20ns. To prevent radiation, the power MOSFETs, SW pin and input bypass capacitor leads should be kept as short as possible. A ground plane should be used under the switching circuitry to prevent interplane coupling and to act as a thermal spreading path. Note that the bottom metal of the package is the heat sink, as well as the IC signal ground, and must be soldered to the ground plane.

Output Voltage Programming

The feedback reference voltage is 0.8V. The output voltage can be easily programmed by the resistor divider, R3 and R4, as shown in the Block Diagram.

$$V_{OUT2} = 0.8 \bullet \left(1 + \frac{R3}{R4}\right)$$

Filtering on the SYNC Input

It is necessary to add RC filtering on the SYNC input of the LT3710 to eliminate the negative glitch at the turn on of the top MOSFET. When the top MOSFET M1 turns on, the transformer secondary current instantly changes from the original first output inductor current to the sum of two output inductor currents. The high di/dt on the transformer leakage inductance causes the transformer secondary voltage V_S to drop for a short interval. If the leakage inductance is large enough, the V_S dip will be lower than the synchronization threshold (about 2.5V), falsely triggering the synchronization. The top MOSFET is turned off immediately. As a result, the output voltage will not be regulated properly.

A filter circuit is needed to ensure proper operation. A small RC filter with R_S = 10k and C_S = 10pF are typical.

APPLICATIONS INFORMATION

Output Inductor Selection

The key parameters for choosing the inductor include inductance, RMS and saturation current ratings and DCR. The inductance must be selected to achieve a reasonable value of ripple current, which is determined by:

$$\Delta I_L = \frac{V_{OUT2} \bullet (1 - D2)}{f \bullet L}$$

Typically, the inductor ripple current is designed to be 20% to 40% of the maximum output current.

The RMS current rating must be high enough to deliver the maximum output current. A sufficient saturation current rating should prevent the inductor core from saturating. These two current ratings can be determined by:

$$I_{RMS} \geq \sqrt{I_O^2 + \frac{\Delta I_{LMAX}^2}{12}}$$

$$I_{SAT} \geq I_O + \frac{\Delta I_{LMAX}}{2}$$

where I_O is the maximum output current and ΔI_{LMAX} is the maximum peak-to-peak inductor ripple current.

To optimize the efficiency, we usually choose the inductor with the minimum DCR if the inductance and current ratings are the same.

Power MOSFET Selection

The LT3710 drives two external N-channel MOSFETs to deliver high currents at high efficiency. The gate drive voltage is typically 6.5V. The key parameters for choosing MOSFETs include drain to source voltage rating V_{DSS} and $R_{DS(ON)}$ at 6.5V gate drive. Note that the transformer secondary voltage waveform will overshoot at its rising edge due to the ringing between transformer leakage inductance and parasitic capacitance. The V_{DSS} of both top and bottom MOSFETs must be sufficiently higher than the maximum overshoot. It is recommended that an RC snubber or a voltage clamping circuitry be placed across the transformer secondary winding to limit the V_S overshoot.

The $R_{DS(ON)}$ of the MOSFETs should be selected to deliver the required current at the desired efficiency as well as to meet the thermal requirement of the MOSFET package. The conduction power losses of the MOSFETs are:

$$P_{M1} \cong I_O^2 \bullet R_{DS(ON)M1} \bullet D2$$

$$P_{M2} \cong I_O^2 \bullet R_{DS(ON)M2} \bullet (1 - D2)$$

where I_O is the maximum output current of LT3710 circuit, $R_{DS(ON)M1}$ and $R_{DS(ON)M2}$ are the on-resistance for the top and bottom MOSFETs, respectively. The $R_{DS(ON)}$ must be determined with 6.5V gate drive and the expected operating temperature.

A good number of high performance power MOSFET selections are available from Siliconix, International Rectifier and Fairchild. If the V_{DSS} and $R_{DS(ON)}$ ratings are the same, the MOSFETs with the lowest gate charge Q_G should be chosen to minimize the power loss associated with the MOSFET gate drives, the switching transitions and the controller bias supply.

Output Capacitor Selection

The selection of the output capacitor is determined by the output ripple and load transient requirements. In low output voltage applications, always choose capacitors with low ESR. The output ripple voltage is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

where ΔI_L is the inductor peak-to-peak ripple current.

A partial list of low ESR high performance capacitor types includes SP capacitors from Panasonic and Cornell Dubilier, POSCAPs and OS-CON capacitors from Sanyo, T510 and T520 surface mount capacitors from Kemet.

Design Example

Figure 3 shows an application example for the LT3710. It is a dual output, high efficiency, isolated DC/DC power supply with 36V to 72V input, 3.3V/10A and 1.8V/10A outputs. The basic power stage topology is a 2-transistor

APPLICATIONS INFORMATION

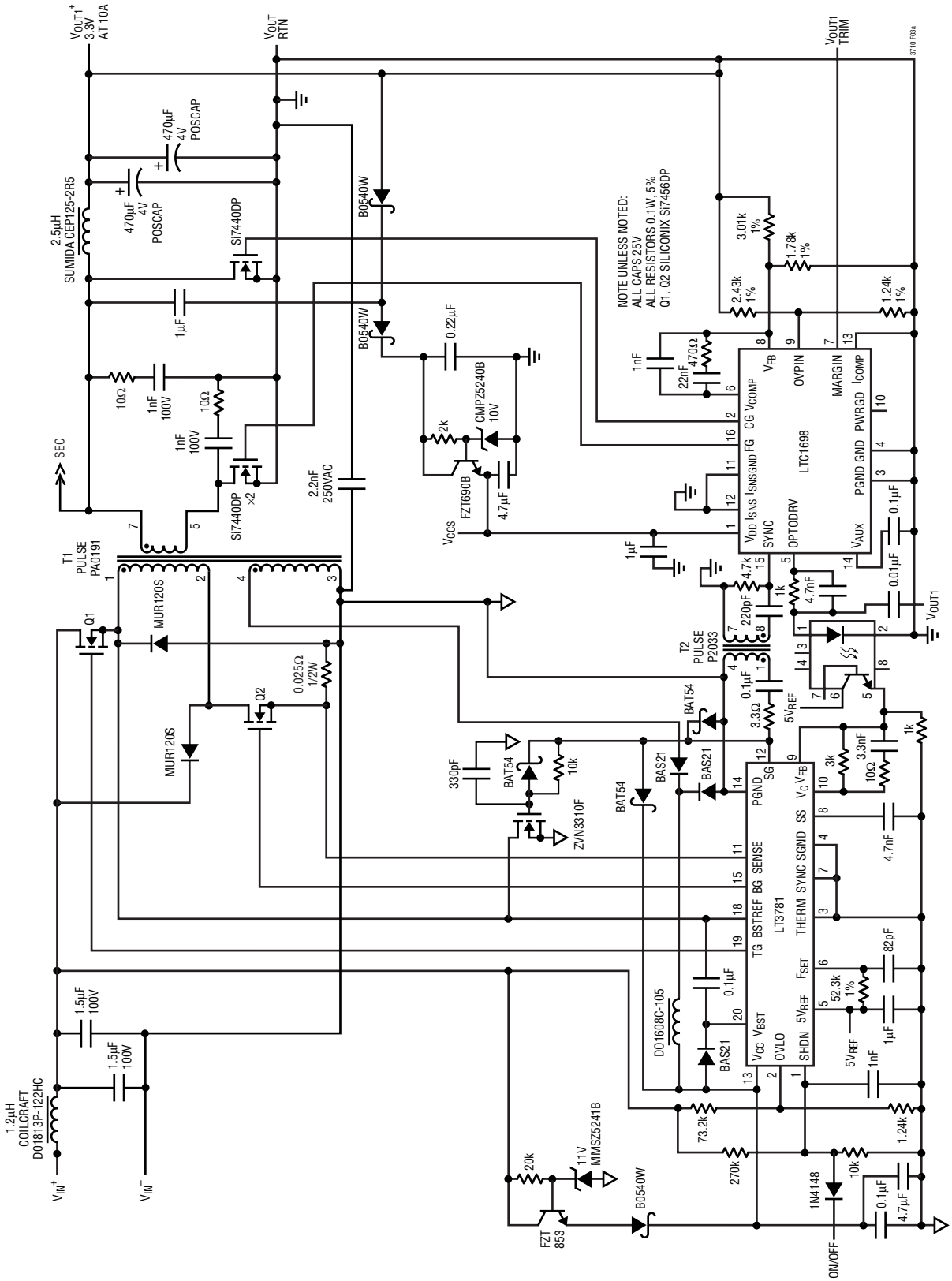


Figure 3a. 36V to 72V DC to 3.3V/10A and 1.8V/10A (or 2.5V/10A) Dual Output Isolated Power Supply-Basic Circuit (Part 1 of 2, See Next Page)

APPLICATIONS INFORMATION

forward converter with synchronous rectification. The primary side controller uses an LT3781, a current mode 2-transistor forward controller with built-in MOSFET drivers. On the secondary side, an LTC1698 is used to provide the voltage feedback for the 3.3V output, as well as the gate drive for the synchronous MOSFETs. The error amplifier output is fed into the optocoupler and then relayed to LT3781 on the primary side to complete the 3.3V regulation. The 1.8V output is generated by the LT3710 circuit. A planar transformer PA0191 built by Pulse Engineering is employed as the power transformer in this design. This transformer is constructed on a PQ20 core with a nine turn primary winding, two turn secondary winding and seven turn auxiliary winding for the LT3781 bias supply. Because the maximum secondary voltage V_{SP} is about 16V, 30V MOSFETs are chosen with the consideration that the secondary voltage overshoot is typically 20% to 30% of V_{SP}. In this particular design, Si7440DP is selected due to its low $R_{SD(ON)}$, 30V V_{DSS} rating and its compact and thermally enhanced PowerPak SO-8 package.

The switching frequency of the circuit is about 230kHz. 1500V input to output isolation is provided. Additional features of this design include primary side on/off control, ±5% secondary side trimming on the 3.3V output, input overvoltage protection and undervoltage lockout. The complete design will mount within a standard half brick PC board with about half inch height.

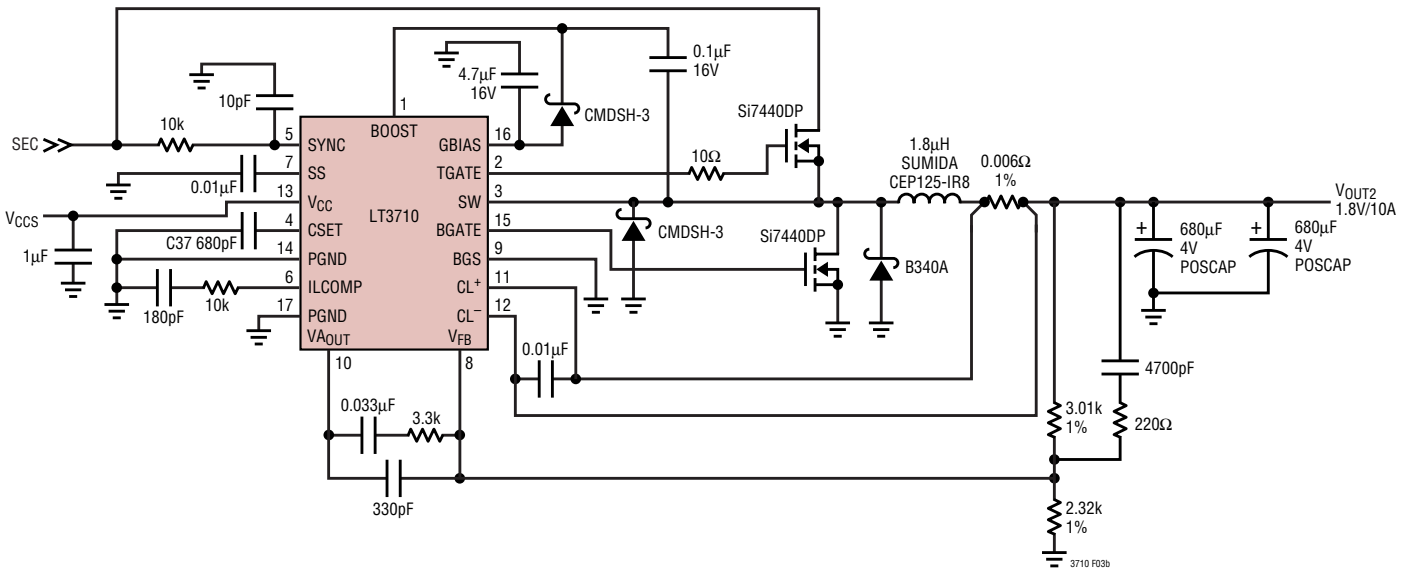
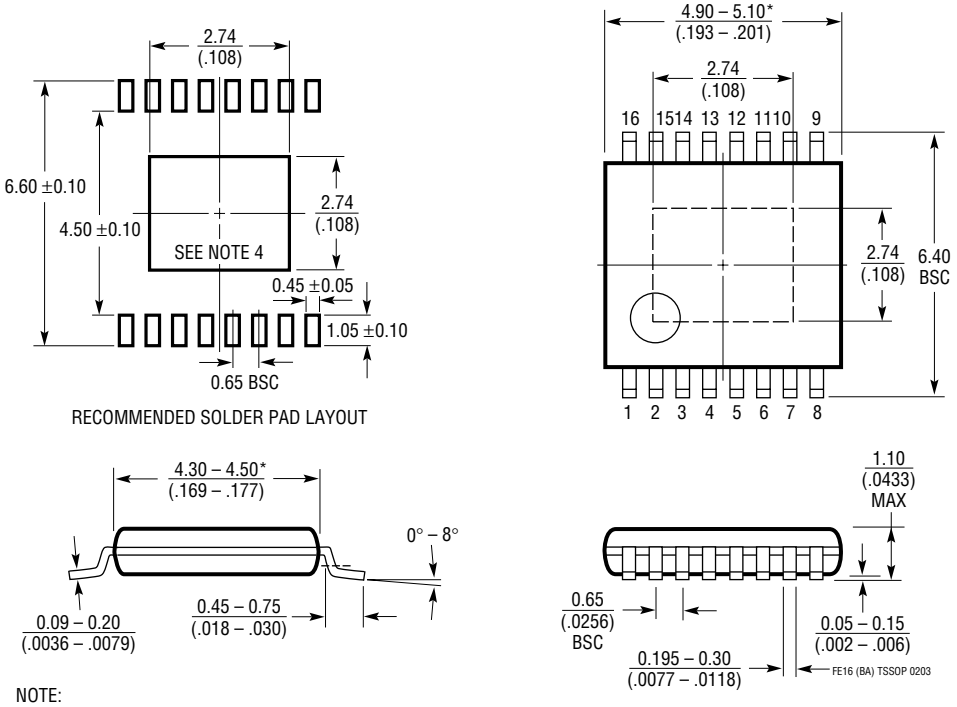


Figure 3b. 36V to 72V DC to 3.3V/10A and 1.8V/10A Dual Output Isolated Power Supply (Part 2 of 2, See Previous Page)

PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation BA



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1339	High Power Synchronous DC/DC Controller	Operation Up to 60V Maximum
LT1425	Isolated Flyback Switching Regulator	General Purpose with External Application Resistor
LT1431	Programmable Reference	0.4% Initial Voltage Tolerance
LT1680	High Power DC/DC Step-Up Controller	Operation Up to 60V Maximum
LT3781	Dual Transistor Synchronous Forward Controller	Operation Up to 72V Maximum
LT1725	General Purpose Isolated Flyback Controller	Drives External Power MOSFET with External I_{SENSE} Resistor
LT1737	High Power Isolated Flyback Controller	Sense Output Voltage Directly from Primary-Side Winding
LT1950	PWM Controller for Flyback, Forward and SEPIC Applications	15W to 500W, Isolated and Nonisolated Power Supply 50% Smaller Transformer, Protects MOSFET
LT3804	Secondary Side Dual Output Controller with Optodriver	Regulates Two Outputs, Optocoupler Feedback Driver and Second Output Synchronous Driver Controller

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT/TP 0803 1K • PRINTED IN USA