

LA6261

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 8\text{V}$, $V_{REF} = 1.65\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
All Blocks						
No-load current drain ON	I _{CC} -ON	All outputs on *1, FWD=REV=0V		30	50	mA
V _{REF} input voltage range	V _{REF} -IN		0.5		V _{CC} -1.5	V
BTL AMP						
Output offset voltage	V _{OFF}	BTL amplifier, the voltage difference between each channel outputs	-50		+50	mV
Input voltage range	V _{IN}	Applied to pins V _{IN} 1 to V _{IN} 4	0		V _{CC}	V
Output voltage	V _O	Voltage between V _O + and V _O - for each channel when R _L =8Ω *2	4	5		V
Closed-circuit voltage gain	V _G	The gain from the input to the output		4		deg
MUTE ON voltage	V _{MT} ON	*3	2		SV _{CC}	V
MUTE OFF voltage	V _{MT} OFF	*3	0		0.5	V
Slew rate	SR	For the independent amplifier. Times 2 when between outputs *4		0.5		V/μs
H-bridge Block						
Output voltage	V _O -LOAD	Voltage between V _O + and V _O - for each channel when R _L =10Ω	6.2	6.7		V
Input low level	V _{IN} -L		0		1	V
Input high level	V _{IN} -H		2		SV _{CC}	V
Output setting voltage	V _{CONT}	Voltage between V _O + and V _O - for each channel when V _{CONT} =3V and R _L =10Ω		2.8		V
Regulator Block						
Output voltage	V _{reg}	I _L =100mA	3.05	3.3	3.55	V
Output load variation	ΔV _{RL}	I _L =0 to 200mA	-50	0	10	mV
Supply voltage variation	ΔV _{VCC}	V _{CC} =6 to 12V, I _L =100mA	-15	21	60	mV

*1: The total current dissipation for SV_{CC} , PV_{CC1} , and PV_{CC2} with no load

*2: Output in the saturated state

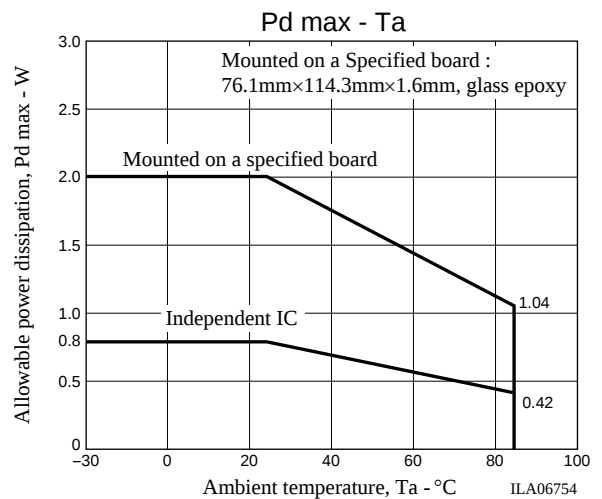
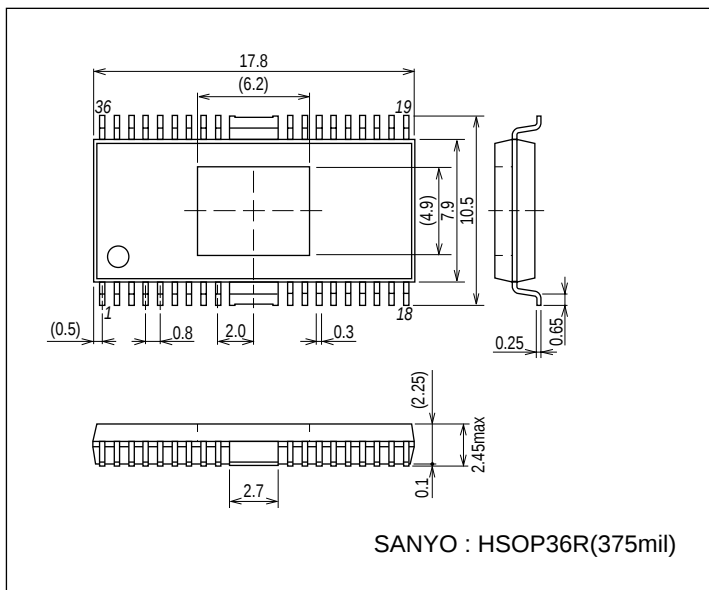
*3: When the MUTE pin is high, the BTL output will be on, and when low, the BTL output will be OFF (HI impedance).

*4: Design guarantee value

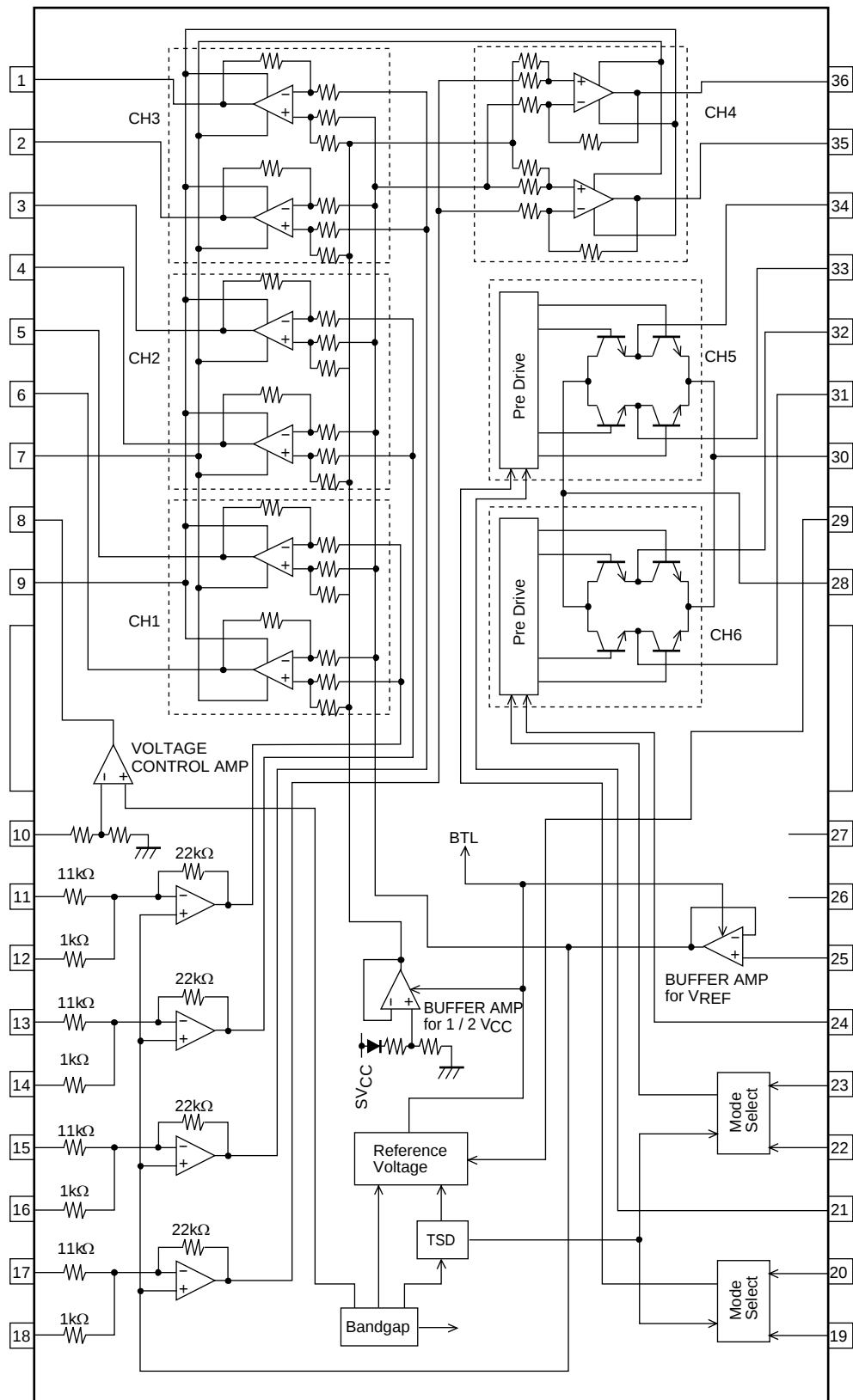
Package Dimensions

unit : mm (typ)

3251



Block Diagram



ILA06744

Pin Description

Pin No.	Pin Name	Description	Equivalent Circuit Diagram
1	V _{O3+}	Channel 3 (BTL) output (+)	
2	V _{O3-}	Channel 3 (BTL) output (-)	
3	V _{O2+}	Channel 2 (BTL) output (+)	
4	V _{O2-}	Channel 2 (BTL) output (-)	
5	V _{O1+}	Channel 1 (BTL) output (+)	
6	V _{O1-}	Channel 1 (BTL) output (-)	
7	PGND	Power system ground for channels 1 to 4 (BTL)	
9	PV _{CC1}	Power system power supply for channels 1 to 4 (BTL) (shorted to SV _{CC})	
35	V _{O4+}	Channel 4 (BTL) output (+)	
36	V _{O4-}	Channel 4 (BTL) output (-)	
8	REGIN	Regulator (to the base of the external PNP transistor)	
10	REGOUT	Regulator (to the collector of the external PNP transistor)	
11	V _{IN1}	Channel 1 input	
12	V _{IN1G}	Channel 1 input (gain adjustment)	
13	V _{IN2}	Channel 2 input	
14	V _{IN2G}	Channel 2 input (gain adjustment)	
15	V _{IN3}	Channel 3 input	
16	V _{IN3G}	Channel 3 input (gain adjustment)	
17	V _{IN4}	Channel 4 input	
18	V _{IN4G}	Channel 4 input (gain adjustment)	
19	FWD5	Channel 5 output direction switching (FWD), H-bridge logic input	
20	REV5	Channel 5 output direction switching (REV), H-bridge logic input	
22	FWD6	Channel 6 output direction switching (FWD), H-bridge logic input	
23	REV6	Channel 6 output direction switching (REV), H-bridge logic input	

Continued on next page.

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Pin No.	Pin Name	Description	Equivalent Circuit Diagram
21 24	VCONT5 VCONT6	Channel 5 output voltage setting Channel 6 output voltage setting	
25	VREFIN	Reference voltage input	
28 30 31 32 33 34	PVCC2 PGND2 VO6+ VO6- VO5+ VO5-	Power system power supply for for channels 5 and 6 (H-bridge) Power system ground for channels 5 and 6 (H-bridge) Channel 6 (H-bridge) output (+) Channel 6 (H-bridge) output (-) Channel 5 (H-bridge) output (+) Channel 5 (H-bridge) output (-)	
29	MUTE	BTL mute signal input	
26	SGND	Signal system ground	
27	SVCC	Signal system power supply (shorted to PVCC1)	

Truth Table

INPUT		OUTPUT	
FWD5(6)	REV5(6)	VO5(6)+	VO5(6)-
L	L	Z	Z
L	H	H	L
H	L	L	H
H	H	L	L

*Z: HI-Impedance



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