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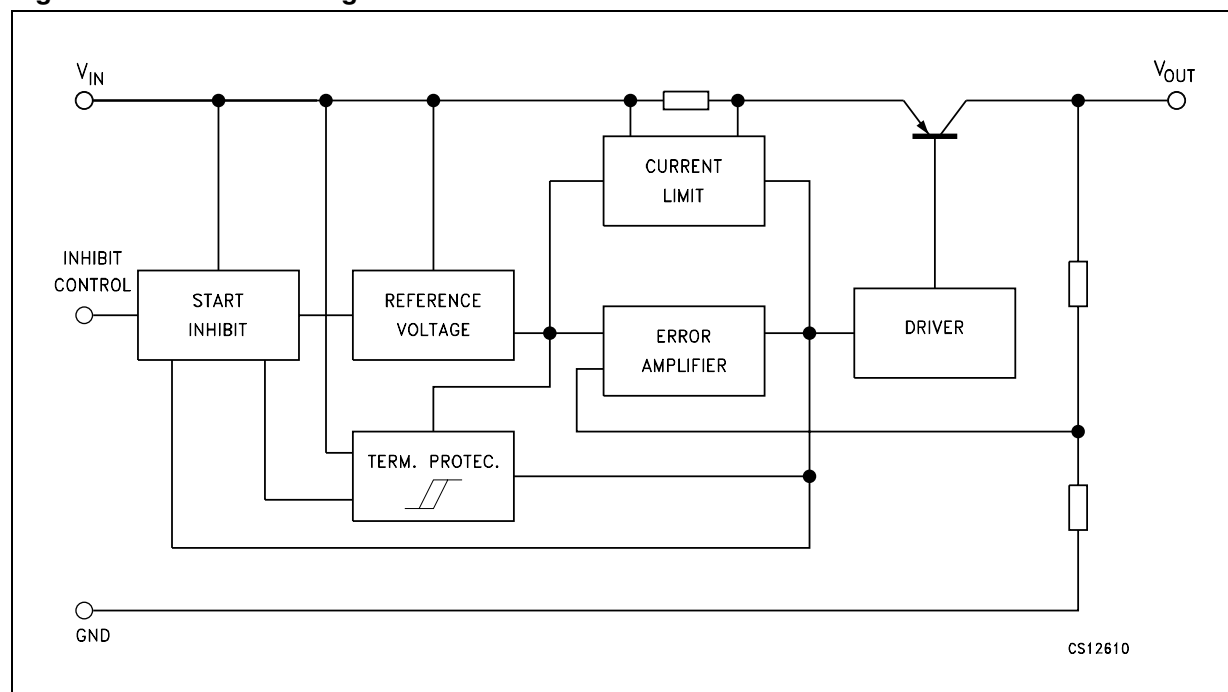
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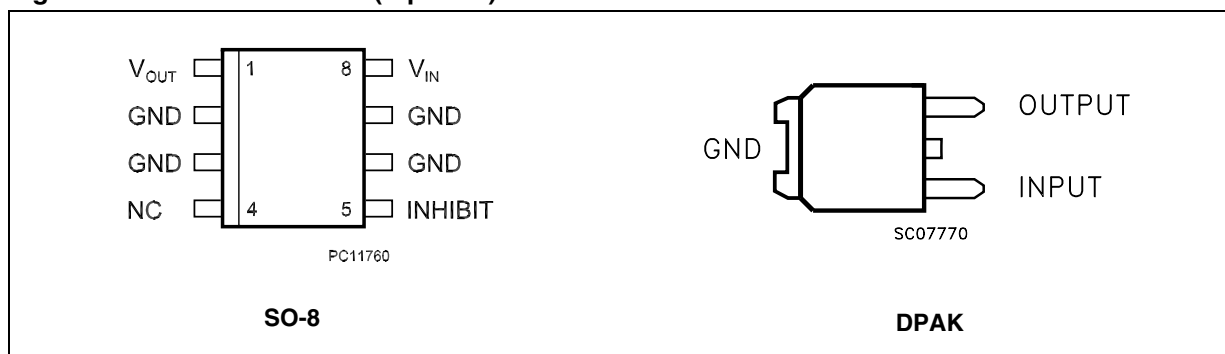
1 Diagram

Figure 1. Schematic diagram



2 Pin configuration

Figure 2. Pin connections (top view)



3 Maximum ratings

Table 2. Absolute maximum ratings

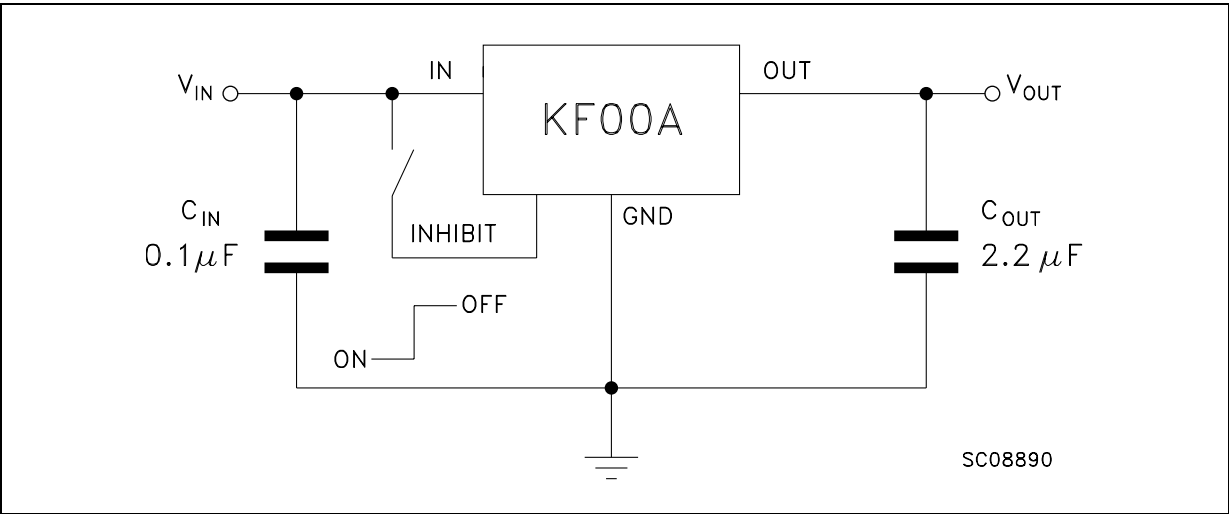
Symbol	Parameter	Value	Unit
V_I	DC input voltage	-0.5 to 20	V
I_O	Output current	Internally Limited	
P_{TOT}	Power dissipation	Internally Limited	
T_{STG}	Storage temperature range	-40 to 150	°C
T_{OP}	Operating junction temperature range	-40 to 125	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 3. Thermal data

Symbol	Parameter	DPAK	SO-8	Unit
R_{thJC}	Thermal resistance junction-case	8	20	°C/W

Figure 3. Test circuit



4 Electrical characteristics

Table 4. Electrical characteristics for KF15 (refer to the test circuits, $T_J = 25\text{ }^{\circ}\text{C}$, $C_I = 0.1\text{ }\mu\text{F}$, $C_O = 2.2\text{ }\mu\text{F}$ unless otherwise specified.)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	$I_O = 50\text{ mA}$, $V_I = 3.5\text{ V}$	1.47	1.5	1.53	V
		$I_O = 50\text{ mA}$, $V_I = 3.5\text{ V}$, $T_a = -25\text{ to }85^{\circ}\text{C}$	1.44		1.56	
V_I	Operating input voltage	$I_O = 500\text{ mA}$	2.5		20	V
I_O	Output current limit			1		A
ΔV_O	Line regulation	$V_I = 2.5\text{ to }20\text{ V}$, $I_O = 5\text{ mA}$		2	12	mV
ΔV_O	Load regulation	$V_I = 2.8\text{ V}$, $I_O = 5\text{ to }500\text{ mA}$		2	50	mV
I_d	Quiescent current	$V_I = 2.5\text{ to }20\text{ V}$, $I_O = 0\text{ mA}$	ON MODE	0.5	1	mA
		$V_I = 2.8\text{ to }20\text{ V}$, $I_O = 500\text{ mA}$			12	
		$V_I = 6\text{ V}$	OFF MODE	50	100	μA
SVR	Supply voltage rejection	$I_O = 5\text{ mA}$, $V_I = 3.5 \pm 1\text{ V}$	$f = 120\text{ Hz}$	82		dB
			$f = 1\text{ kHz}$	77		
			$f = 10\text{ kHz}$	60		
eN	Output noise voltage	$B = 10\text{ Hz to }100\text{ kHz}$		50		μV
V_d	Dropout voltage	$I_O = 200\text{ mA}$		1		V
V_{IL}	Control input logic low	$T_a = -40\text{ to }125^{\circ}\text{C}$			0.8	V
V_{IH}	Control input logic high	$T_a = -40\text{ to }125^{\circ}\text{C}$	2			V
I_I	Control input current	$V_I = 6\text{ V}$, $V_C = 6\text{ V}$		10		μA
C_O	Output bypass capacitance	$\text{ESR} = 0.1\text{ to }10\text{ }\Omega$, $I_O = 0\text{ to }500\text{ mA}$	2	10		μF

Table 5. Electrical characteristics for KF25 (refer to the test circuits, $T_J = 25\text{ }^{\circ}\text{C}$, $C_I = 0.1\text{ }\mu\text{F}$, $C_O = 2.2\text{ }\mu\text{F}$ unless otherwise specified.)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	$I_O = 50\text{ mA}$, $V_I = 4.5\text{ V}$	2.45	2.5	2.55	V
		$I_O = 50\text{ mA}$, $V_I = 4.5\text{ V}$, $T_a = -25\text{ to }85^{\circ}\text{C}$	2.4		2.6	
V_I	Operating input voltage	$I_O = 500\text{ mA}$			20	V
I_O	Output current limit			1		A
ΔV_O	Line regulation	$V_I = 3.5\text{ to }20\text{ V}$, $I_O = 5\text{ mA}$		2	12	mV
ΔV_O	Load regulation	$V_I = 3.8\text{ V}$, $I_O = 5\text{ to }500\text{ mA}$		2	50	mV
I_d	Quiescent current	$V_I = 3.5\text{ to }20\text{ V}$, $I_O = 0\text{ mA}$	ON MODE	0.5	1	mA
		$V_I = 3.8\text{ to }20\text{ V}$, $I_O = 500\text{ mA}$			12	
		$V_I = 6\text{ V}$	OFF MODE	50	100	μA
SVR	Supply voltage rejection	$I_O = 5\text{ mA}$, $V_I = 4.5 \pm 1\text{ V}$	$f = 120\text{ Hz}$	82		dB
			$f = 1\text{ kHz}$	77		
			$f = 10\text{ kHz}$	60		
eN	Output noise voltage	$B = 10\text{ Hz to }100\text{ KHz}$		50		μV
V_d	Dropout voltage	$I_O = 200\text{ mA}$		0.2	0.35	V
		$I_O = 500\text{ mA}$		0.4	0.7	
V_{IL}	Control input logic low	$T_a = -40\text{ to }125^{\circ}\text{C}$			0.8	V
V_{IH}	Control input logic high	$T_a = -40\text{ to }125^{\circ}\text{C}$	2			V
I_I	Control input current	$V_I = 6\text{ V}$, $V_C = 6\text{ V}$		10		μA
C_O	Output bypass capacitance	$\text{ESR} = 0.1\text{ to }10\text{ }\Omega$, $I_O = 0\text{ to }500\text{ mA}$	2	10		μF

Table 6. Electrical characteristics for KF33 (refer to the test circuits, $T_J = 25^\circ\text{C}$, $C_I = 0.1\ \mu\text{F}$, $C_O = 2.2\ \mu\text{F}$ unless otherwise specified.)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	$I_O = 50\ \text{mA}$, $V_I = 5.3\ \text{V}$	3.234	3.3	3.366	V
		$I_O = 50\ \text{mA}$, $V_I = 5.3\ \text{V}$, $T_a = -25\ \text{to}\ 85^\circ\text{C}$	3.168		3.432	
V_I	Operating input voltage	$I_O = 500\ \text{mA}$			20	V
I_O	Output current limit			1		A
ΔV_O	Line regulation	$V_I = 4.3\ \text{to}\ 20\ \text{V}$, $I_O = 5\ \text{mA}$		2	12	mV
ΔV_O	Load regulation	$V_I = 4.6\ \text{V}$, $I_O = 5\ \text{to}\ 500\ \text{mA}$		2	50	mV
I_d	Quiescent current	$V_I = 4.3\ \text{to}\ 20\ \text{V}$, $I_O = 0\ \text{mA}$	ON MODE	0.5	1	mA
		$V_I = 4.6\ \text{to}\ 20\ \text{V}$, $I_O = 500\ \text{mA}$			12	
		$V_I = 6\ \text{V}$	OFF MODE	50	100	μA
SVR	Supply voltage rejection	$I_O = 5\ \text{mA}$, $V_I = 5.3 \pm 1\ \text{V}$	$f = 120\ \text{Hz}$	80		dB
			$f = 1\ \text{kHz}$	75		
			$f = 10\ \text{kHz}$	60		
eN	Output noise voltage	$B = 10\ \text{Hz to}\ 100\ \text{kHz}$		50		μV
V_d	Dropout voltage	$I_O = 200\ \text{mA}$		0.2	0.35	V
		$I_O = 500\ \text{mA}$		0.4	0.7	
V_{IL}	Control input logic low	$T_a = -40\ \text{to}\ 125^\circ\text{C}$			0.8	V
V_{IH}	Control input logic high	$T_a = -40\ \text{to}\ 125^\circ\text{C}$	2			V
I_I	Control input current	$V_I = 6\ \text{V}$, $V_C = 6\ \text{V}$		10		μA
C_O	Output bypass capacitance	$\text{ESR} = 0.1\ \text{to}\ 10\ \Omega$, $I_O = 0\ \text{to}\ 500\ \text{mA}$	2	10		μF

Table 7. Electrical characteristics for KF40 (refer to the test circuits, $T_J = 25^\circ\text{C}$, $C_I = 0.1\ \mu\text{F}$, $C_O = 2.2\ \mu\text{F}$ unless otherwise specified.)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	$I_O = 50\ \text{mA}$, $V_I = 6\ \text{V}$	3.92	4	4.08	V
		$I_O = 50\ \text{mA}$, $V_I = 6\ \text{V}$, $T_a = -25\ \text{to}\ 85^\circ\text{C}$	3.84		4.16	
V_I	Operating input voltage	$I_O = 500\ \text{mA}$			20	V
I_O	Output current limit			1		A
ΔV_O	Line regulation	$V_I = 5\ \text{to}\ 20\ \text{V}$, $I_O = 5\ \text{mA}$		3	18	mV
ΔV_O	Load regulation	$V_I = 5.3\ \text{V}$, $I_O = 5\ \text{to}\ 500\ \text{mA}$		2	50	mV
I_d	Quiescent current	$V_I = 5\ \text{to}\ 20\ \text{V}$, $I_O = 0\ \text{mA}$	ON MODE	0.5	1	mA
		$V_I = 5.3\ \text{to}\ 20\ \text{V}$, $I_O = 500\ \text{mA}$			12	
		$V_I = 6\ \text{V}$	OFF MODE	50	100	μA
SVR	Supply voltage rejection	$I_O = 5\ \text{mA}$, $V_I = 6 \pm 1\ \text{V}$	$f = 120\ \text{Hz}$	78		dB
			$f = 1\ \text{kHz}$	73		
			$f = 10\ \text{kHz}$	60		
eN	Output noise voltage	$B = 10\ \text{Hz to}\ 100\ \text{KHz}$		50		μV
V_d	Dropout voltage	$I_O = 200\ \text{mA}$		0.2	0.35	V
		$I_O = 500\ \text{mA}$		0.4	0.7	
V_{IL}	Control input logic low	$T_a = -40\ \text{to}\ 125^\circ\text{C}$			0.8	V
V_{IH}	Control input logic high	$T_a = -40\ \text{to}\ 125^\circ\text{C}$	2			V
I_I	Control input current	$V_I = 6\ \text{V}$, $V_C = 6\ \text{V}$		10		μA
C_O	Output bypass capacitance	$\text{ESR} = 0.1\ \text{to}\ 10\ \Omega$, $I_O = 0\ \text{to}\ 500\ \text{mA}$	2	10		μF

Table 8. Electrical characteristics for KF50 (refer to the test circuits, $T_J = 25\text{ }^{\circ}\text{C}$, $C_I = 0.1\text{ }\mu\text{F}$, $C_O = 2.2\text{ }\mu\text{F}$ unless otherwise specified.)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	$I_O = 50\text{ mA}$, $V_I = 7\text{ V}$	4.9	5	5.1	V
		$I_O = 50\text{ mA}$, $V_I = 7\text{ V}$, $T_a = -25\text{ to }85^{\circ}\text{C}$	4.8		5.2	
V_I	Operating input voltage	$I_O = 500\text{ mA}$			20	V
I_O	Output current limit			1		A
ΔV_O	Line regulation	$V_I = 6\text{ to }20\text{ V}$, $I_O = 5\text{ mA}$		3	18	mV
ΔV_O	Load regulation	$V_I = 6.3\text{ V}$, $I_O = 5\text{ to }500\text{ mA}$		2	50	mV
I_d	Quiescent current	$V_I = 6\text{ to }20\text{ V}$, $I_O = 0\text{ mA}$	ON MODE	0.5	1	mA
		$V_I = 6.3\text{ to }20\text{ V}$, $I_O = 500\text{ mA}$			12	
		$V_I = 6\text{ V}$	OFF MODE	50	100	μA
SVR	Supply voltage rejection	$I_O = 5\text{ mA}$, $V_I = 7 \pm 1\text{ V}$	$f = 120\text{ Hz}$	76		dB
			$f = 1\text{ kHz}$	71		
			$f = 10\text{ kHz}$	60		
eN	Output noise voltage	$B = 10\text{ Hz to }100\text{ KHz}$		50		μV
V_d	Dropout voltage	$I_O = 200\text{ mA}$		0.2	0.35	V
		$I_O = 500\text{ mA}$		0.4	0.7	
V_{IL}	Control input logic low	$T_a = -40\text{ to }125^{\circ}\text{C}$			0.8	V
V_{IH}	Control input logic high	$T_a = -40\text{ to }125^{\circ}\text{C}$	2			V
I_I	Control input current	$V_I = 6\text{ V}$, $V_C = 6\text{ V}$		10		μA
C_O	Output bypass capacitance	$\text{ESR} = 0.1\text{ to }10\text{ }\Omega$, $I_O = 0\text{ to }500\text{ mA}$	2	10		μF

Table 9. Electrical characteristics for KF80 (refer to the test circuits, $T_J = 25\text{ }^{\circ}\text{C}$, $C_I = 0.1\text{ }\mu\text{F}$, $C_O = 2.2\text{ }\mu\text{F}$ unless otherwise specified.)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	$I_O = 50\text{ mA}$, $V_I = 10\text{ V}$	7.84	8	8.16	V
		$I_O = 50\text{ mA}$, $V_I = 10\text{ V}$, $T_a = -25\text{ to }85^{\circ}\text{C}$	7.68		8.32	
V_I	Operating input voltage	$I_O = 500\text{ mA}$			20	V
I_O	Output current limit			1		A
ΔV_O	Line regulation	$V_I = 9\text{ to }20\text{ V}$, $I_O = 5\text{ mA}$		4	24	mV
ΔV_O	Load regulation	$V_I = 9.3\text{ V}$, $I_O = 5\text{ to }500\text{ mA}$		2	50	mV
I_d	Quiescent current	$V_I = 9\text{ to }20\text{ V}$, $I_O = 0\text{ mA}$	ON MODE	0.7	1.5	mA
		$V_I = 9.3\text{ to }20\text{ V}$, $I_O = 500\text{ mA}$			12	
		$V_I = 9\text{ V}$	OFF MODE	70	140	μA
SVR	Supply voltage rejection	$I_O = 5\text{ mA}$, $V_I = 10 \pm 1\text{ V}$	$f = 120\text{ Hz}$	72		dB
			$f = 1\text{ kHz}$	67		
			$f = 10\text{ kHz}$	60		
eN	Output noise voltage	$B = 10\text{ Hz to }100\text{ KHz}$		50		μV
V_d	Dropout voltage	$I_O = 200\text{ mA}$		0.2	0.35	V
		$I_O = 500\text{ mA}$		0.4	0.7	
V_{IL}	Control input logic low	$T_a = -40\text{ to }125^{\circ}\text{C}$			0.8	V
V_{IH}	Control input logic high	$T_a = -40\text{ to }125^{\circ}\text{C}$	2			V
I_I	Control input current	$V_I = 6\text{ V}$, $V_C = 6\text{ V}$		10		μA
C_O	Output bypass capacitance	$\text{ESR} = 0.1\text{ to }10\text{ }\Omega$, $I_O = 0\text{ to }500\text{ mA}$	2	10		μF

5 Typical performance characteristics

(unless otherwise specified $V_{O(NOM)} = 3.3\text{ V}$)

Figure 4. Dropout voltage vs output current

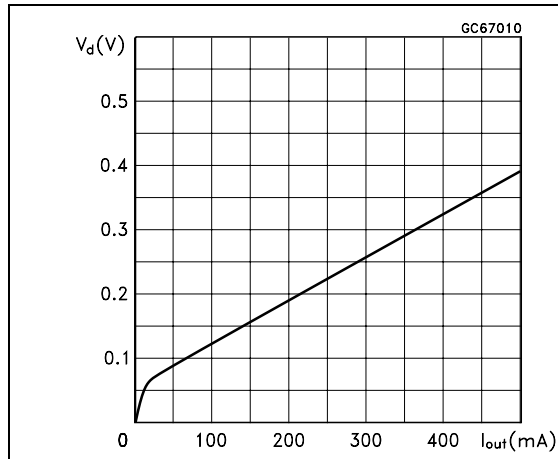


Figure 5. Dropout voltage vs temperature

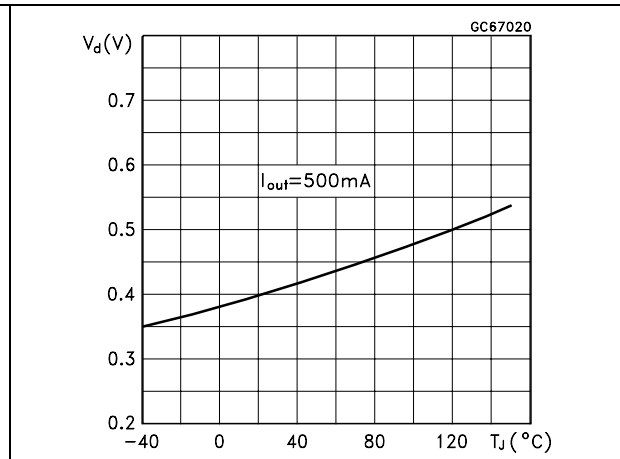


Figure 6. Supply current vs input voltage

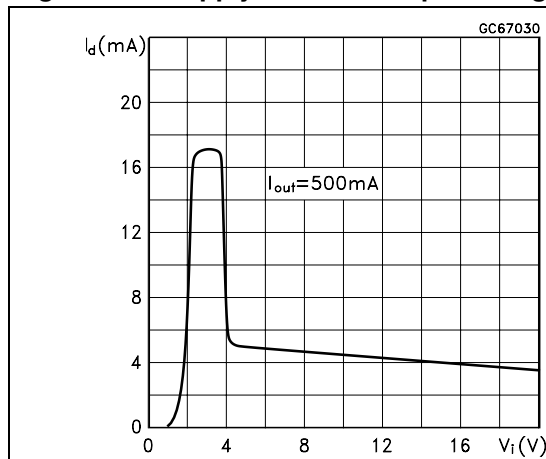


Figure 7. Supply current vs input voltage

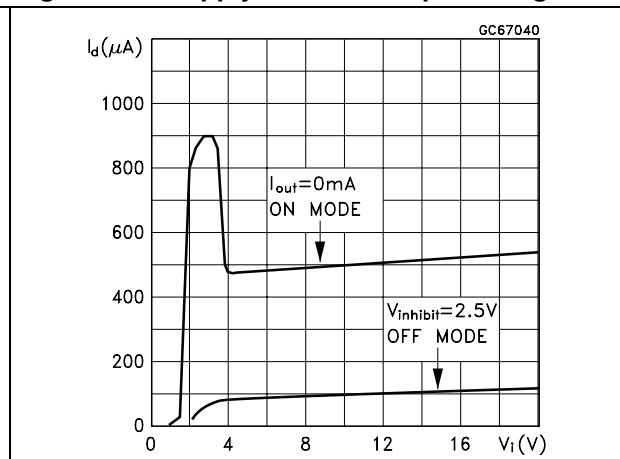


Figure 8. Short circuit current vs input voltage

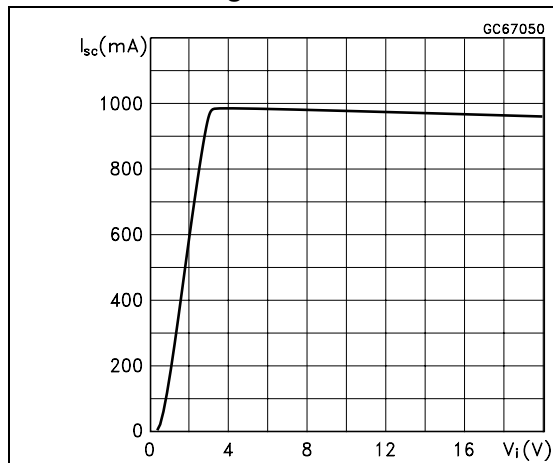
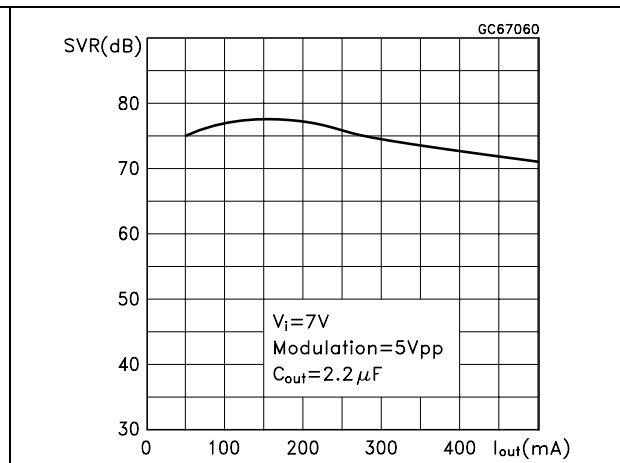


Figure 9. Supply current vs temperature

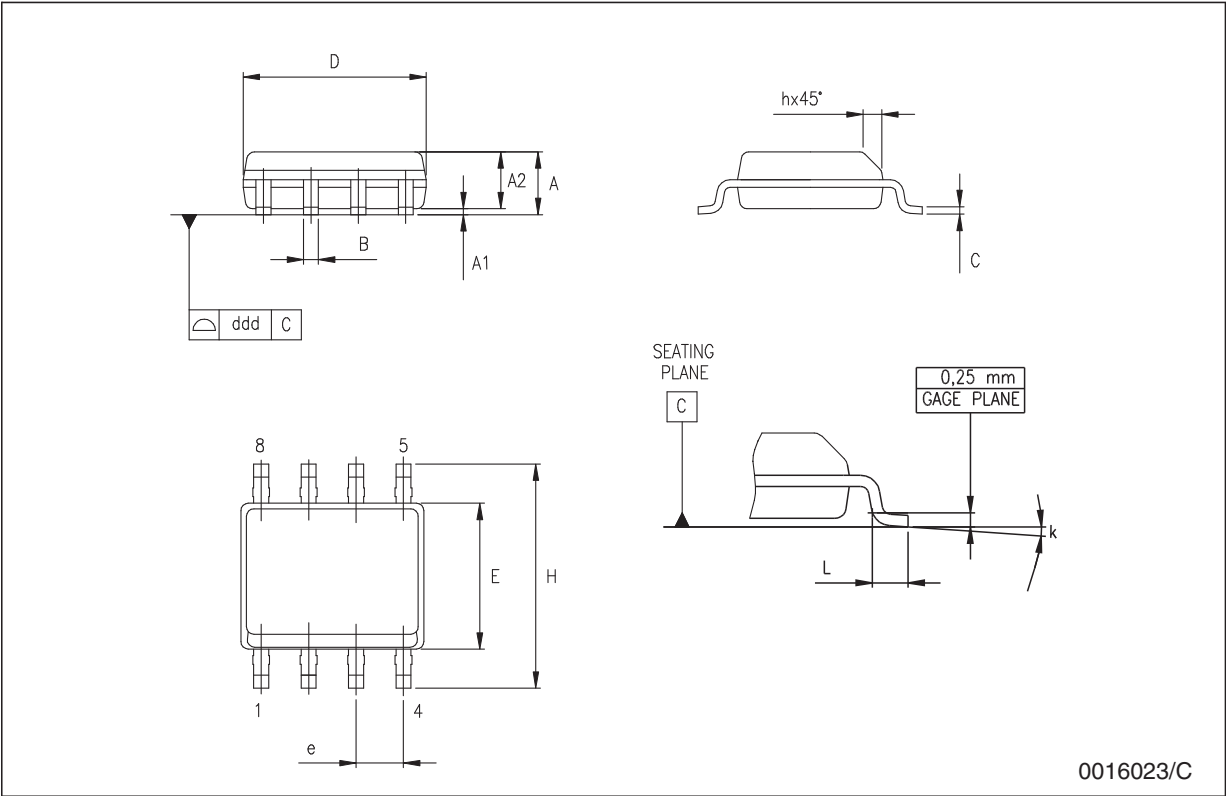


6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

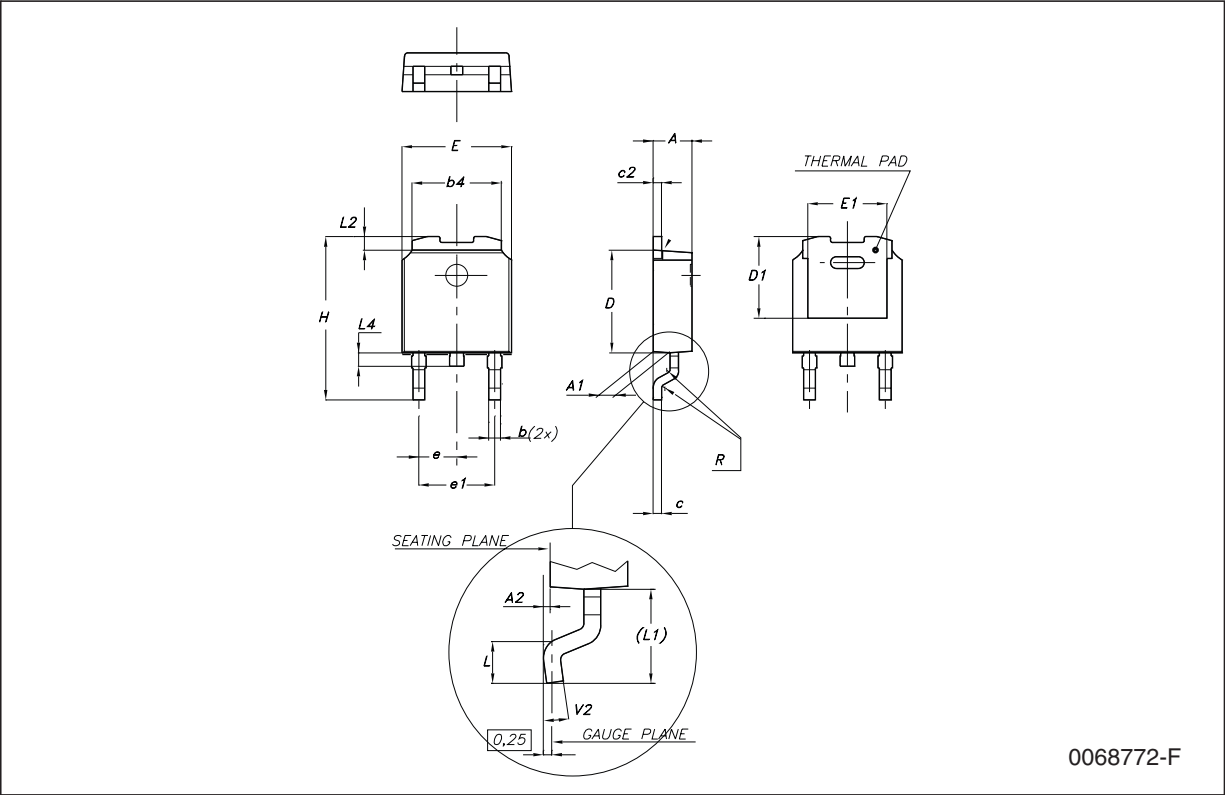
SO-8 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



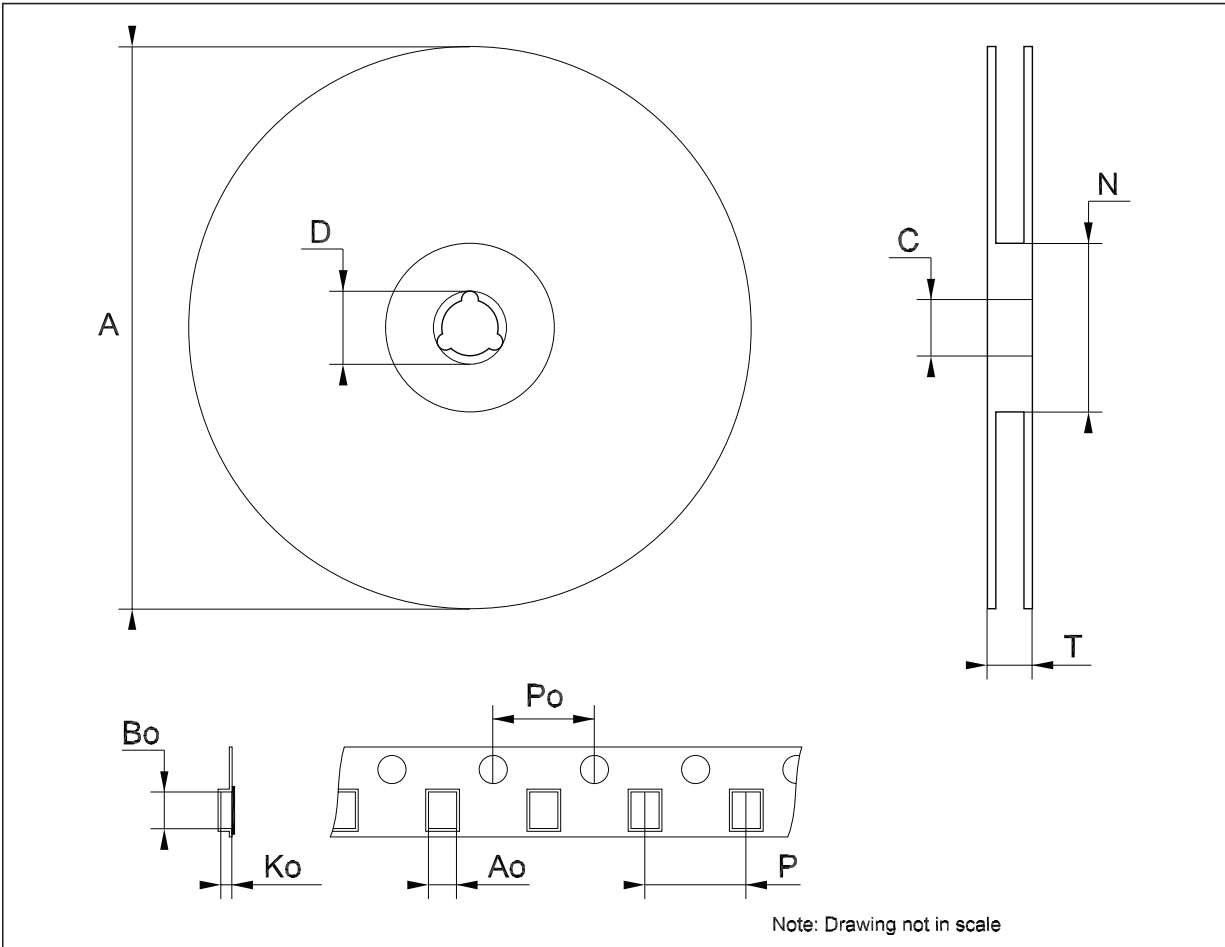
DPAK mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



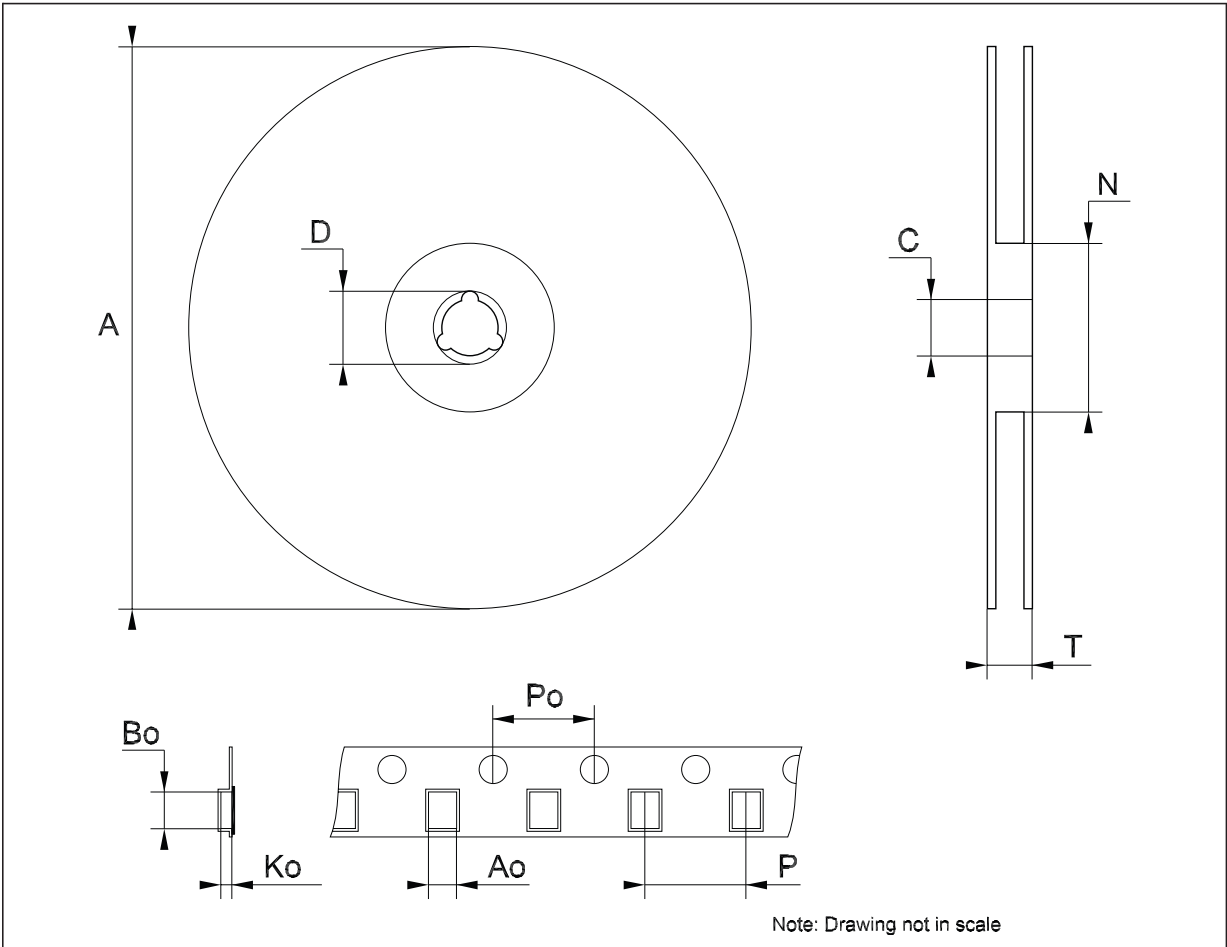
Tape & reel SO-8 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.1		8.5	0.319		0.335
Bo	5.5		5.9	0.216		0.232
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Tape & reel DPAK-PPAK mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.80	6.90	7.00	0.268	0.272	0.276
Bo	10.40	10.50	10.60	0.409	0.413	0.417
Ko	2.55	2.65	2.75	0.100	0.104	0.105
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	7.9	8.0	8.1	0.311	0.315	0.319



7 Order codes

Table 10. Order codes

Packages		Output voltage
SO-8 (tape and reel)	DPAK (tape and reel)	
	KF15BDT-TR	1.5 V
KF25BD-TR	KF25BDT-TR	2.5 V
KF33BD-TR	KF33BDT-TR	3.3 V
	KF40BDT-TR	4 V
KF50BD-TR	KF50BDT-TR	5 V
	KF80BDT-TR	8 V

8 Revision history

Table 11. Document revision history

Date	Revision	Changes
06-Jun-2007	9	Order codes updated.
14-Dec-2007	10	Modified: Table 10 .
21-Feb-2008	11	Modified: Table 10 on page 18 .

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